Electronics
Logic Gates: Measuring Voltage Limits

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• Similarly, output voltages will not always be at ideal values. A range of output values should be considered high. Another range of output values should be considered low.
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Input voltages will not always be at ideal values, a range of input values must be considered high, another range of input values must be considered low.

Similarly output voltages will not always be at ideal values, a range of output voltages should be considered as high, another range of output voltages should be considered low.
\( V_{IH_{\text{min}}} \)
\( V_{IH_{\text{min}}} \)

the *minimum* input voltage which will be accepted as a logic 1.
• $V_{IH_{\text{min}}}$
  the \textit{minimum} input voltage which will be accepted as a logic 1.
• $V_{IL_{\text{max}}}$
- \( V_{IH_{\text{min}}} \)
  the *minimum* input voltage which will be accepted as a logic 1.

- \( V_{IL_{\text{max}}} \)
  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{IH_{\text{min}}}$
  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{\text{max}}}$
  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{\text{min}}}$
- $V_{IH_{min}}$
  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{max}}$
  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{min}}$
  the *minimum* output voltage representing a logic 1 state.
- $V_{IH_{\text{min}}}$
  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{\text{max}}}$
  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{\text{min}}}$
  the *minimum* output voltage representing a logic 1 state.
- $V_{OL_{\text{max}}}$
- $V_{IH_{\min}}$
  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{\max}}$
  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{\min}}$
  the *minimum* output voltage representing a logic 1 state.
- $V_{OL_{\max}}$
  the *maximum* output voltage representing a logic 0 state.
The actual limits on voltage, current, timing, etc. will be given in manufacturer’s data sheets. Different manufacturers arrange their data sheets differently, and use different names.
Reading Data sheets

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Supply voltage Designations

The supply voltages for various families have names which are based on the type of transistors used in their construction. For instance, TTL gates are made with bipolar transistors, which have a collector and an emitter, the supply voltages are $V_{CC}$ and GROUND is occasionally given as $V_{EE}$.

On the other hand, CMOS gates are built with field–effect transistors which have a drain and a source, the supply voltages are $V_{DD}$ and $V_{SS}$. 

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Measuring voltage limits

In order to measure the voltage limits, you can connect up the circuit as in the following figure.
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Real logic gates
Measuring voltage limits

V_{cc}
V_{in}
GND
Using a sine wave input with the oscilloscope operating in the X–Y mode, a trace similar to the one shown in the following figure should be obtained.
Using a sine wave input with the oscilloscope operating in the X–Y mode, a trace similar to the one shown in the following figure should be obtained.
(The output shown is for an LSTTL *inverting* gate.)
$V_{in}$
Real logic gates
Measuring voltage limits

\[ V_{out} \]

\[ V_{in} \]

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Real logic gates
Measuring voltage limits

![Diagram showing voltage limits for logic gates](image)

- $V_{OH_{min}}$
- $V_{out}$
- $V_{in}$

Logic "0" input

$V_{in}$: 0.8

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Real logic gates

Measuring voltage limits

$V_{in}$ $V_{out}$

logic “1” input

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\[ V_{out} \]

\[ V_{OL_{\text{max}}} \]

\[ V_{in} \]

2.0

logic "1" input

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Real logic gates
Measuring voltage limits

\[ V_{out} \]

\[ V_{in} \]

- 0.5
logic "0"
output

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Real logic gates
Measuring voltage limits

V_{\text{in}} \quad V_{\text{out}}

- 0.5
logic “0”
output

V_{\text{IH_{min}}}

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Real logic gates
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logic "1"
output
-
2.7

$V_{out}$

$V_{in}$

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Real logic gates

Measuring voltage limits

logic “1” output

$V_{out}$

$V_{IL_{max}}$ $V_{in}$

$V_{in}$

$2.7$
This is called the **transfer characteristic** of the gate.
This is called the **transfer characteristic** of the gate. Note that the input voltage, $V_{in}$, is on the X axis and the output voltage, $V_{out}$, on the Y axis.
Real logic gates

Measuring voltage limits

$V_{out}$

$V_{in}$

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Real logic gates
Measuring voltage limits

CMOS will look slightly different.
Measuring Output Voltage Limits

The output voltage produced by an input voltage of the specified value of $V_{IL_{\text{max}}}$ would be the measured value of $V_{OH_{\text{min}}}$.

The output voltage is produced by an input voltage of the specified value of $V_{IH_{\text{min}}}$ would be the measured value of $V_{OL_{\text{max}}}$.
The output voltage produced by an input voltage of the specified value of $V_{IL_{\text{max}}}$ would be the measured value of $V_{OH_{\text{min}}}$. 
The output voltage produced by an input voltage of the specified value of $V_{IL\text{max}}$ would be the measured value of $V_{OH\text{min}}$.

The output voltage is produced by an input voltage of the specified value of $V_{IH\text{min}}$ would be the measured value of $V_{OL\text{max}}$. 
The output voltage produced by an input voltage of the specified value of $V_{IL\text{max}}$ would be the measured value of $V_{OH\text{min}}$.

The output voltage is produced by an input voltage of the specified value of $V_{IH\text{min}}$ would be the measured value of $V_{OL\text{max}}$. 

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