Electronics
Logic Gate Characteristics: Timing

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Ideal logic gates

In PC/CP220, logic gates are treated as “ideal” devices. As well, only one or perhaps two logic families were discussed. Now the real (i.e. non-ideal) operating characteristics of different logic families will be studied.

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• Inputs will draw no current from whatever drives them, and outputs can supply as much current as necessary for whatever follows.
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Any change of an input will immediately be reflected on the output.
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another range of input values must be considered \textit{low}. Similarly output voltages will not always be at ideal values. A range of output voltages should be considered \textit{high}

another range of output voltages should be considered \textit{low}. Changes made at the inputs will take a finite amount of time to be reflected on the outputs. Inputs must draw a small but finite amount of current from whatever is driving them in order that they will be recognized. Outputs have a limited current capacity for maintaining the output voltage at the desired level.
Input voltages will not always be at ideal values. A range of input values must be considered high, and another range of input values must be considered low.

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Reading Data sheets

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Logic families

The real limitations on voltages, timing, and currents depend on the logic family involved. Note that usually comparing “real” to “ideal” values involves seeing how close one number, (the “real” value) is to another (the “ideal” value). With digital logic chips, however, rather than having a single “ideal” value for a parameter, the manufacturers give bounds for it instead. This is because these specifications are not values that should be matched, but rather they are values that should be considered as limits that one should achieve even in the “worst case” during real operation.
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For instance, if a family has a nominal input “high” voltage of 5 volts, then any voltage above some voltage will be considered “high”.
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If an actual gate accepts a slightly lower voltage as a high, then that is not surprising and in fact is desirable.
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Here’s a very simple circuit; a single inverter.
This is what you *expect* the output to look like...
This is what the output *actually* looks like.
Note the output is shifted right due to the propagation delay of the gate.
Zoomed in, the delay is around 10 nS.
Here the output is going from LOW to HIGH.
Here the output is going from HIGH to LOW.
In general, the two delays needn’t be the same.
Timing Limits

Ideally changes to the inputs of a gate would be reflected at the output immediately, but in reality there is a slight delay. In general, the delay may be different depending on whether the gate's output is going from low to high or from high to low. Furthermore, the transitions themselves are not instantaneous, so they are defined as being at the 50% point of the voltage transitions. Thus there are two quantities of interest:
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Note that in both cases above, the direction of the *input* transition is immaterial.
Measuring timing limits
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In order to measure timing limits, you can wire up the circuit as in the following figure and use the oscilloscope to measure $V_{in}$ and $V_{out}$. 
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*Why can we not measure both \(t_{PHL}\) and \(t_{PLH}\) from the circuit shown?*
In order to obtain a good measurement of the delay time, a frequency of operation should be chosen sufficiently high so that the total delay in the chain \( nt_p \) is comparable to the period of the input clock.
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<table>
<thead>
<tr>
<th>Delay Time (nS)</th>
<th>2V</th>
<th>3V</th>
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