

Electronics

Logic Gate Characteristics: Timing

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- Now the real (i.e. non-ideal) operating characteristics of different logic families will be studied.
- The operation of an *ideal* logic gate can be summarized by the following rules:

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- Inputs will draw no current from whatever drives them, and outputs can supply as much current as necessary for whatever follows.
- Any change of an input will immediately be reflected on the output.

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A *real* logic gate operates under the following restrictions:

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- Inputs must draw a small but finite amount of current from whatever is driving them in order that they will be recognized.
- Outputs have a limited current capacity for maintaining the output voltage at the desired level.

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Different manufacturers arrange their data sheets differently, and use different names.

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- *With digital logic chips, however, rather than having a single “ideal” value for a parameter, the manufacturers give **bounds** for it instead.*

*This is because these **specifications** are not values that should be matched, but rather they are values that should be considered as limits that one should achieve even in the “worst case” during real operation.*

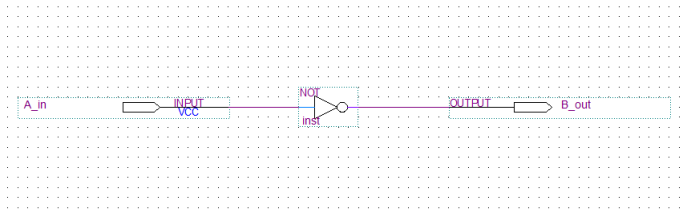
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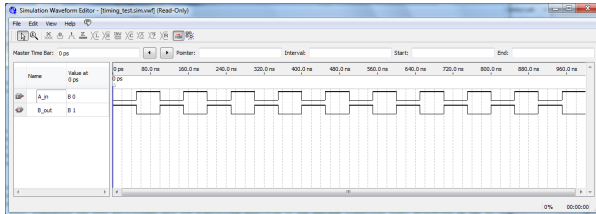
If an actual gate accepts a slightly lower voltage as a high, then that is not surprising and in fact is desirable.

Note that for some parameters the specifications will give an *upper* bound while for some they will give a *lower* bound.

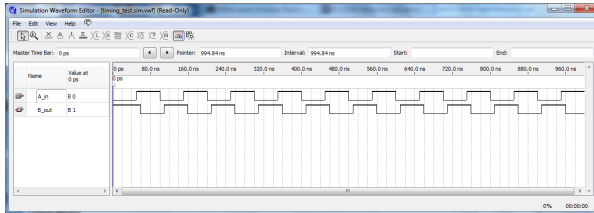
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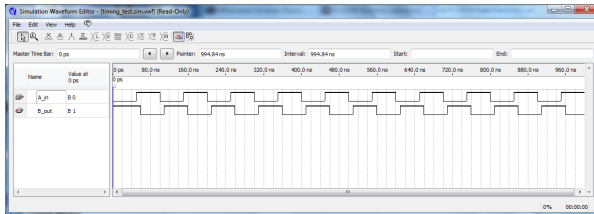
Here's a very simple circuit; a single inverter.



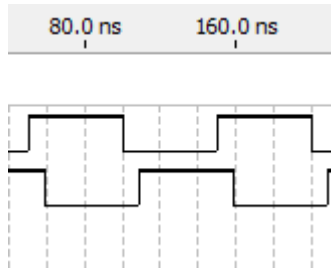
This is what you *expect* the output to look like...



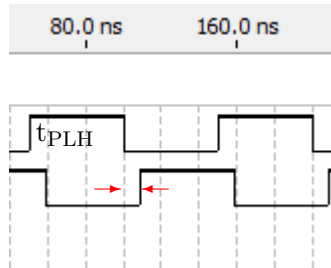
This is what the output *actually* looks like.



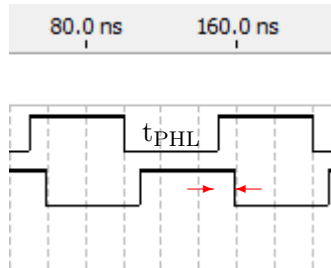
Note the output is shifted right due to the **propagation delay** of the gate.



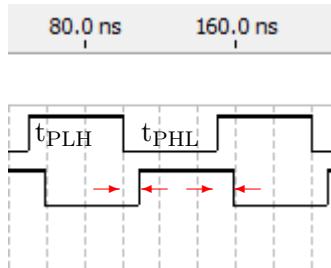
Zoomed in, the delay is around 10 nS.



Here the output is going from LOW to HIGH.



Here the output is going from HIGH to LOW.



In general, the two delays needn't be the same.

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Thus there are two quantities of interest:

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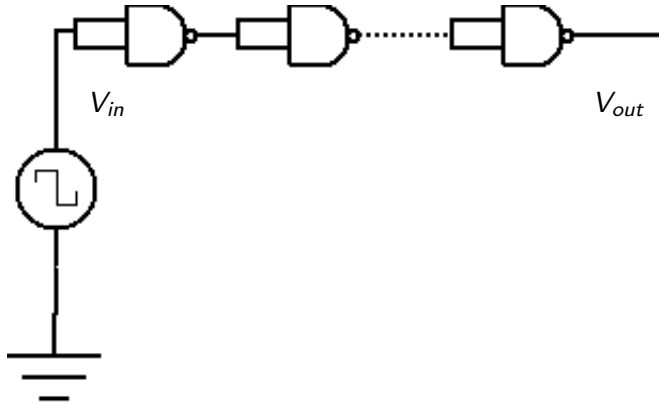
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Note that in both cases above, the direction of the *input* transition is immaterial.

Measuring timing limits

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In order to measure timing limits, you can wire up the circuit as in the following figure and use the oscilloscope to measure V_{in} and V_{out} .



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Why can we not measure both t_{PHL} and t_{PLH} from the circuit shown?

In order to obtain a good measurement of the delay time, a frequency of operation should be chosen sufficiently high so that the total delay in the chain (nt_p) is comparable to the period of the input clock.

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The propagation delay of a CMOS gate is not only a function of the load capacitance but also the supply voltage V_{DD} .

Delay Time (nS)		
2V	3V	6V
75	30	13

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74HC00A (ON Semiconductor)