Electronics
Logic Gate Characteristics: Timing

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  As well, only one or perhaps two logic families were discussed.
- Now the real (i.e. non-ideal) operating characteristics of different logic families will be studied.
- The operation of an *ideal* logic gate can be summarized by the following rules:

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- Any change of an input will immediately be reflected on the output.

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A *real* logic gate operates under the following restrictions:

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- Changes made at the inputs will take a finite amount of time to be reflected on the outputs.
- Inputs must draw a small but finite amount of current from whatever is driving them in order that they will be recognized.
- Outputs have a limited current capacity for maintaining the output voltage at the desired level.

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Different manufacturers arrange their data sheets differently, and use different names.

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- *With digital logic chips, however, rather than having a single "ideal" value for a parameter, the manufacturers give* ***bounds*** *for it instead.*

  This is because these ***specifications*** *are not values that should be matched, but rather they are values that should be considered as limits that one should achieve even in the "worst case" during real operation.*

- *For instance, if a family has a nominal input "high" voltage of 5 volts, then any voltage above some voltage will be considered "high".*

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  If an actual gate accepts a slightly lower voltage as a high, then that is not surprising and in fact is desirable.

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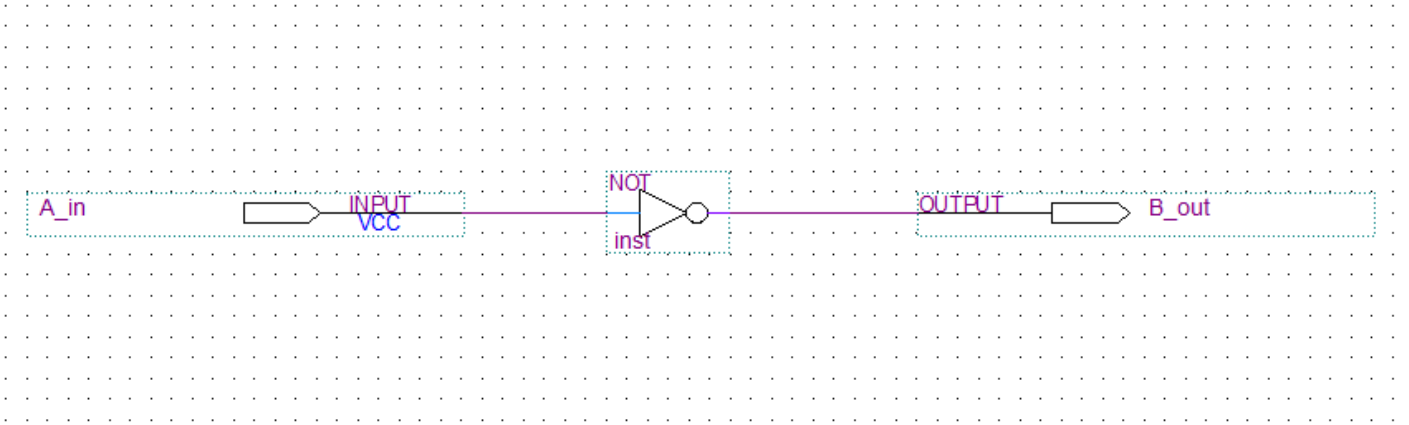
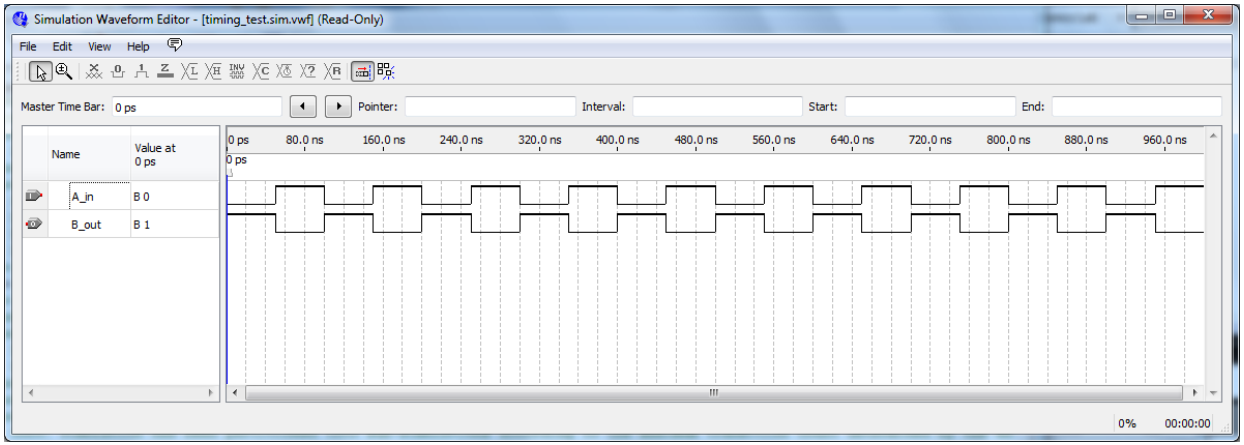
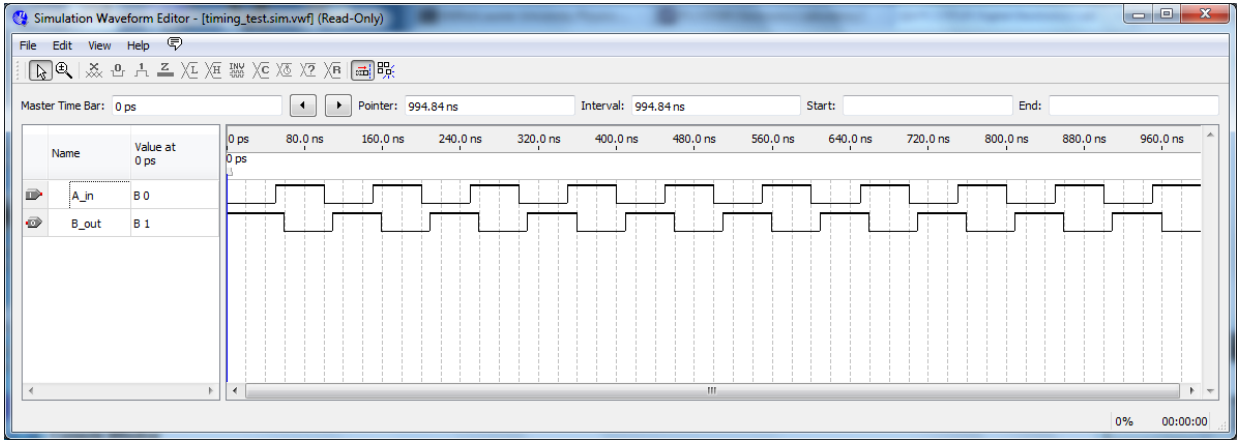
Which one is given will make sense if you understand what each parameter means.



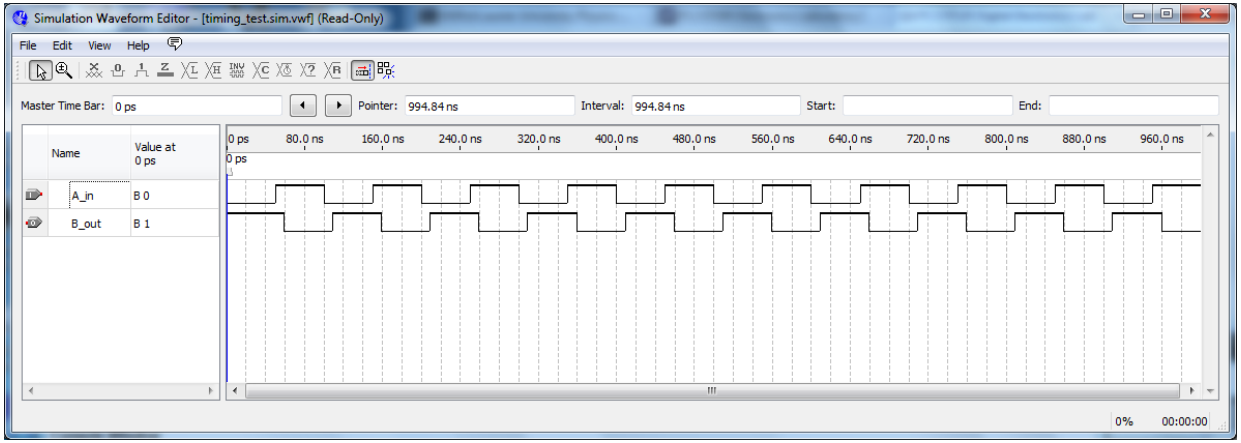
Here's a very simple circuit; a single inverter.



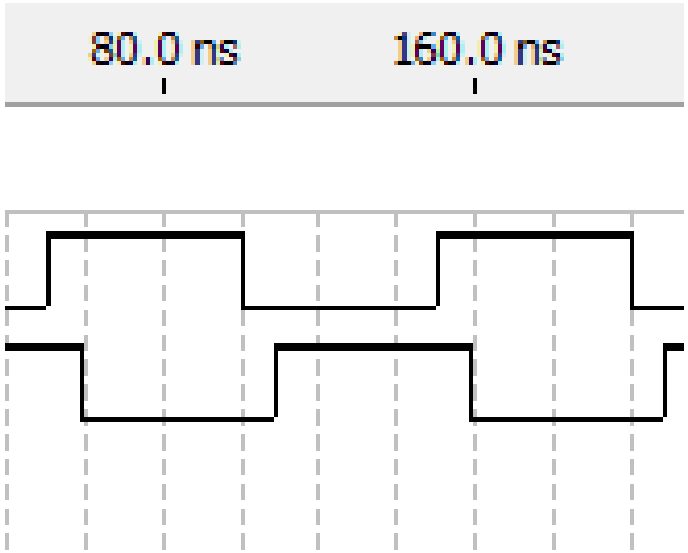
This is what you *expect* the output to look like...



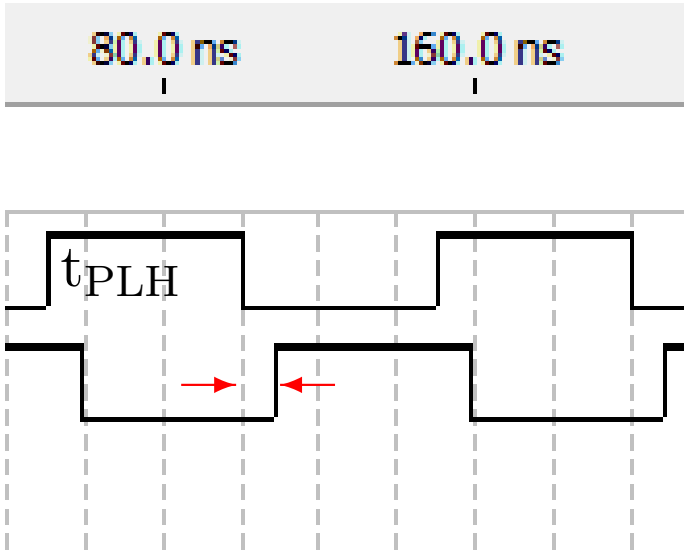
This is what the output *actually* looks like.



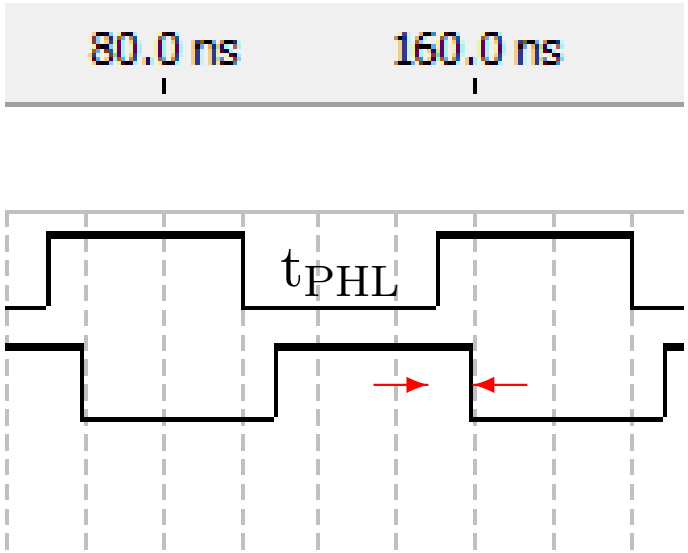
Note the output is shifted right due to the **propagation delay** of the gate.



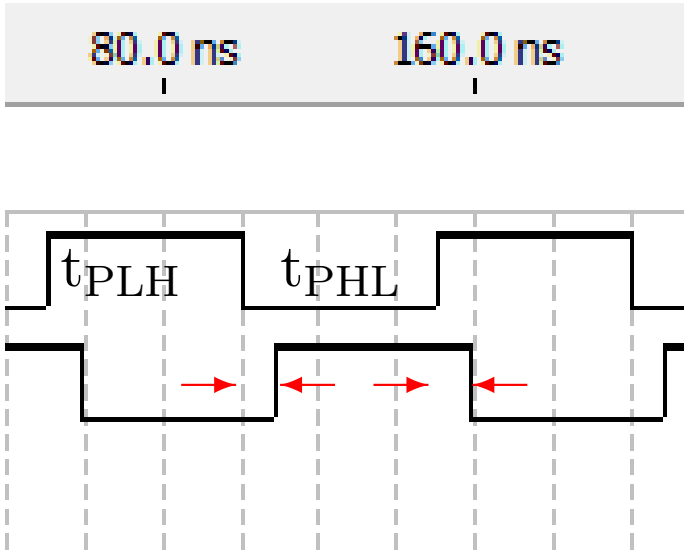
Zoomed in, the delay is around 10 nS.



Here the output is going from LOW to HIGH.



Here the output is going from HIGH to LOW.



In general, the two delays needn't be the same.

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Furthermore, the transitions themselves are not instantaneous, so they are defined as being at the 50% point of the voltage transitions.
Thus there are two quantities of interest:

- t_{PLH}

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  the time interval between the change of an input and the resulting change in output, when the *output* must change from low to high.

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Note that in both cases above, the direction of the *input* transition is immaterial.

Measuring timing limits

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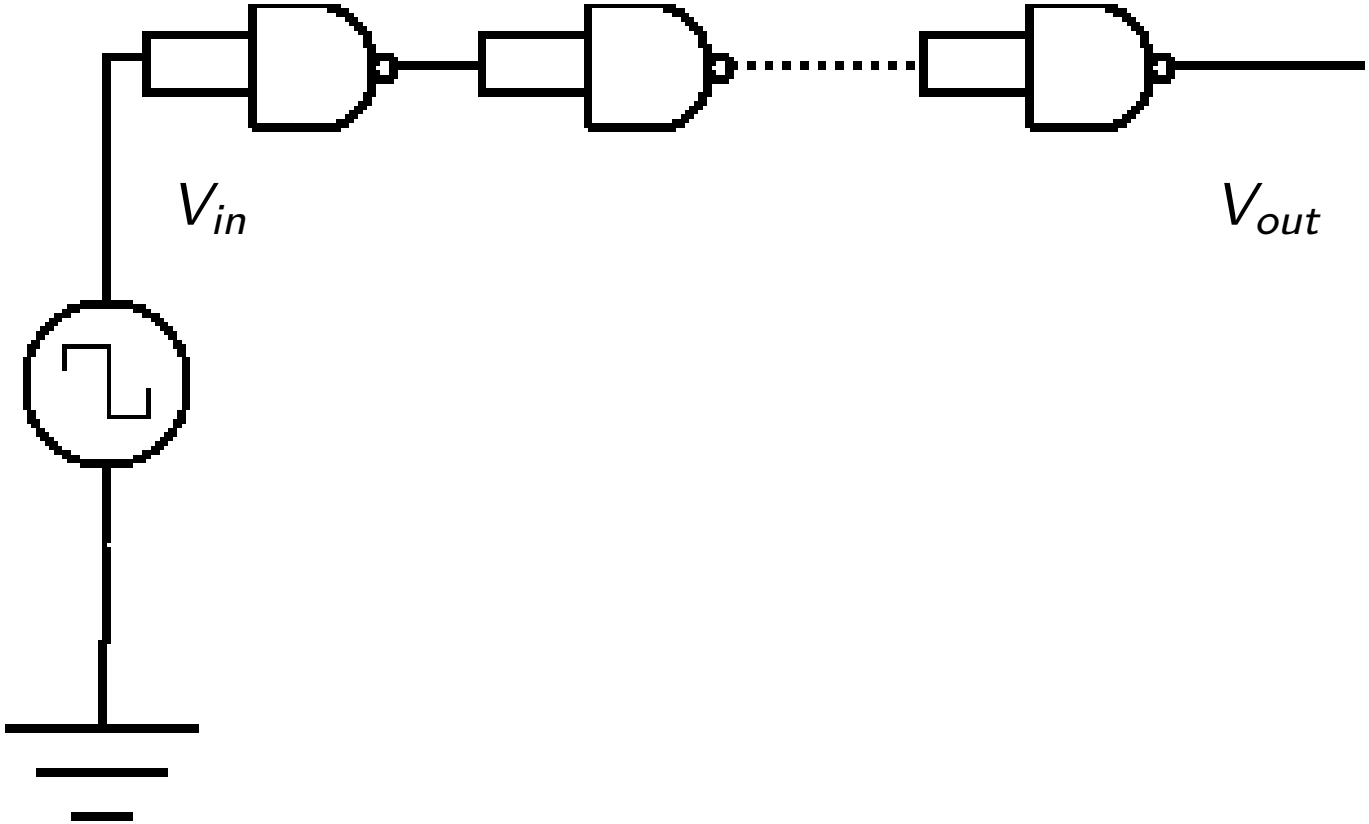
In order to measure timing limits, you can wire up the circuit as in the following figure and use the oscilloscope to measure $\mathrm{V_{in}}$ and $\mathrm{V_{out}}$.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Use a chain of gates (n = 8) as shown to determine the propagation delay $\mathrm{t_p}$ of a given family.
Why can we not measure both $\mathrm{t_{PHL}}$ *and* $\mathrm{t_{PLH}}$ *from the circuit shown?*

In order to obtain a good measurement of the delay time, a frequency of operation should be chosen sufficiently high so that the total delay in the chain ($\mathrm{nt_p}$) is comparable to the period of the input clock.

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The propagation delay of a CMOS gate is not only a function of the load capacitance but also the supply voltage $\mathrm{V_{DD}}$.

Delay Time (nS)		
2V	3V	6V
75	30	13

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74HC00A (ON Semiconductor)