Prime Number Indentifier Circuit
PC/CP220 Project Phase III

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Logic Equation

The numbers between 0 and 15 which are prime are: 2, 3, 5, 7, 11, and 13.

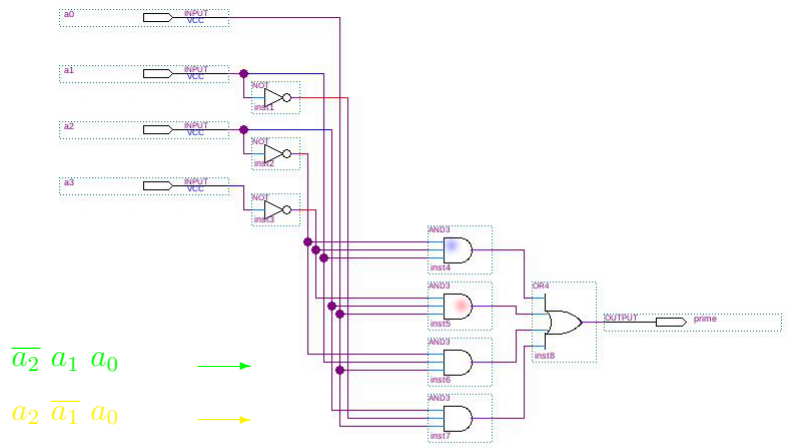
So, for the prime number identifier circuit, there is a single output and the final equation for the output is

$$prime = \overline{a_3}\ \overline{a_2}\ a_1 + \overline{a_3}\ a_2\ a_0 + \overline{a_2}\ a_1\ a_0 + a_2\ \overline{a_1}\ a_0$$

where a_3 is the *most* significant bit of the input, and a_0 is the *least* significant bit of the input.

Circuit Diagram

The circuit was drawn using Altera Quartus II, and is shown in the following figure.



The terms given by the following two terms are highlighted on the circuit diagram by dots of the corresponding colours on the AND gates.

- $\overline{a_3}\ \overline{a_2}\ a_1$
- $\overline{a_3}\ a_2\ a_0$

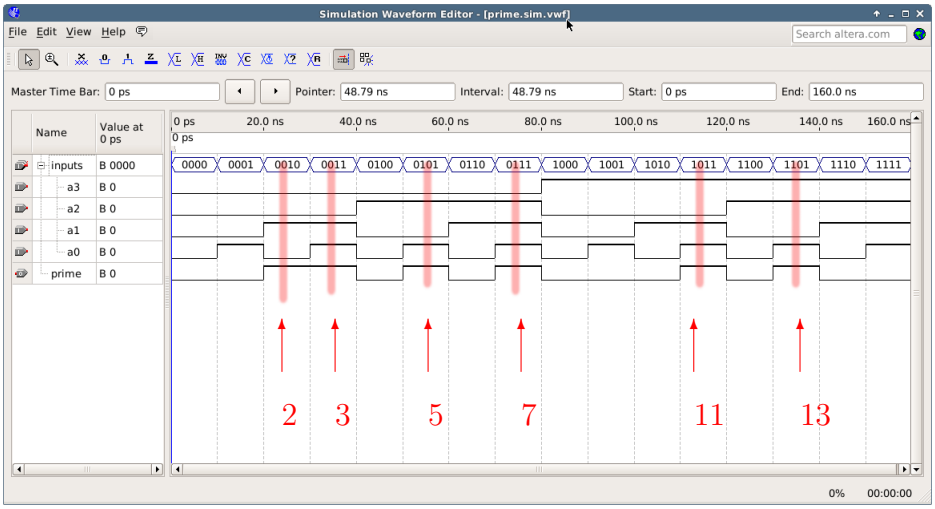
The other two terms

- $\overline{a_2}\ a_1\ a_0$
- $a_2\ \overline{a_1}\ a_0$

have been identified by arrows on the diagram.

Simulation Output

Following a simulation, the output shows that the result is true only for the correct input combinations, which have been highlighted.



Thus the circuit as drawn is correct.

Parts List

In addition to the CPLD, the circuit needs the following parts:

- DIP switch, for input
- Resistor array for the DIP switch; probably 1kΩ or so.
- Single LED for output
- Resistor for the LED; probably 510Ω or so.