Number of Segments Circuit
PC/CP220 Project Phase III

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Logic Equation

The equations for the outputs are:

$$b_2 = \overline{a_3}\ \overline{a_0} + a_3\ \overline{a_2}\ \overline{a_1} + \mathbf{\overline{a_3}\ \overline{a_2}\ a_1} + \overline{a_3}\ a_2\ \overline{a_1}$$

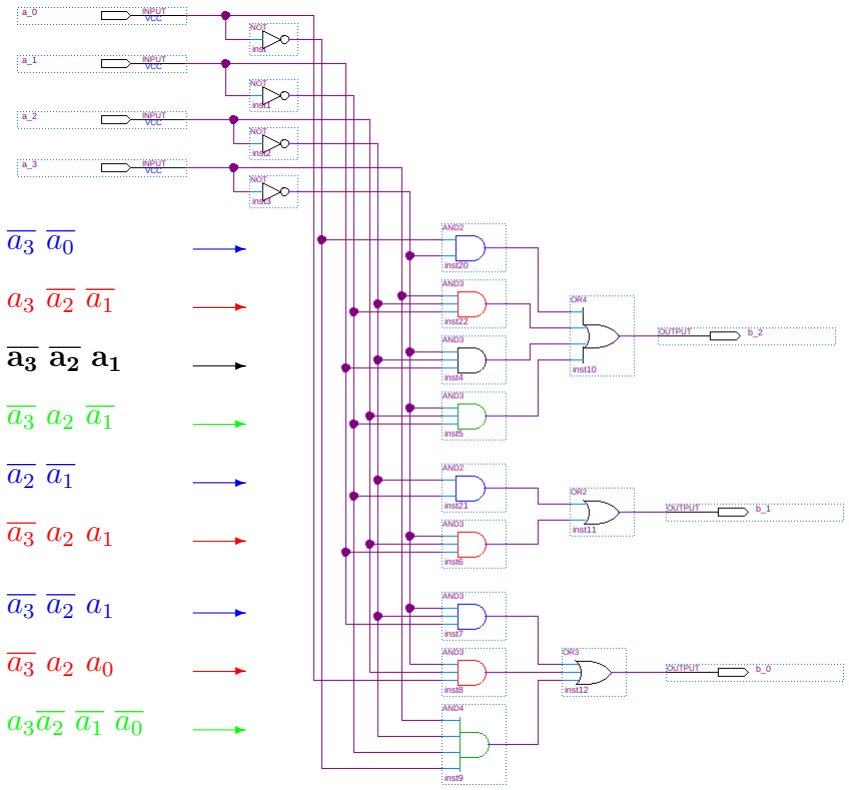
$$b_1 = \overline{a_2}\ \overline{a_1} + \overline{a_3}\ a_2\ a_1$$

$$b_0 = \overline{a_3}\ \overline{a_2}\ a_1 + \overline{a_3}\ a_2\ a_0 + a_3\overline{a_2}\ \overline{a_1}\ \overline{a_0}$$

where a_3 is the *most* significant bit of the input, and a_0 is the *least* significant bit of the input, and b_2 is the *most* significant bit of the output, and b_0 is the *least* significant bit of the output.

Circuit Diagram

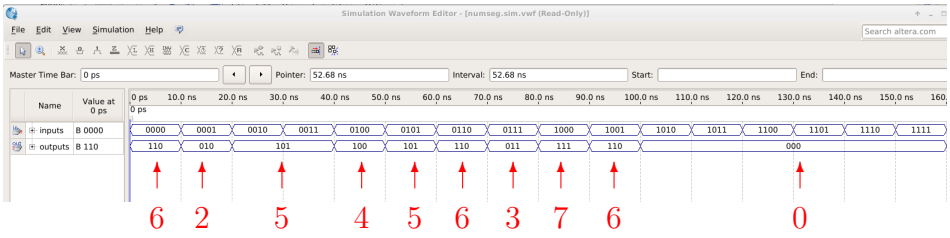
The circuit was drawn using Altera Quartus II, and is shown in the following figure.



The terms for each of the outputs are identified, and the corresponding gates are colour-coded in the same way to make it easy to identify each gate with its corresponding AND term in an equation.

Simulation Output

Following a simulation, the output shows that the output number given by $b_2b_1b_0$ is correct for each input combination. (The simulation output shows the binary values, and the annotation shows the numbers to make it easy to compare with the table from Phase I.)



Thus the circuit as drawn is correct.

Parts List

In addition to the CPLD, the circuit needs the following parts:

- Prototype switch, for input
- Resistors (4) for the prototype switches; probably 1kΩ or so.
- 7 segment decoder and display for the output
- Resistor for the 7 segment display common pin; probably 240Ω or so.