



1.

Input Voltage	Gate	Interpretation (high, low, indeterminate)
0.7 V	5-V TTL	
2.5 V	3.3-V LVTTTL	
2.5 V	5-V CMOS	
4.5 V	5-V CMOS	

2. For a 3.3-V LVTTTL logic gate, an output of a ‘high’ means that the output voltage is a minimum of \_\_\_\_\_ V.

3. You’re short on chips and need to combine a 5-V TTL gate, a 5-V CMOS gate, and a 3.3-V LVTTTL gate in a circuit. (Circle the True or False for each of the following.)

- T F You can combine the two 5-V gates because they are both 5-V chips.
- T F You can combine the two TTL gates because they are both in the TTL family.
- T F You can combine the two 5-V gates if the CMOS is before the TTL.
- T F You can combine the 5-V CMOS and the 3.3-V LVTTTL if the LVTTTL is before the CMOS.
- T F You can combine the two TTL gates if the TTL is before the LVTTTL.