Electronics
Logic Gates: Measuring Voltage Limits

Terry Sturtevant

Wilfrid Laurier University

November 20, 2014

- Input voltages will not always be at ideal values

- Input voltages will not always be at ideal values

  a *range* of input values must be considered *high*

- Input voltages will not always be at ideal values
  a *range* of input values must be considered *high*
  another range of input values must be considered *low*.

- Input voltages will not always be at ideal values

  a *range* of input values must be considered *high*

  another range of input values must be considered *low*.
- Similarly output voltages will not always be at ideal values

- Input voltages will not always be at ideal values

  a *range* of input values must be considered *high*

  another range of input values must be considered *low*.
- Similarly output voltages will not always be at ideal values

  a *range* of output voltages should be considered as *high*

- Input voltages will not always be at ideal values
  a *range* of input values must be considered *high*
  another range of input values must be considered *low*.
- Similarly output voltages will not always be at ideal values
  a *range* of output voltages should be considered as *high*
  another *range* of output voltages should be considered *low*.

- $V_{IH_{min}}$

- $V_{IH_{min}}$

  the *minimum* input voltage which will be accepted as a logic 1.

- $V_{IH_{min}}$
  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{max}}$

- $V_{IH_{min}}$

  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{max}}$

  the *maximum* input voltage which will be accepted as a logic 0.

- $V_{IH_{min}}$

  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{max}}$

  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{min}}$

- $V_{IH_{min}}$

  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{max}}$

  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{min}}$

  the *minimum* output voltage representing a logic 1 state.

- $V_{IH_{min}}$

  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{max}}$

  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{min}}$

  the *minimum* output voltage representing a logic 1 state.
- $V_{OL_{max}}$

- $V_{IH_{min}}$

  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{max}}$

  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{min}}$

  the *minimum* output voltage representing a logic 1 state.
- $V_{OL_{max}}$

  the *maximum* output voltage representing a logic 0 state.

Reading Data sheets

Reading Data sheets

The actual limits on voltage, current, timing, etc. will be given in manufacturer's **data sheets**.

Reading Data sheets

The actual limits on voltage, current, timing, etc. will be given in manufacturer's **data sheets**.

Different manufacturers arrange their data sheets differently, and use different names.

Supply voltage Designations

Supply voltage Designations

- The supply voltages for various families have names which are based on the type of transistors used in their construction.

Supply voltage Designations

- The supply voltages for various families have names which are based on the type of transistors used in their construction.

  For instance, TTL gates are made with **bipolar** transistors, which have a **c**ollector and an **e**mitter,

  the supply voltages are $\mathrm{V_{CC}}$ and GROUND is occasionally given as $\mathrm{V_{EE}}$.

Supply voltage Designations

- The supply voltages for various families have names which are based on the type of transistors used in their construction.

  For instance, TTL gates are made with **bipolar** transistors, which have a **c**ollector and an **e**mitter,

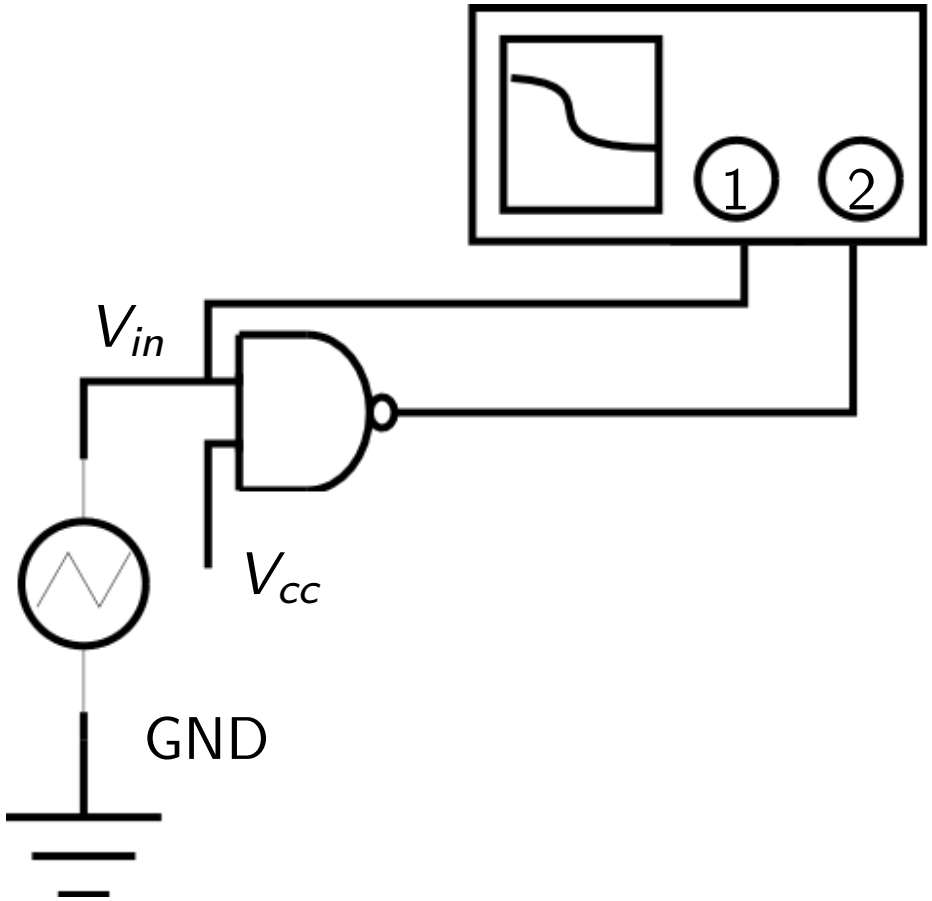
  the supply voltages are $\mathrm{V_{CC}}$ and GROUND is occasionally given as $\mathrm{V_{EE}}$.
- On the other hand, CMOS gates are built with **field–effect** transistors which have a **d**rain and a **s**ource,

  the supply voltages are $\mathrm{V_{DD}}$ and $\mathrm{V_{SS}}$.

Measuring voltage limits

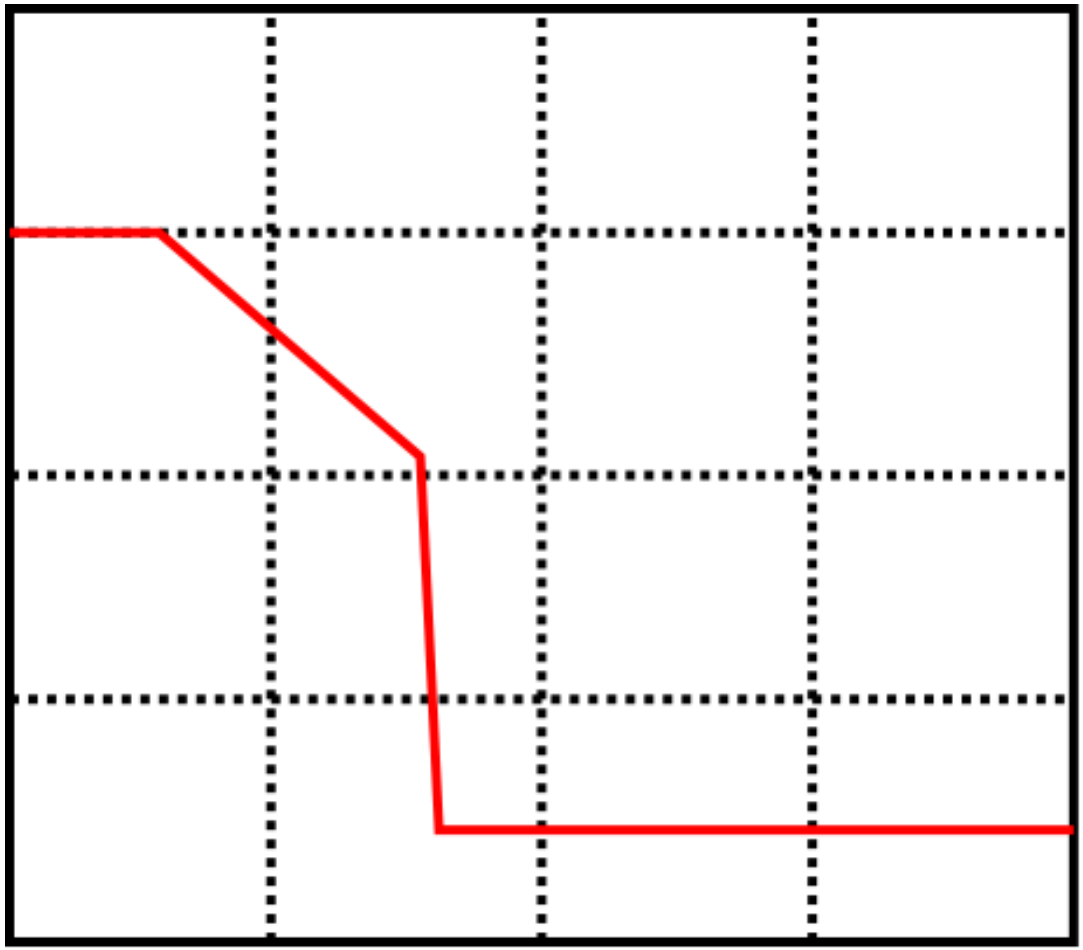
Measuring voltage limits

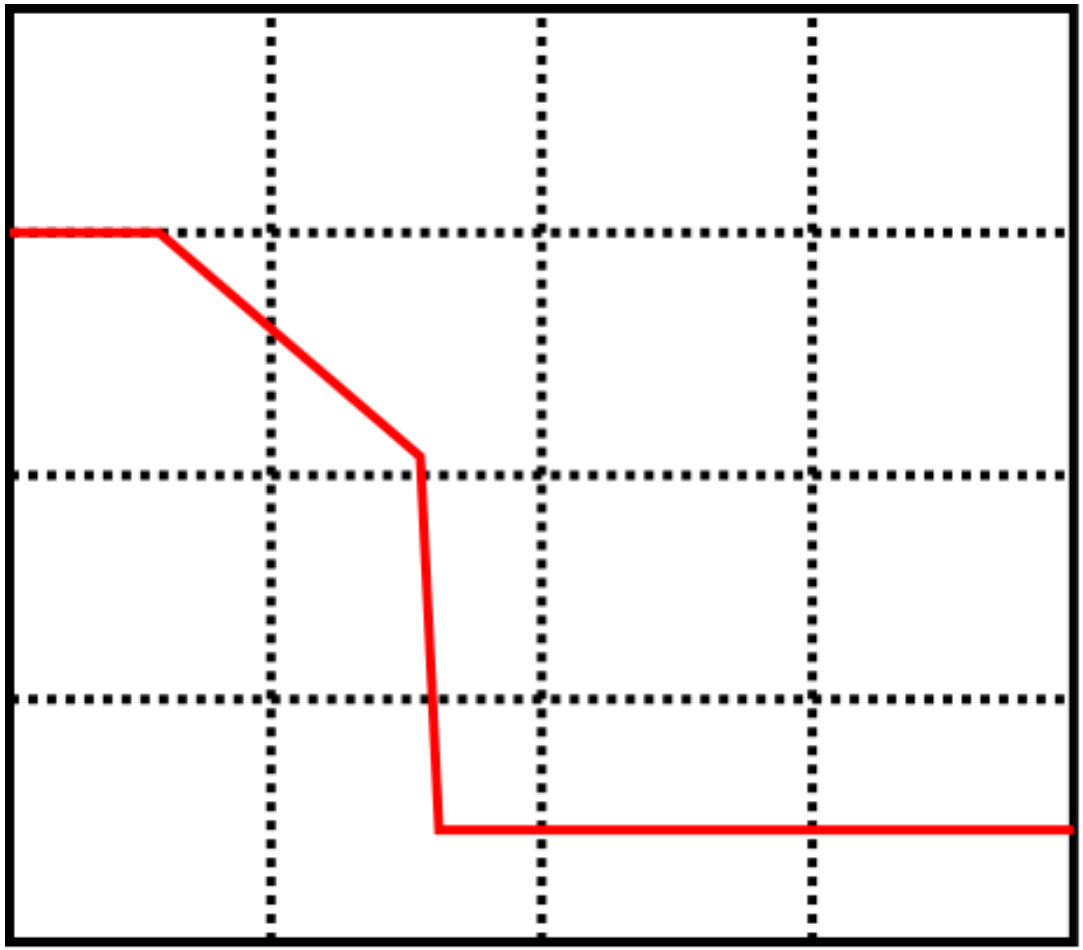
In order to measure the voltage limits, you can connect up the circuit as in the following figure.


1
2
V_{in}
V_{cc}
GND

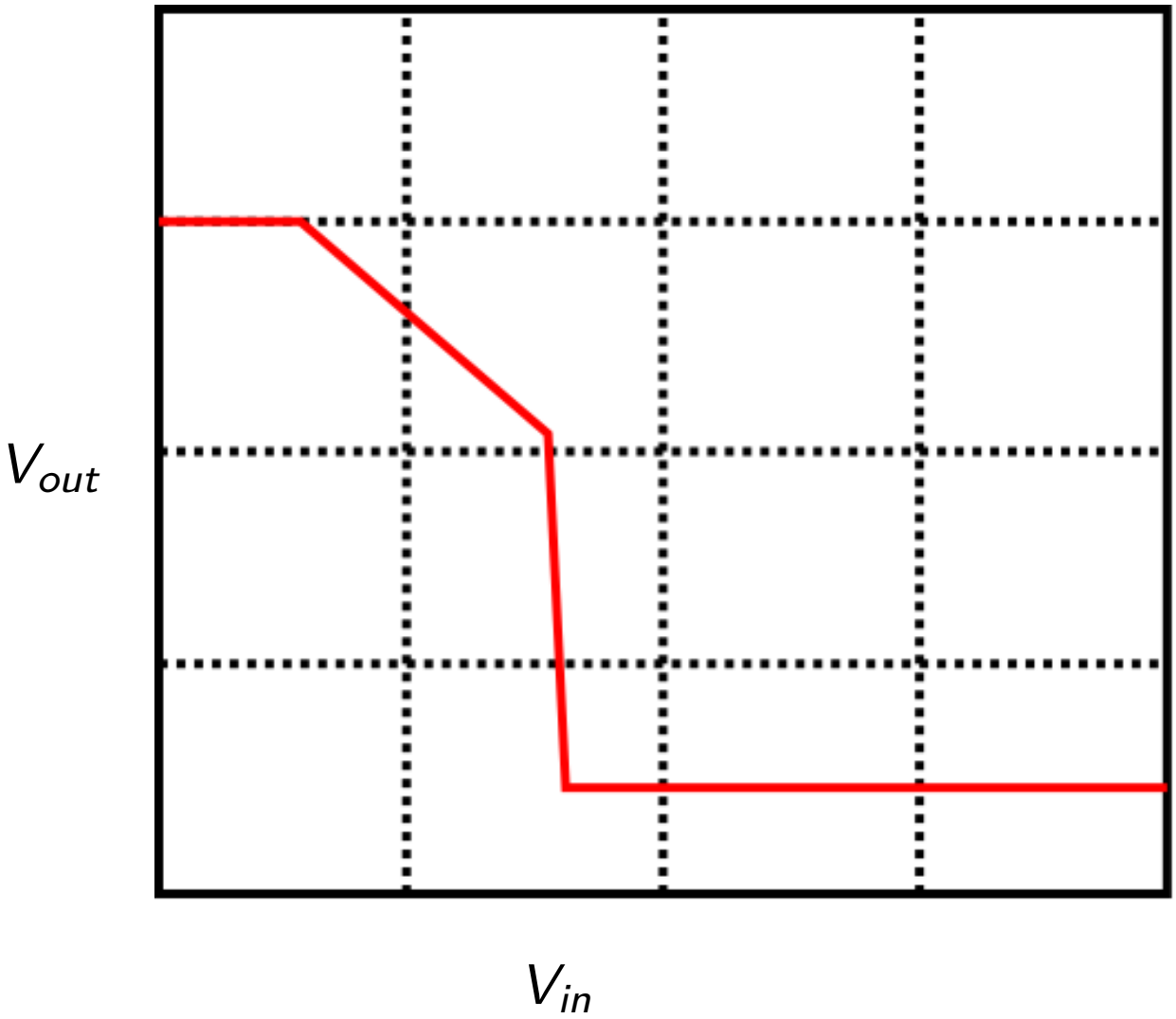
Using a sine wave input with the oscilloscope operating in the X–Y mode, a trace similar to the one shown in the following figure should be obtained.

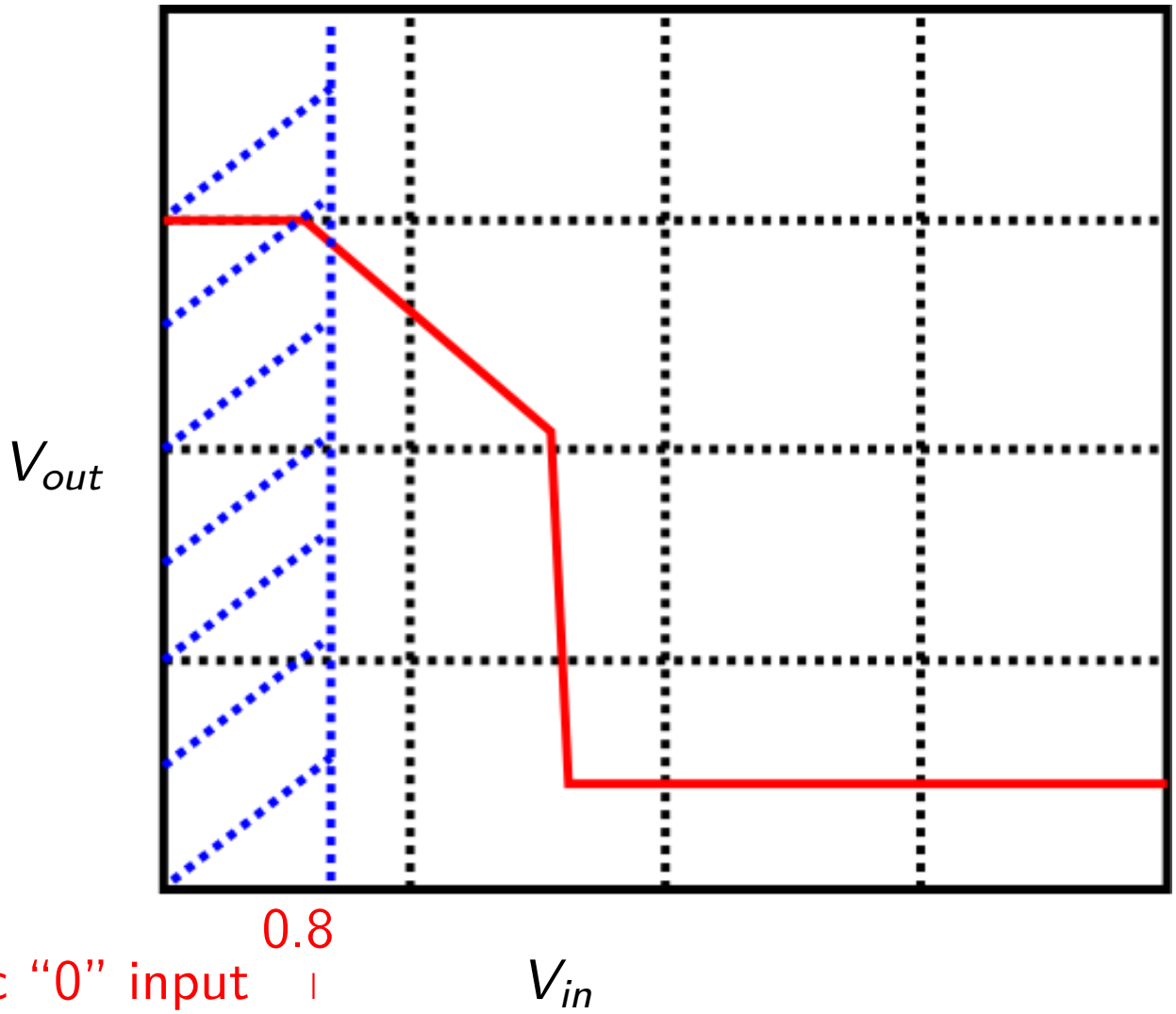
Using a sine wave input with the oscilloscope operating in the X–Y mode, a trace similar to the one shown in the following figure should be obtained.
(The output shown is for an LSTTL *inverting* gate.)

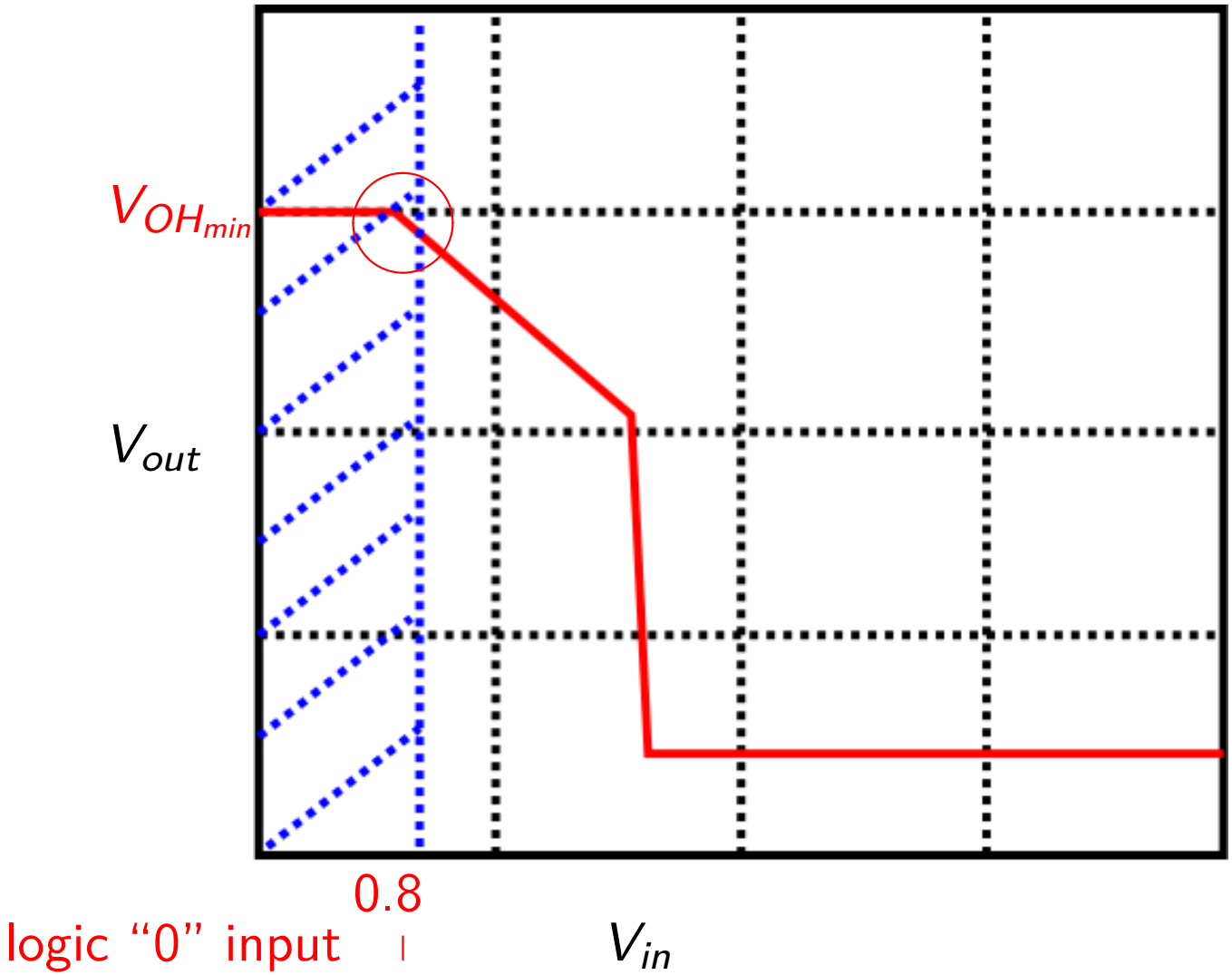


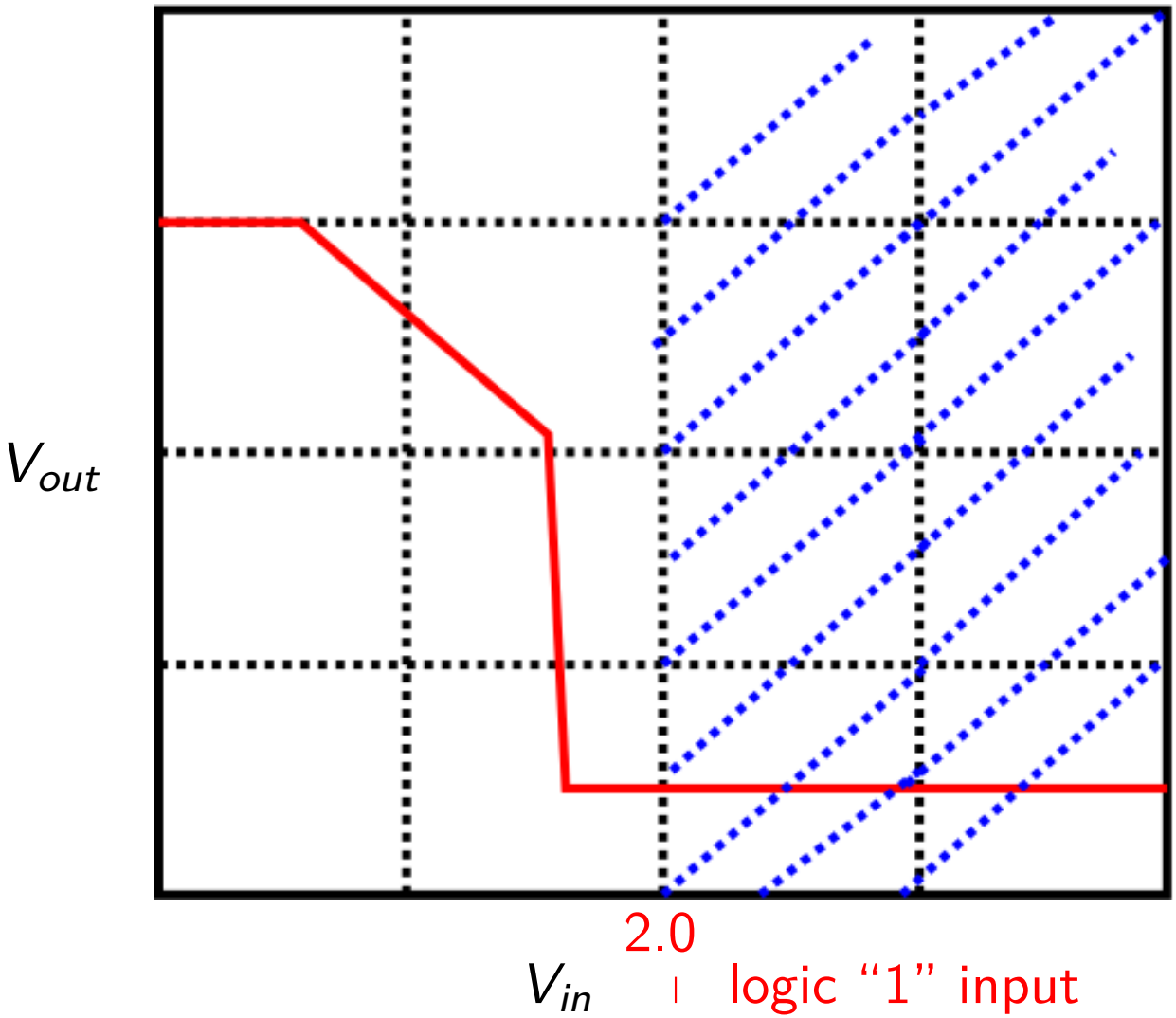


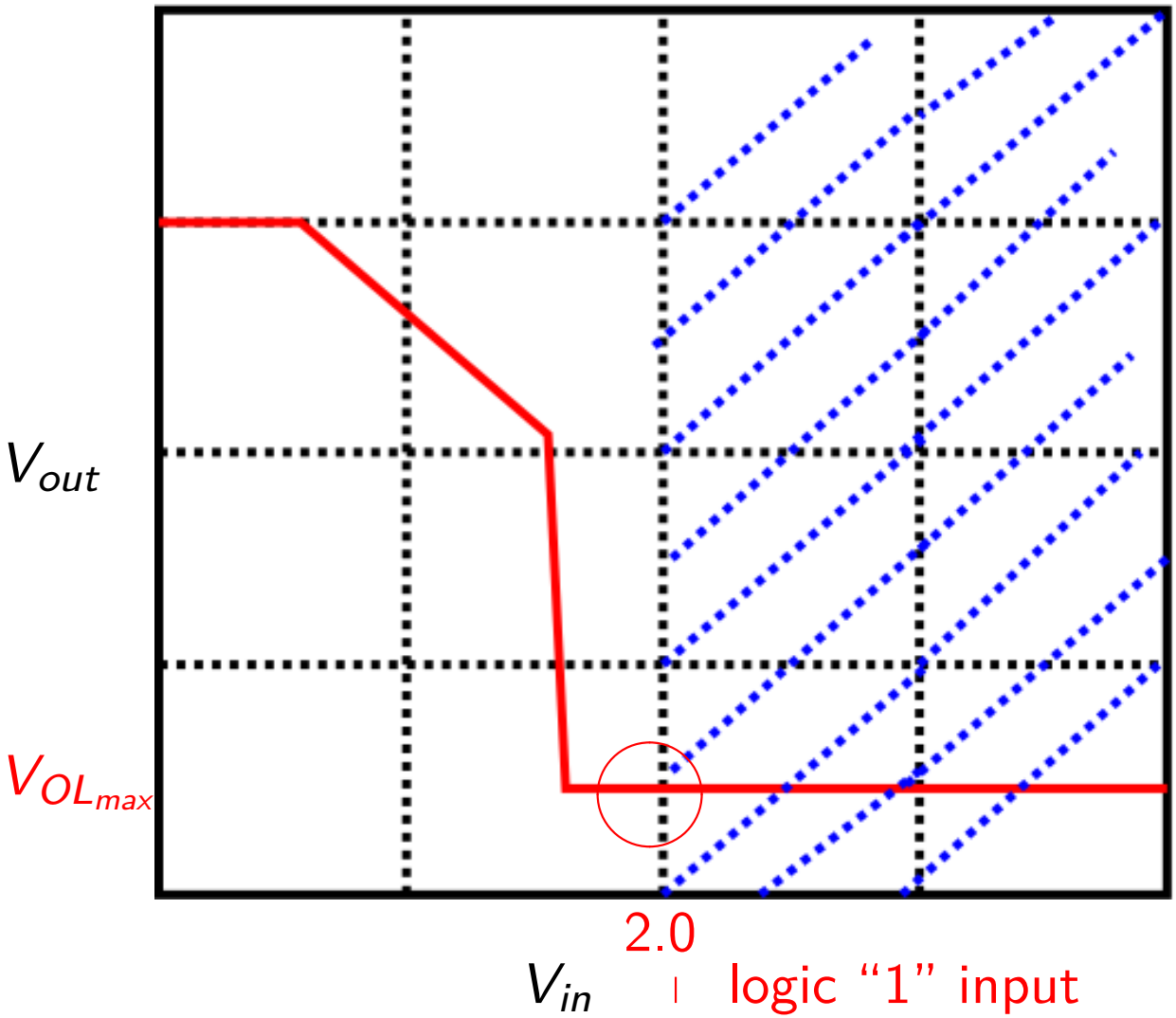
V_{in}

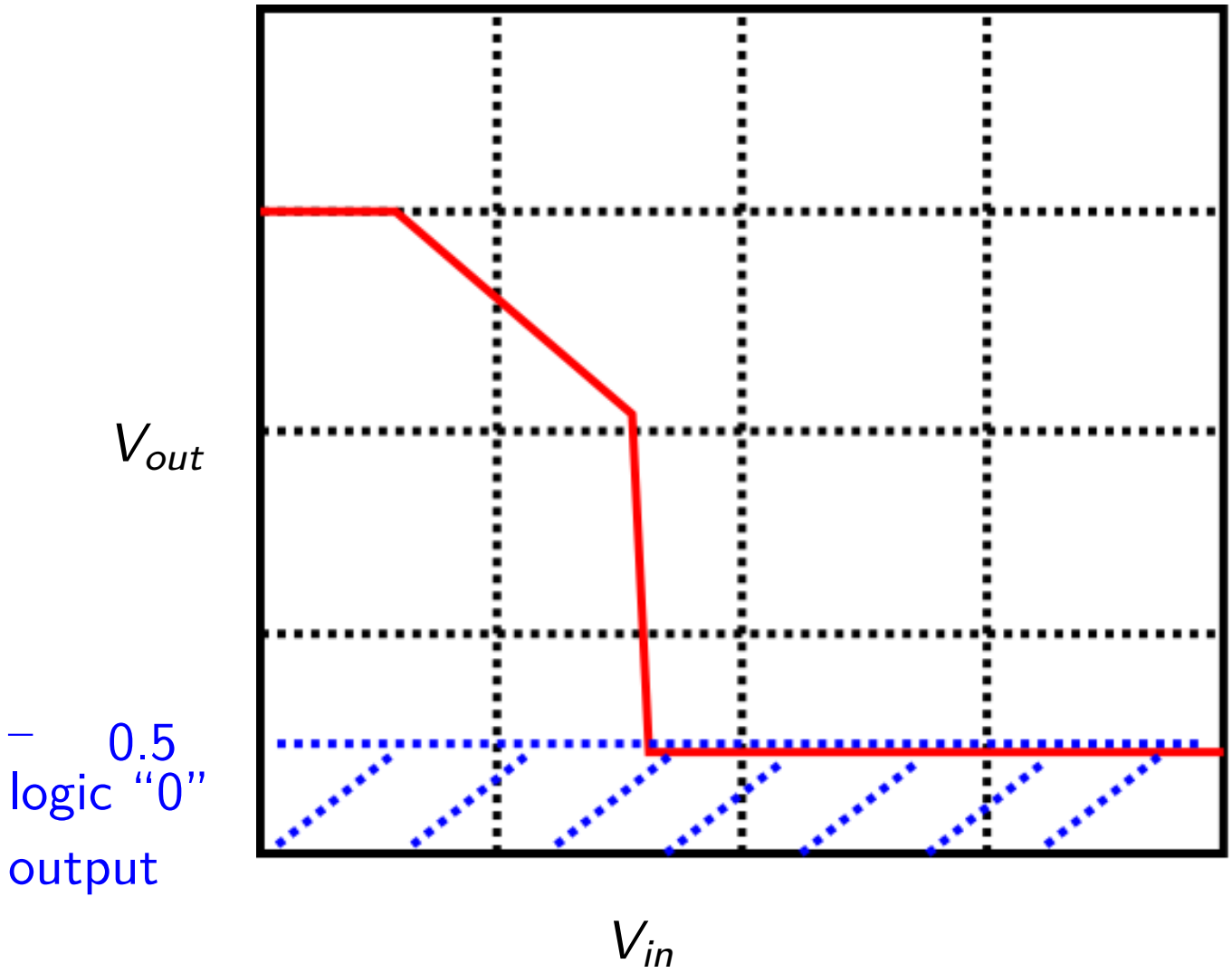

V_{out}
V_{in}

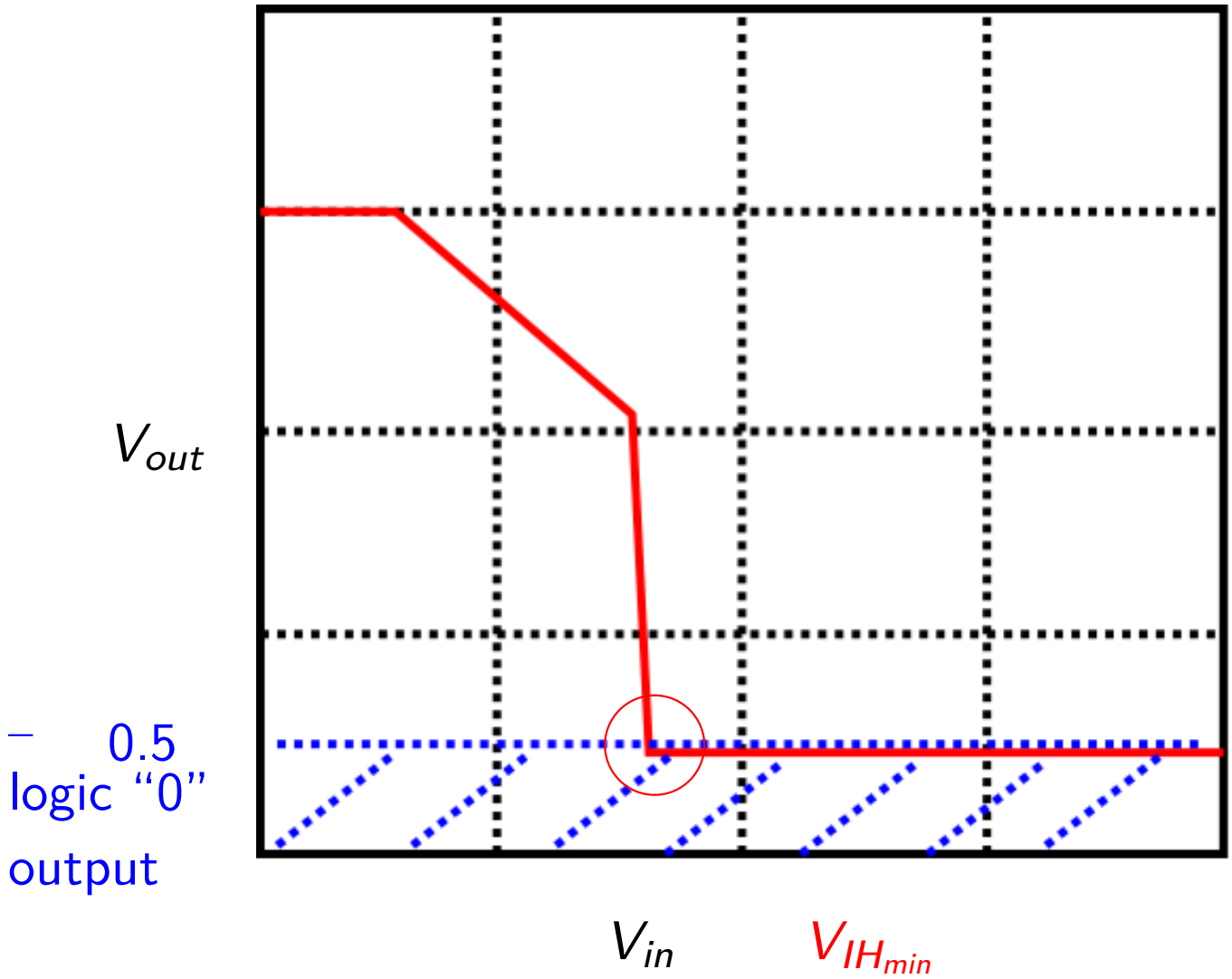

V_{out}
0.8
logic "0" input
V_{in}


$V_{OH_{min}}$
V_{out}
0.8
logic "0" input
V_{in}

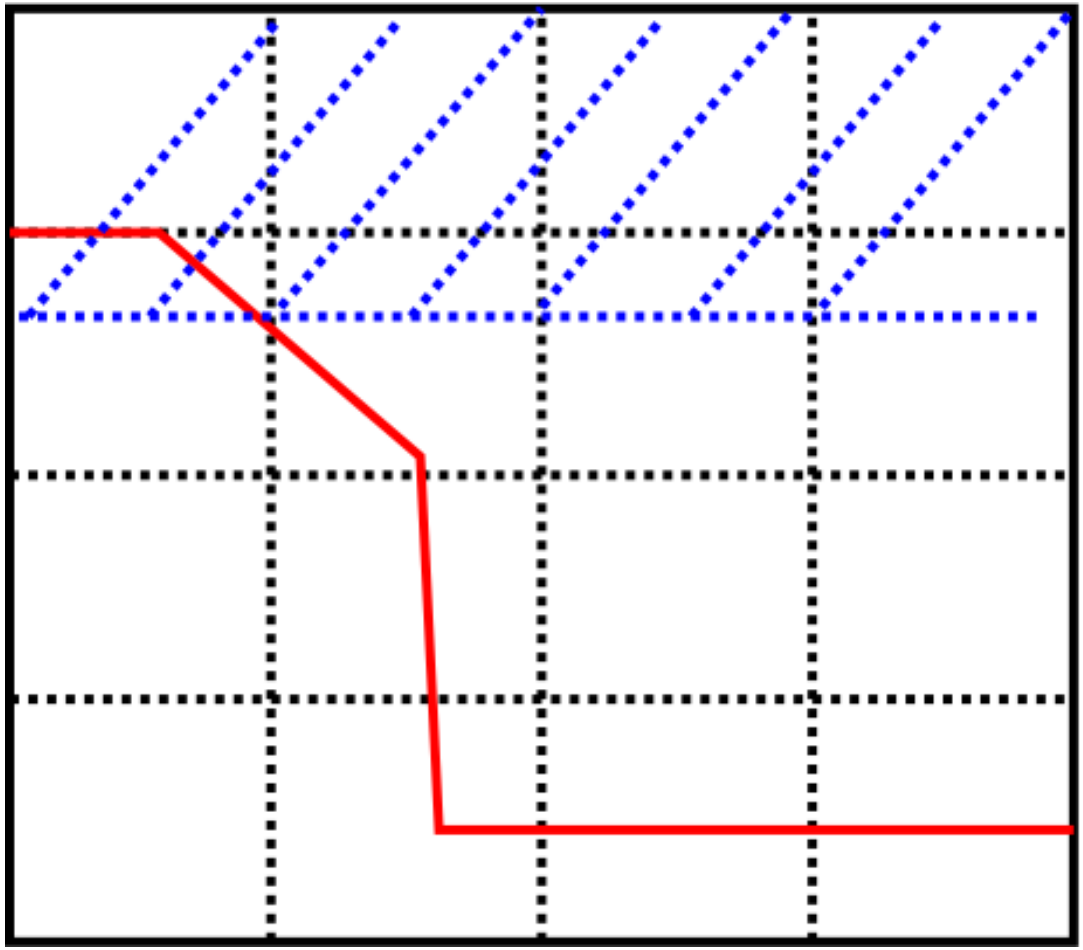

V_{out}
2.0
V_{in}
logic "1" input


V_{out}
$V_{OL_{max}}$
2.0
V_{in}
logic "1" input


V_{out}
0.5
logic "0"
output
V_{in}


V_{out}
0.5
logic "0"
output
V_{in}
$V_{IH_{min}}$

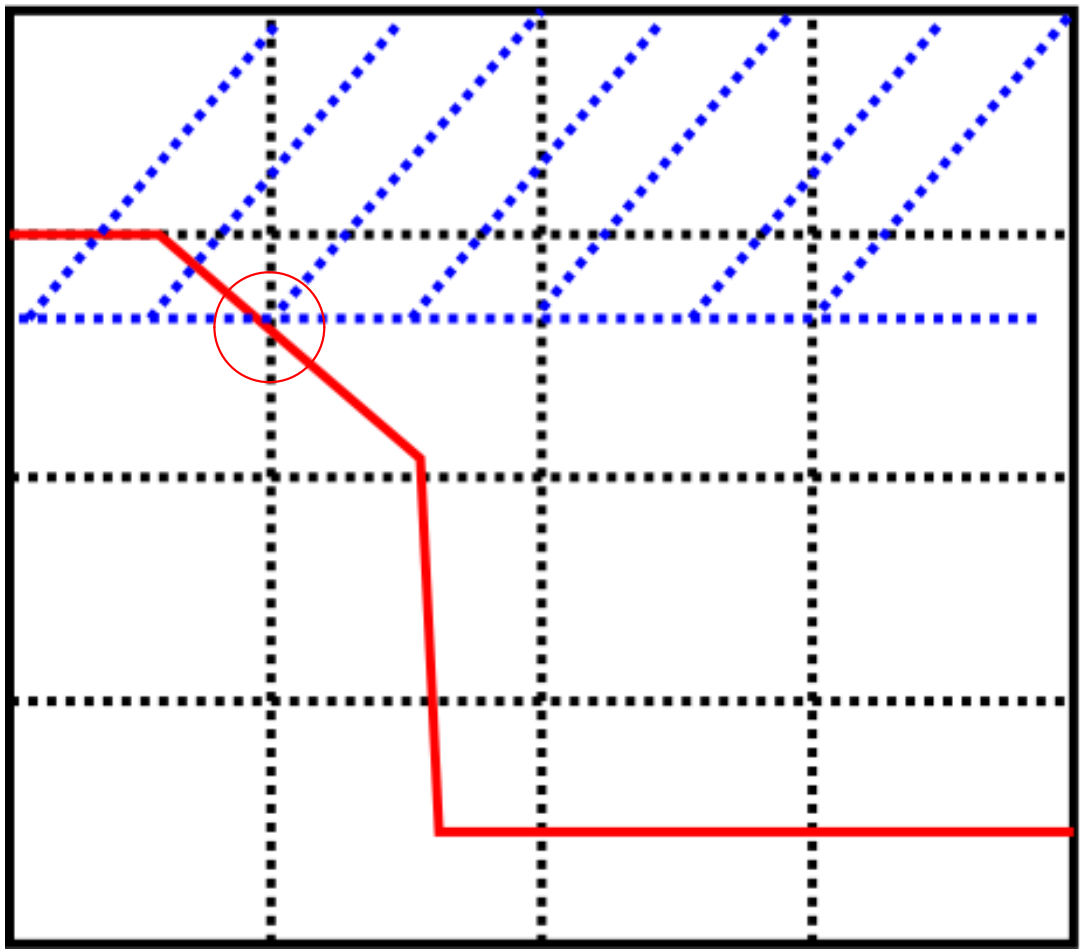
logic "1" output – 2.7



V_{out}

V_{in}

logic "1" output – 2.7

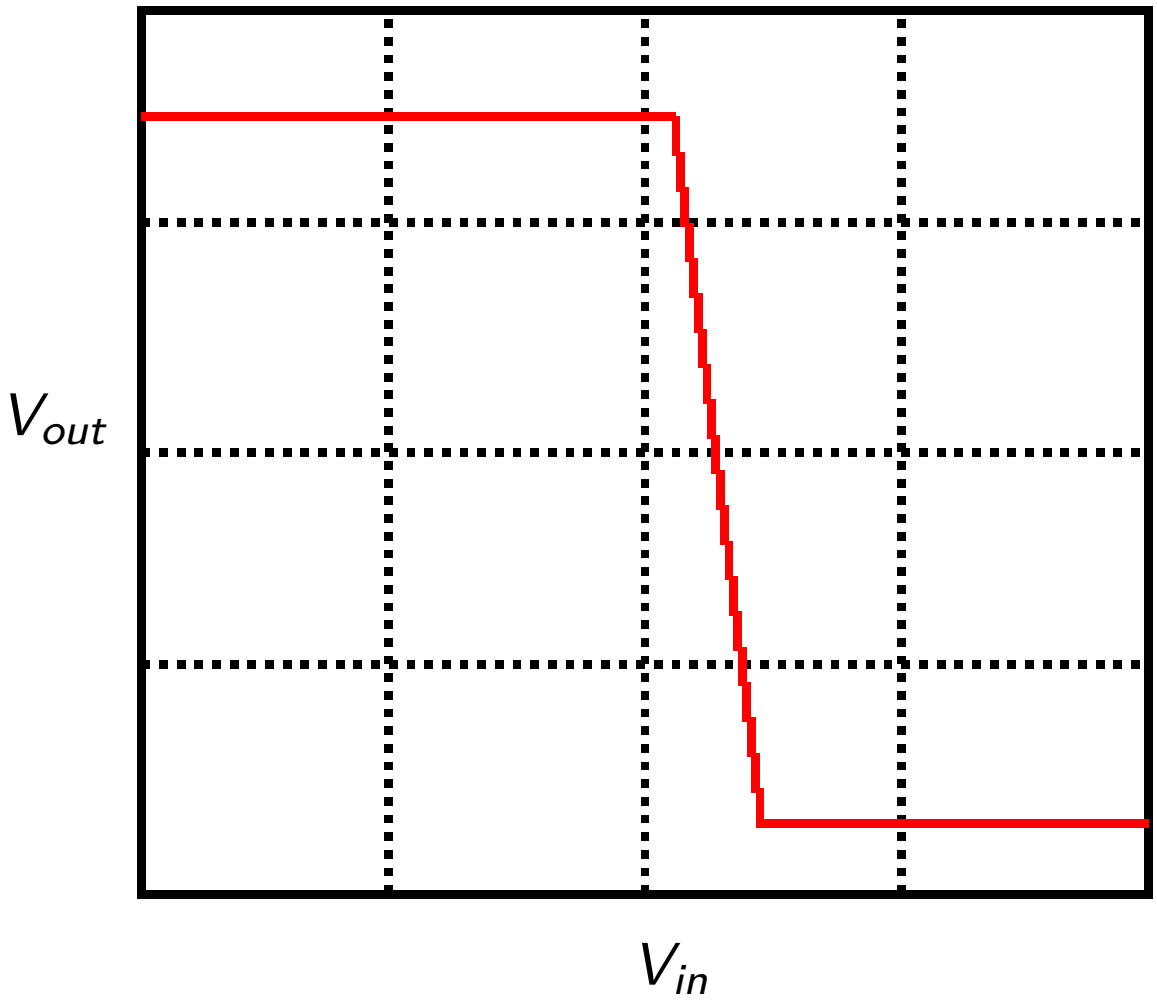


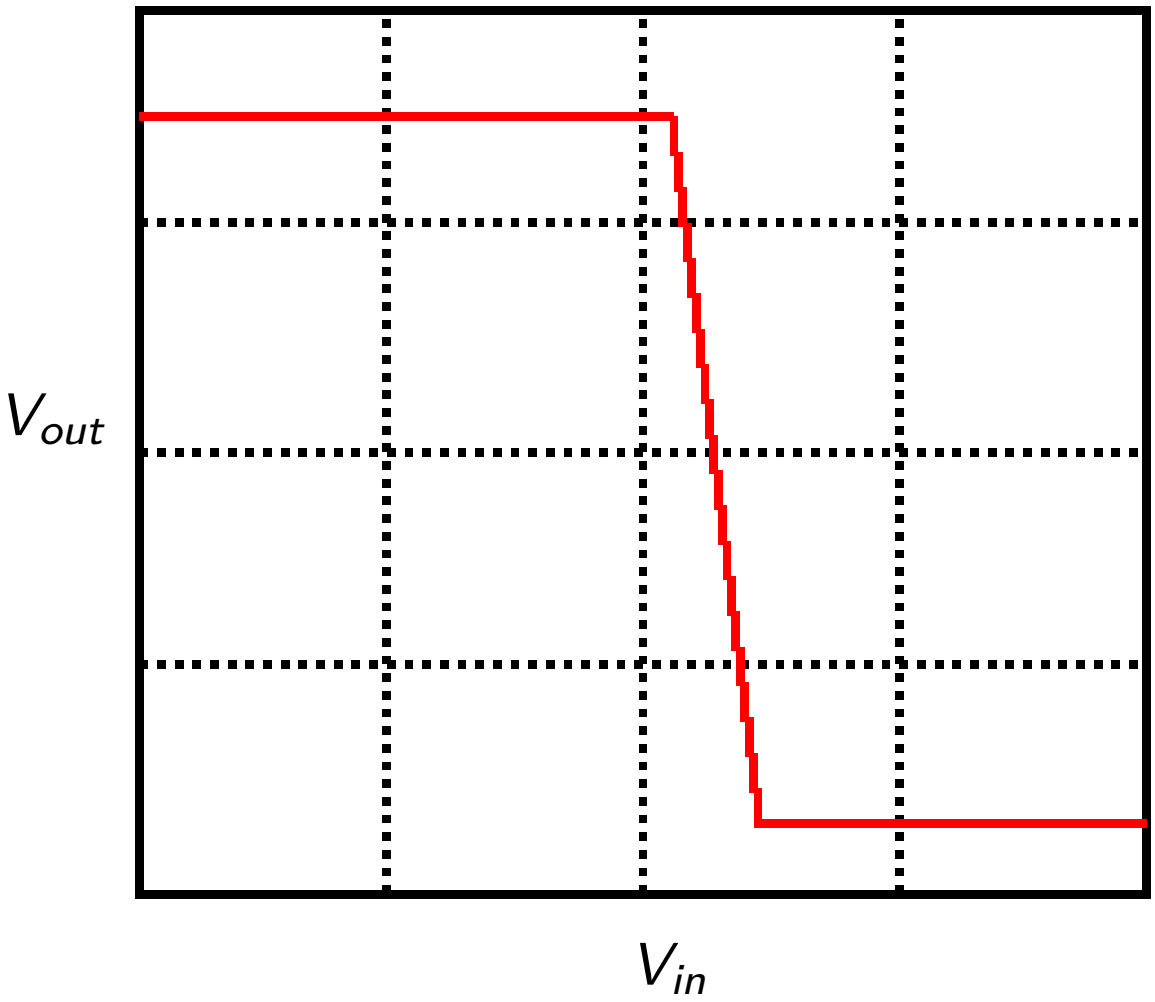
V_{out}

$V_{IL_{max}}$ V_{in}

This is called the **transfer characteristic** of the gate.

This is called the **transfer characteristic** of the gate.
Note that the input voltage, $\mathrm{V_{in}}$, is on the X axis and the output voltage, $\mathrm{V_{out}}$, on the Y axis.


V_{out}
V_{in}



CMOS will look slightly different.

Measuring Output Voltage Limits

Measuring Output Voltage Limits

- The output voltage produced by an input voltage of the specified value of $\mathrm{V_{IL_{max}}}$ would be the *measured* value of $\mathrm{V_{OH_{min}}}$.

Measuring Output Voltage Limits

- The output voltage produced by an input voltage of the specified value of $\mathrm{V_{IL_{max}}}$ would be the *measured* value of $\mathrm{V_{OH_{min}}}$.
- The output voltage is produced by an input voltage of the specified value of $\mathrm{V_{IH_{min}}}$ would be the *measured* value of $\mathrm{V_{OL_{max}}}$.

Measuring Output Voltage Limits

- The output voltage produced by an input voltage of the specified value of $\mathrm{V_{IL_{max}}}$ would be the *measured* value of $\mathrm{V_{OH_{min}}}$.
- The output voltage is produced by an input voltage of the specified value of $\mathrm{V_{IH_{min}}}$ would be the *measured* value of $\mathrm{V_{OL_{max}}}$.