Electronics
Logic Gate Characteristics: Voltage

Terry Sturtevant

Wilfrid Laurier University

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Ideal logic gates

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- Now the real (i.e. non-ideal) operating characteristics of different logic families will be studied.
- The operation of an *ideal* logic gate can be summarized by the following rules:

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- Any change of an input will immediately be reflected on the output.

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- Changes made at the inputs will take a finite amount of time to be reflected on the outputs.
- Inputs must draw a small but finite amount of current from whatever is driving them in order that they will be recognized.
- Outputs have a limited current capacity for maintaining the output voltage at the desired level.

Real logic gates

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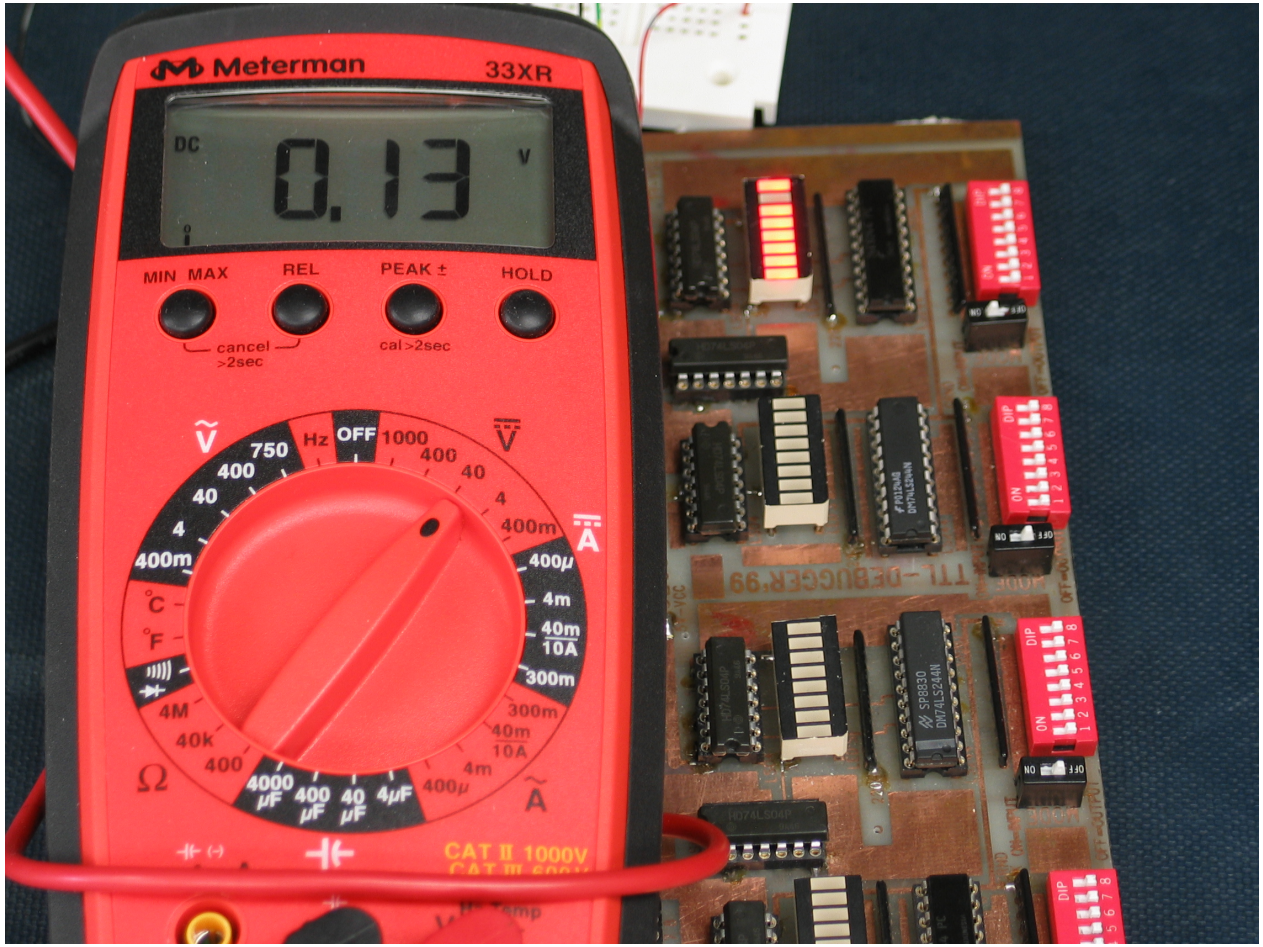

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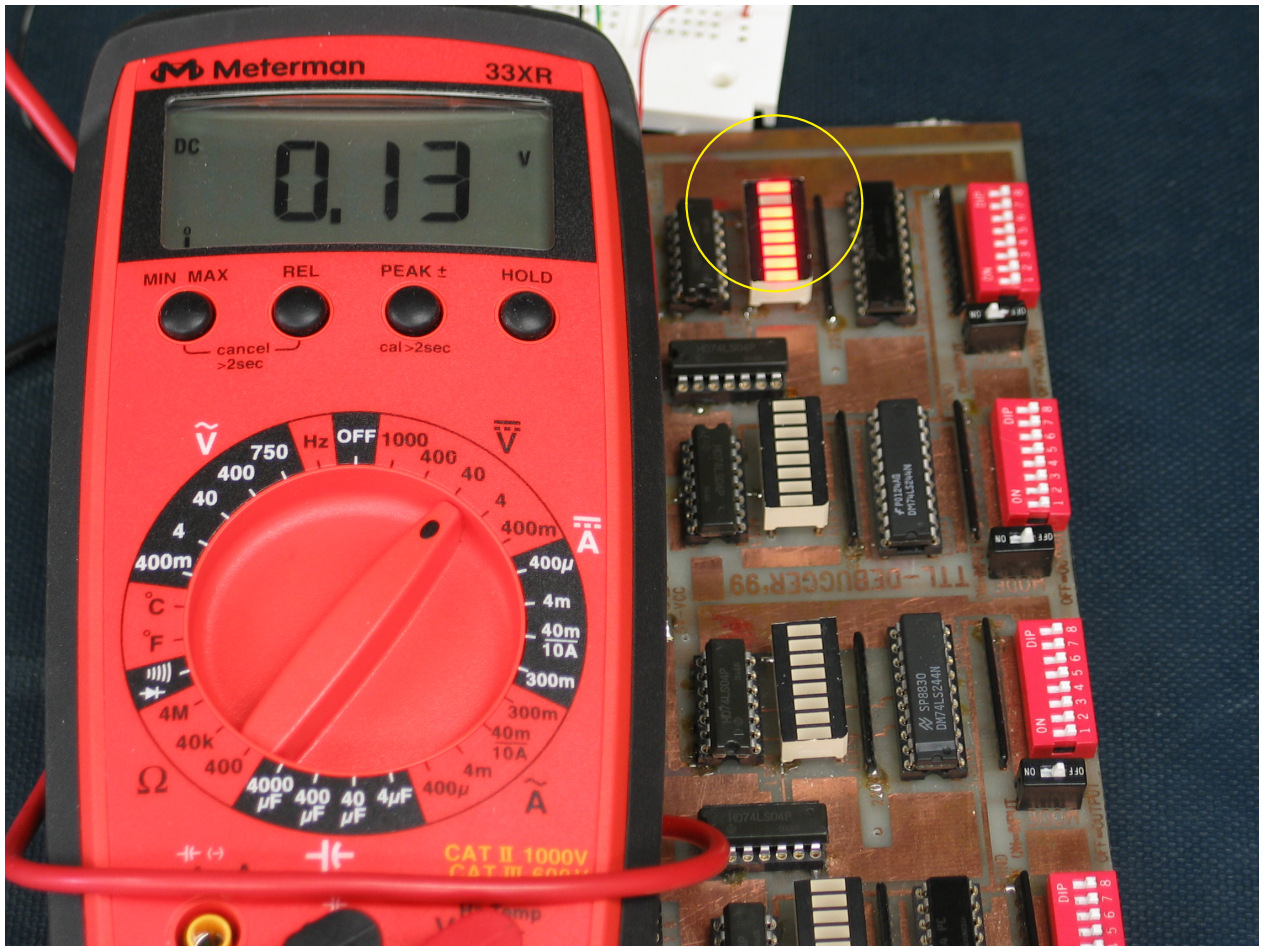

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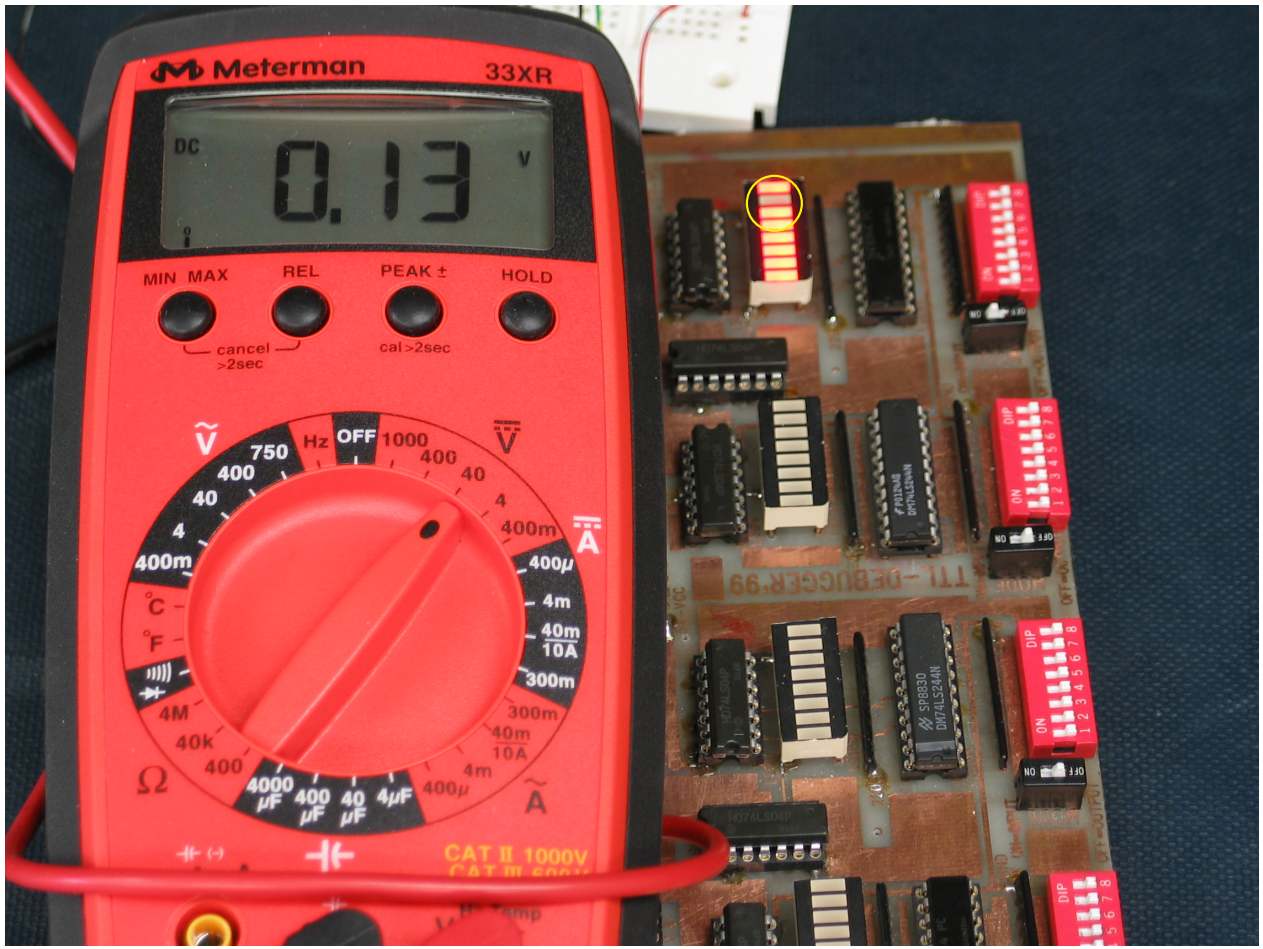

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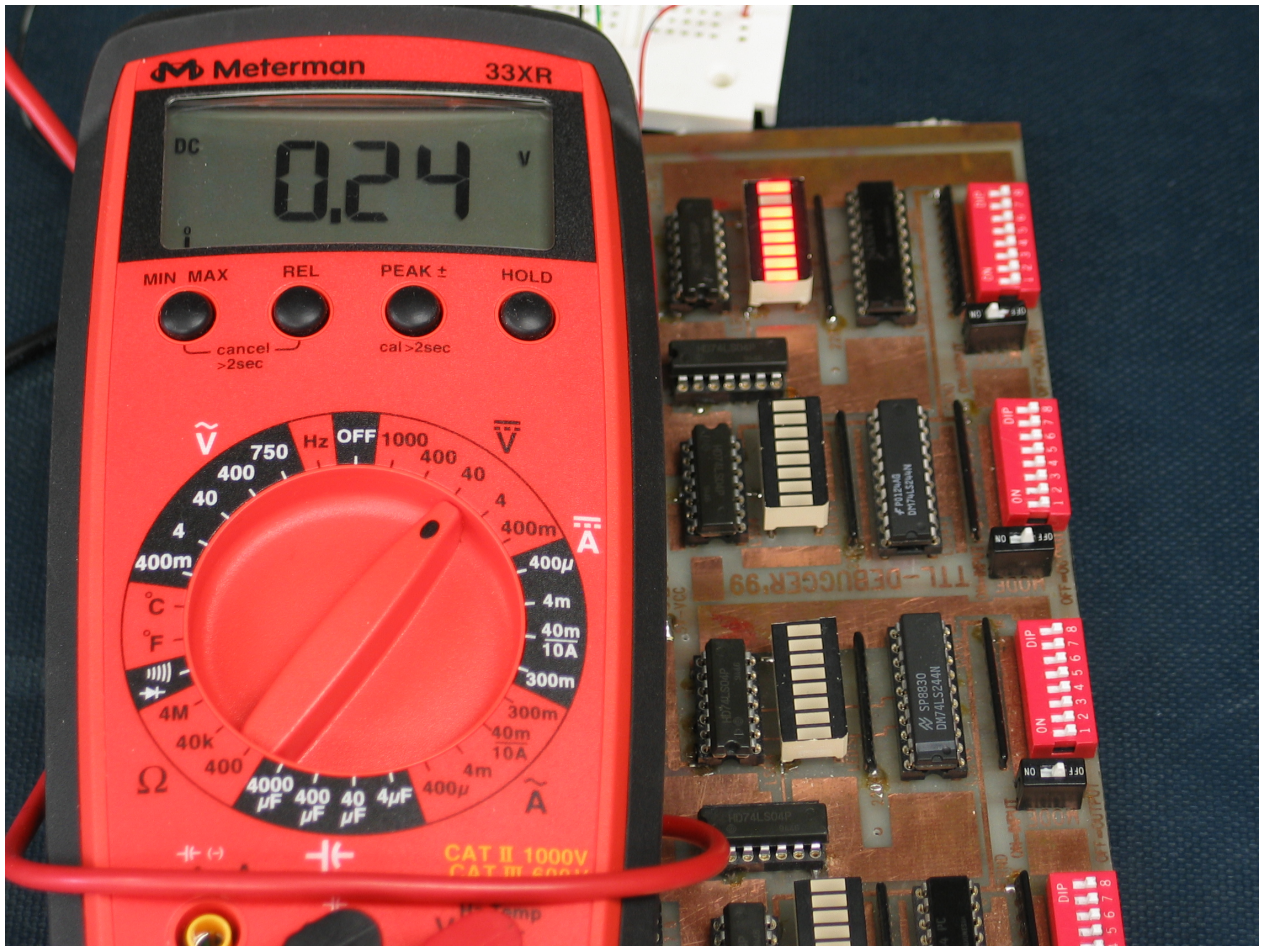

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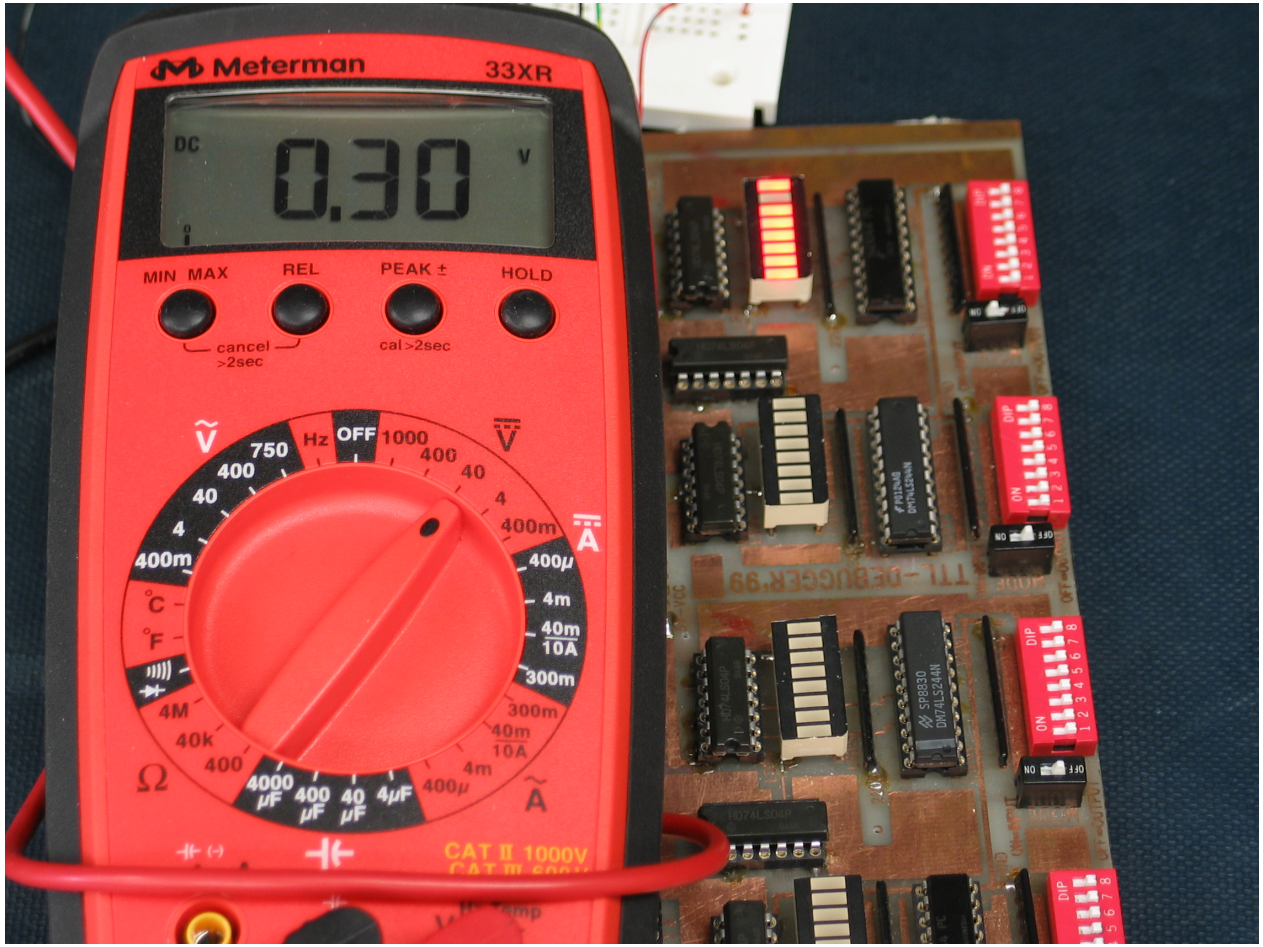

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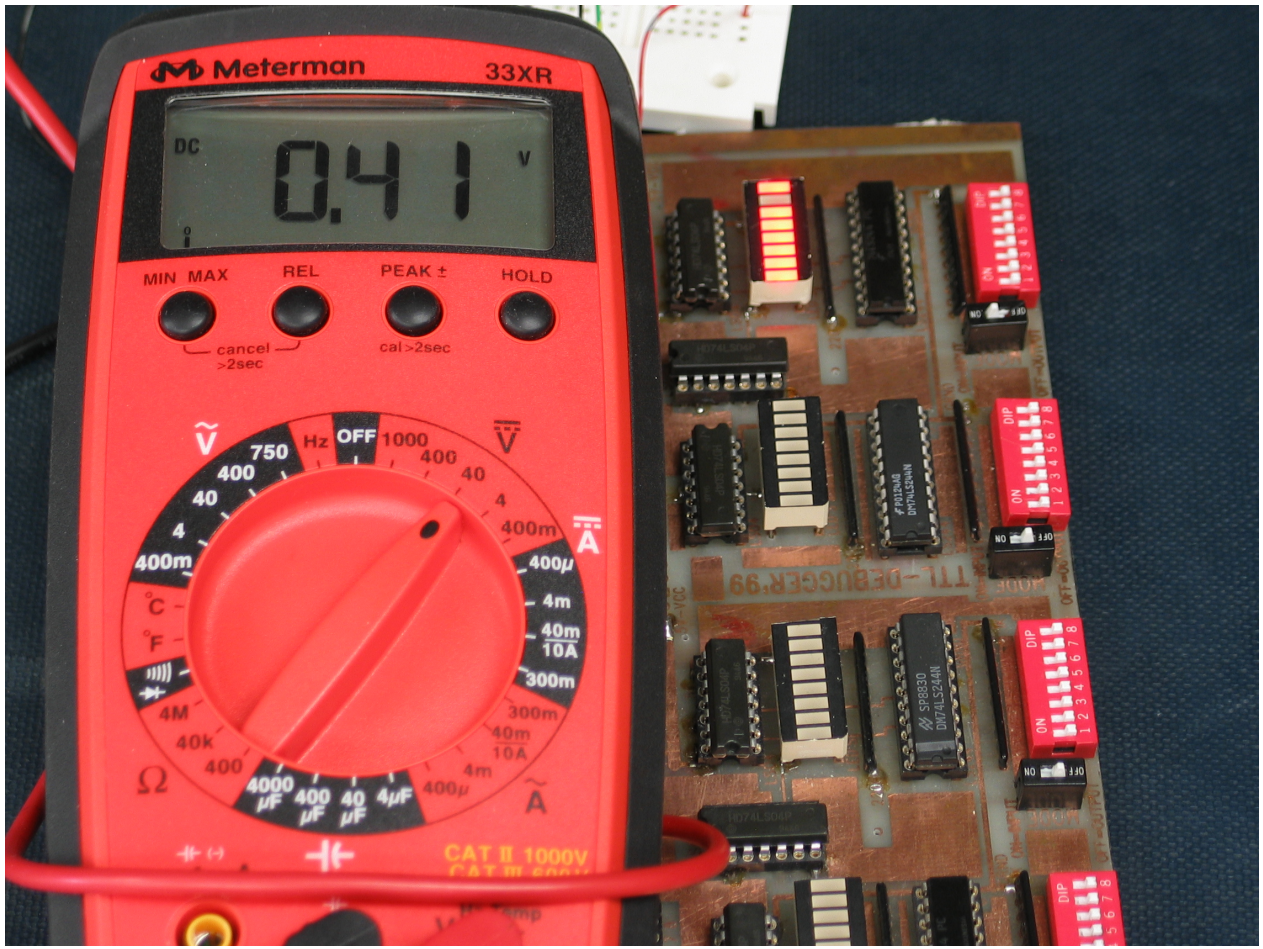

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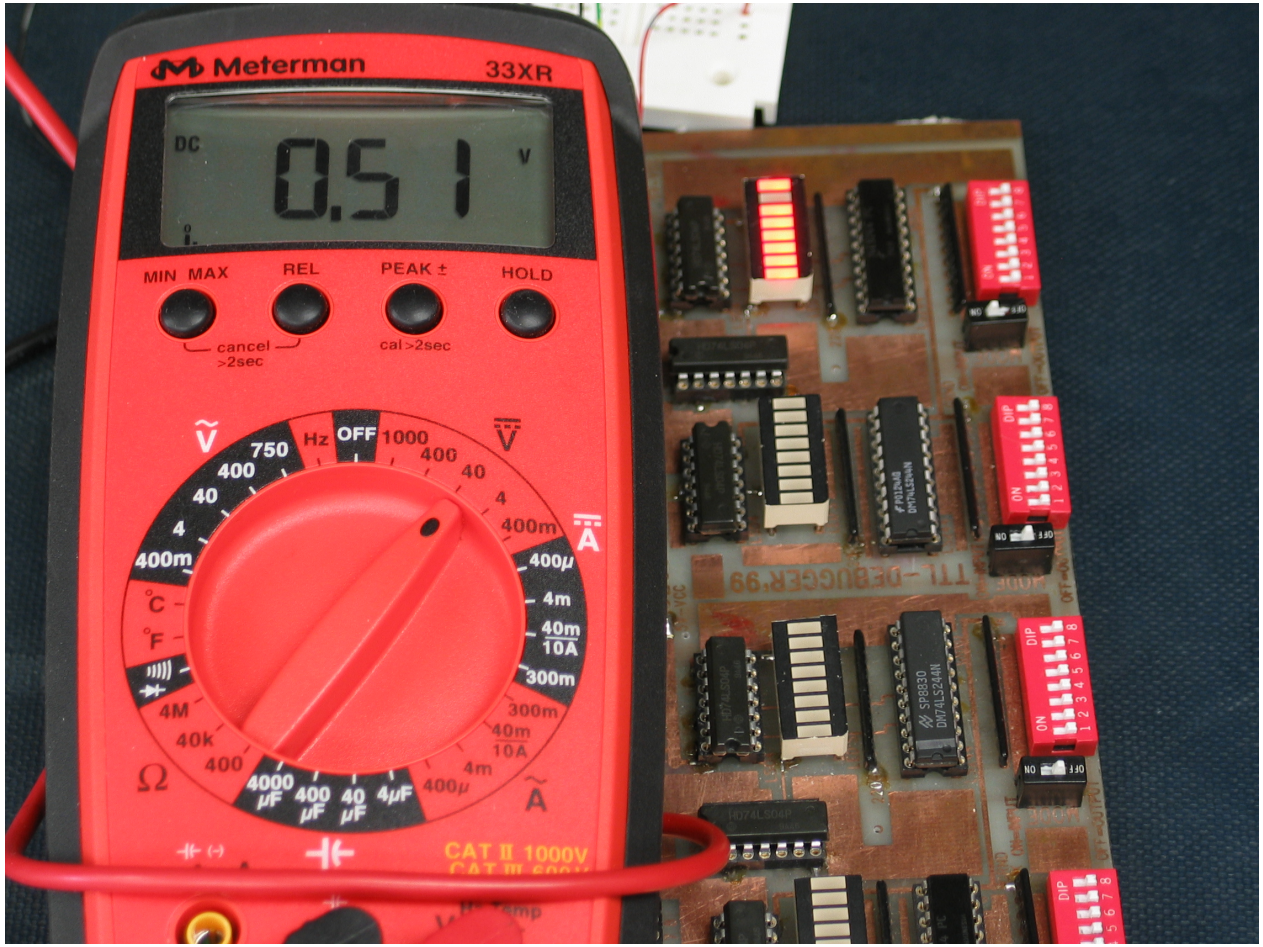

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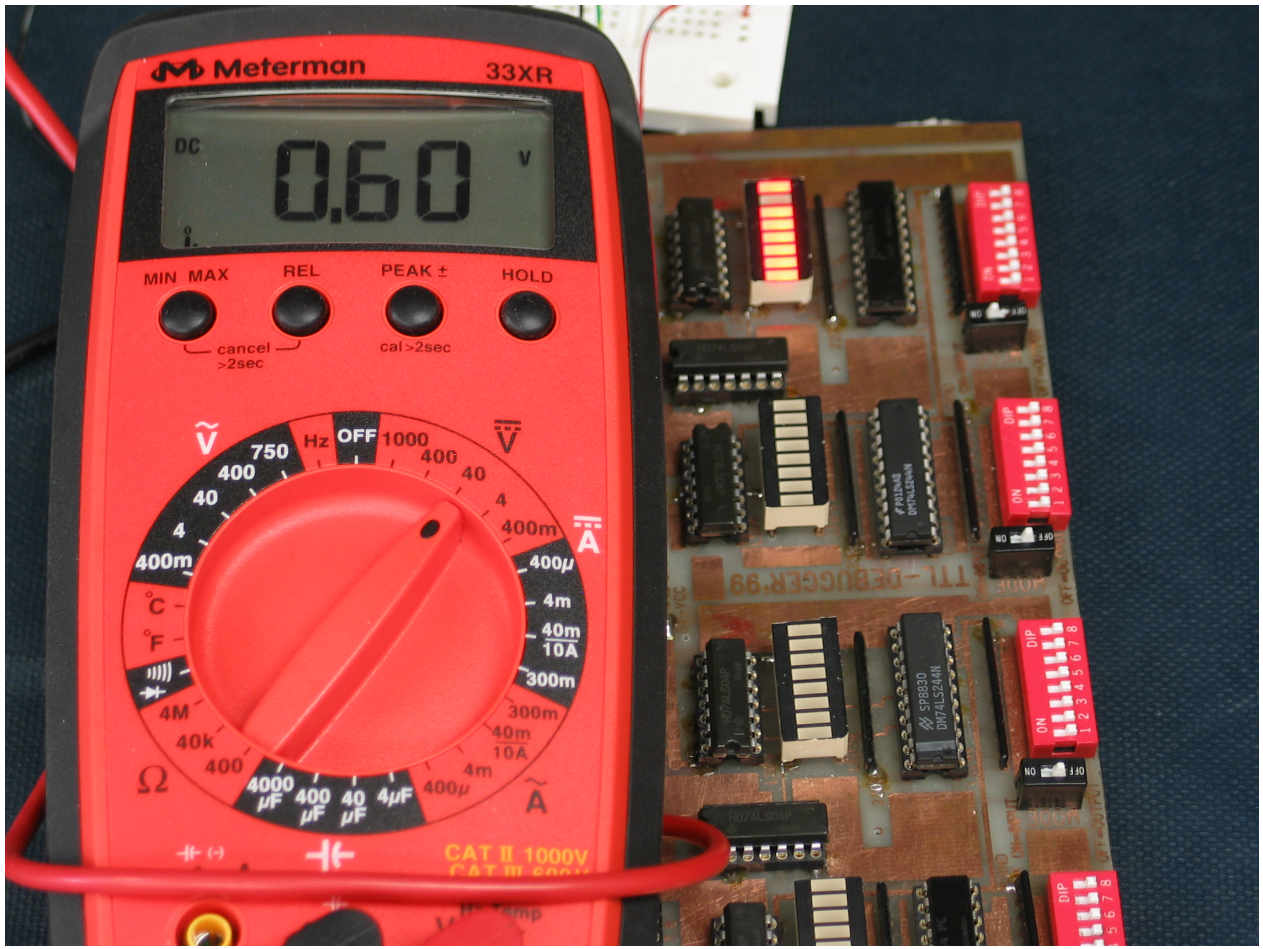

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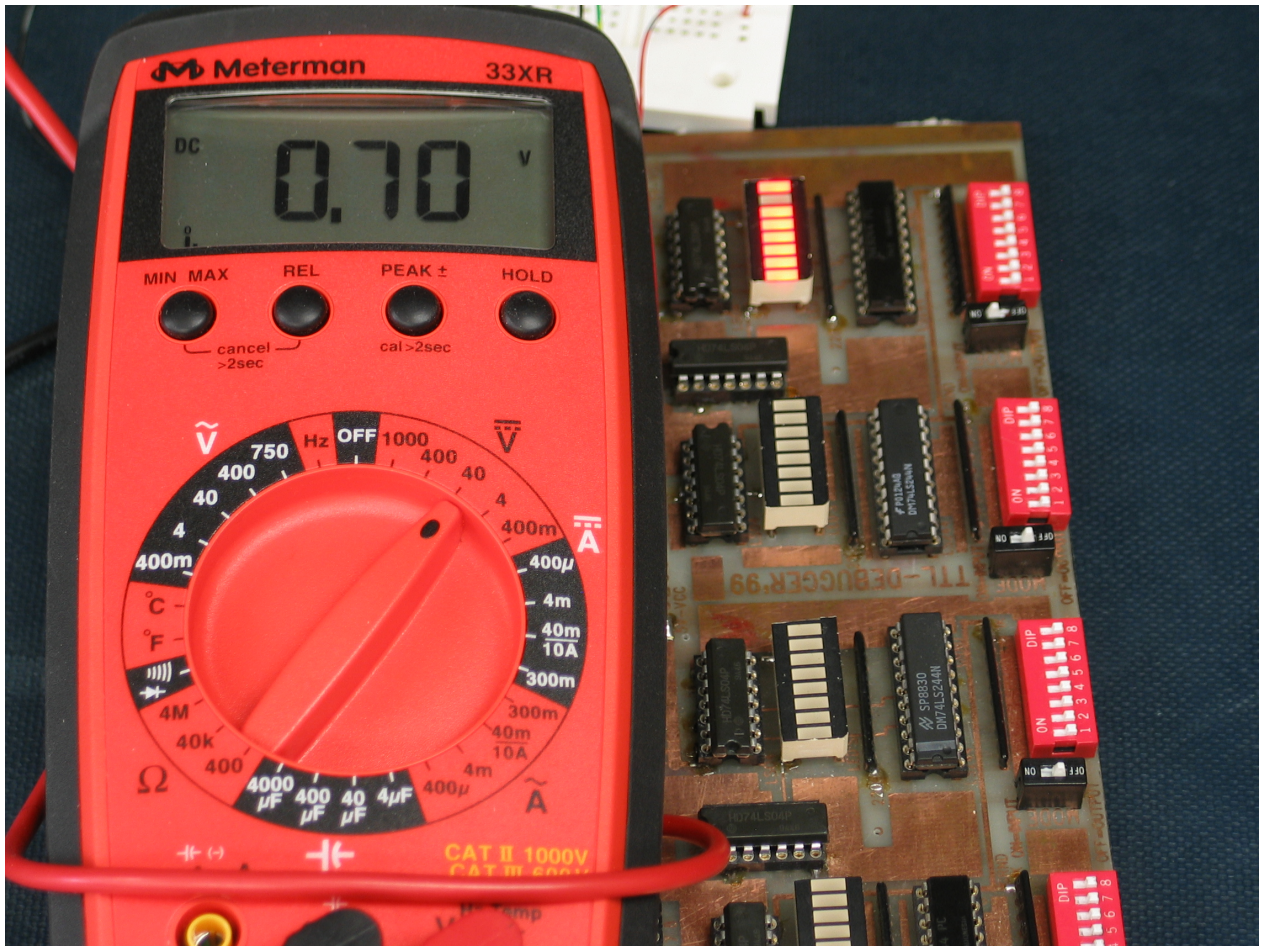

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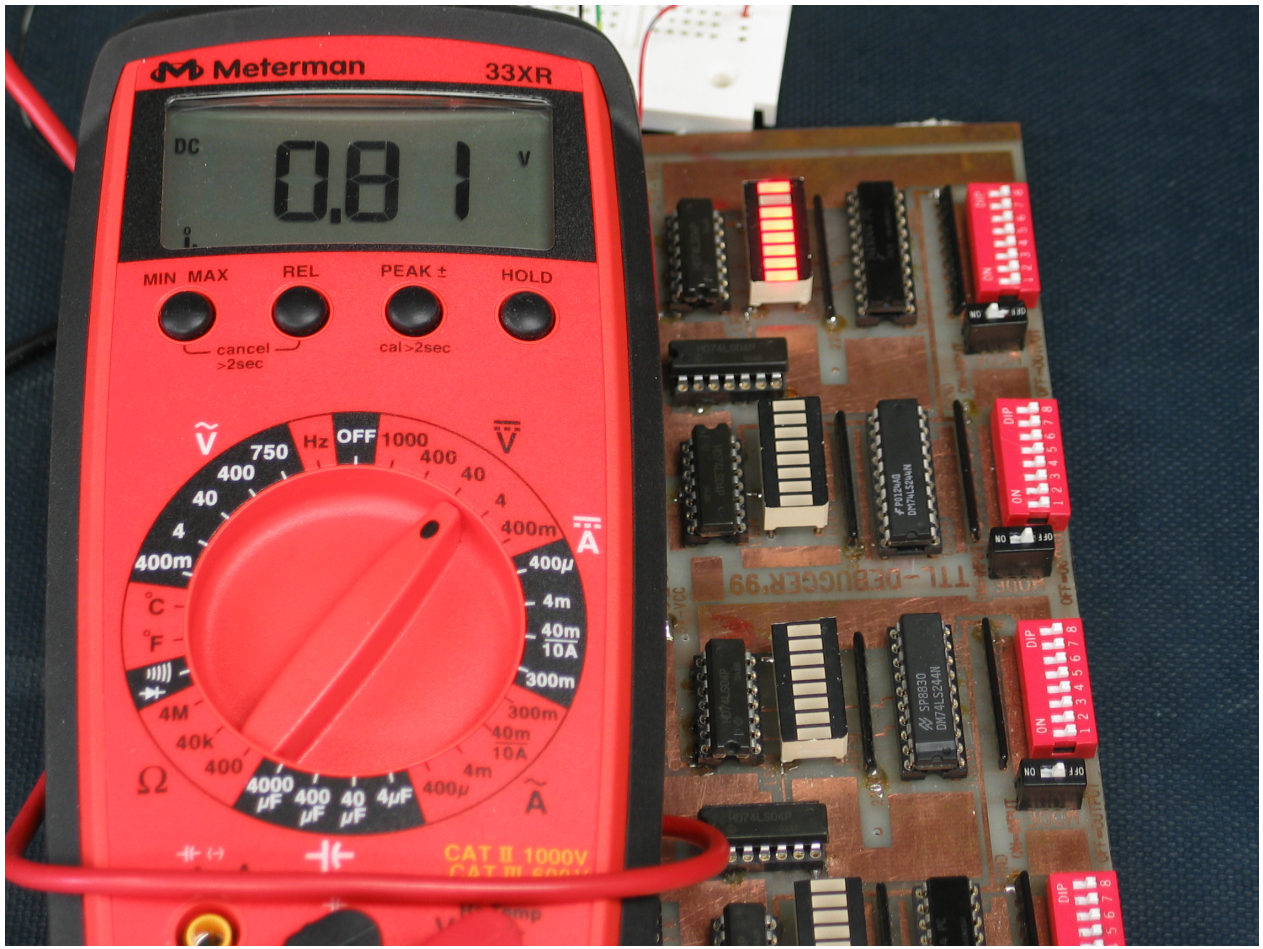

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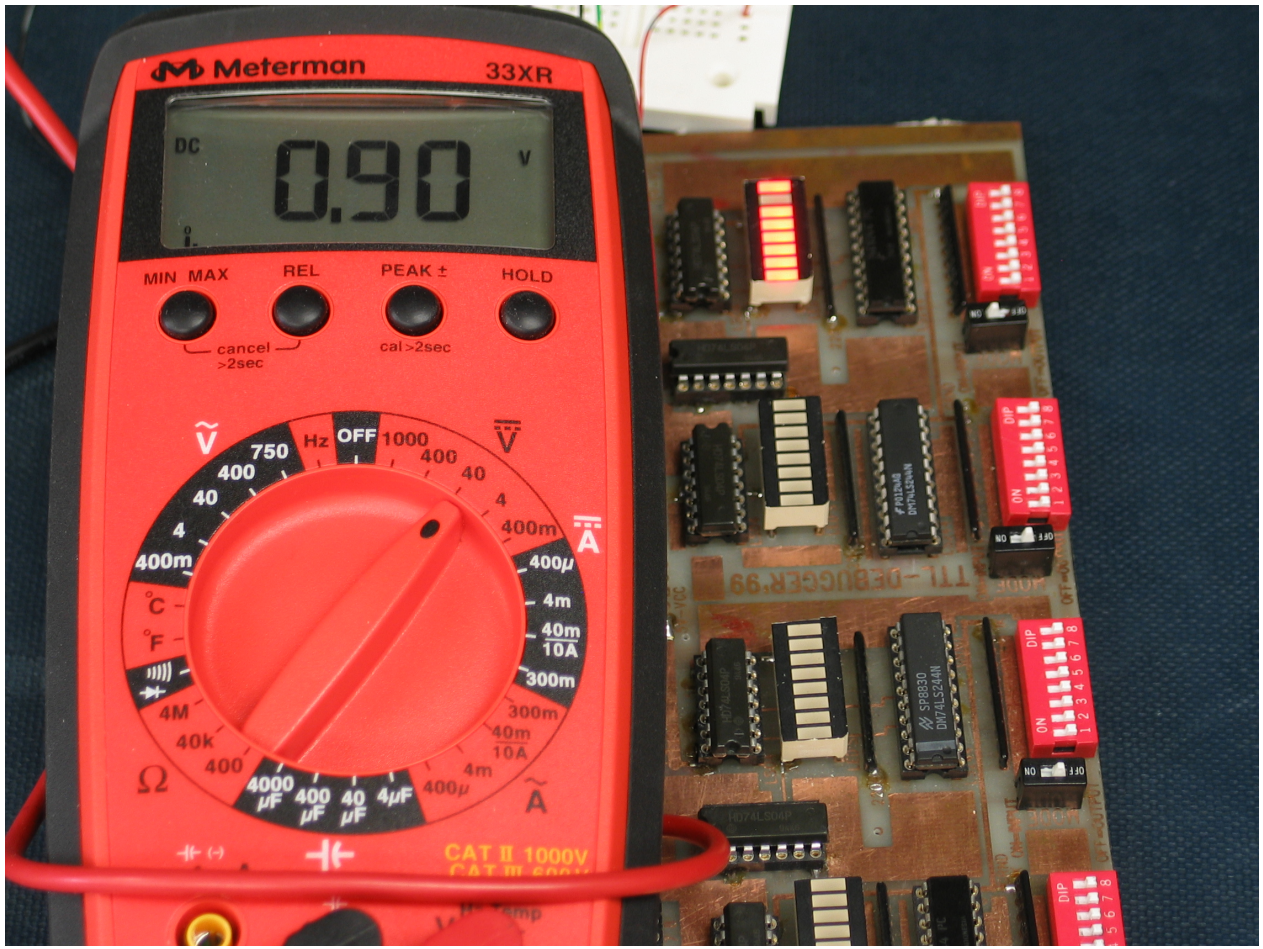

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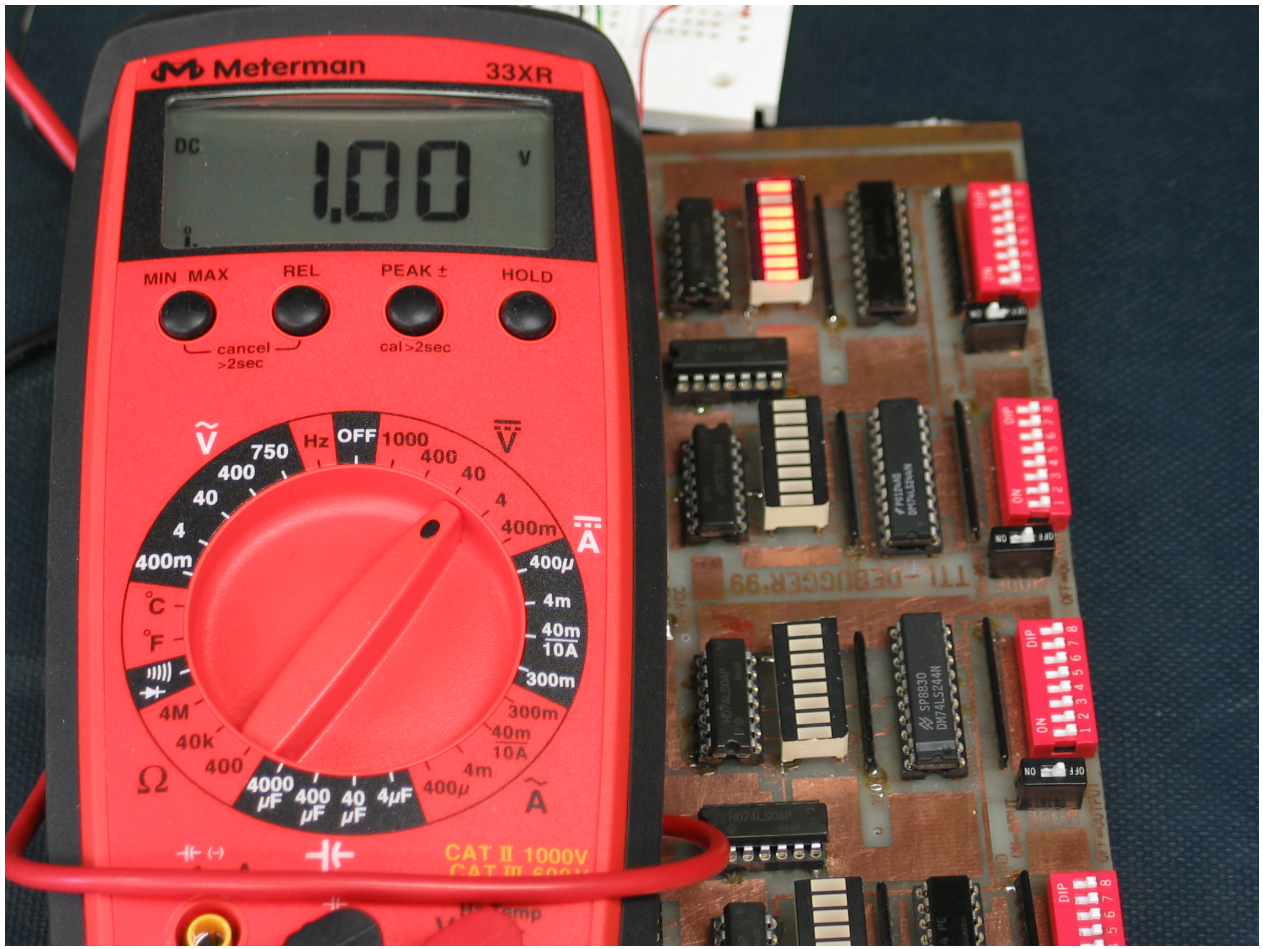

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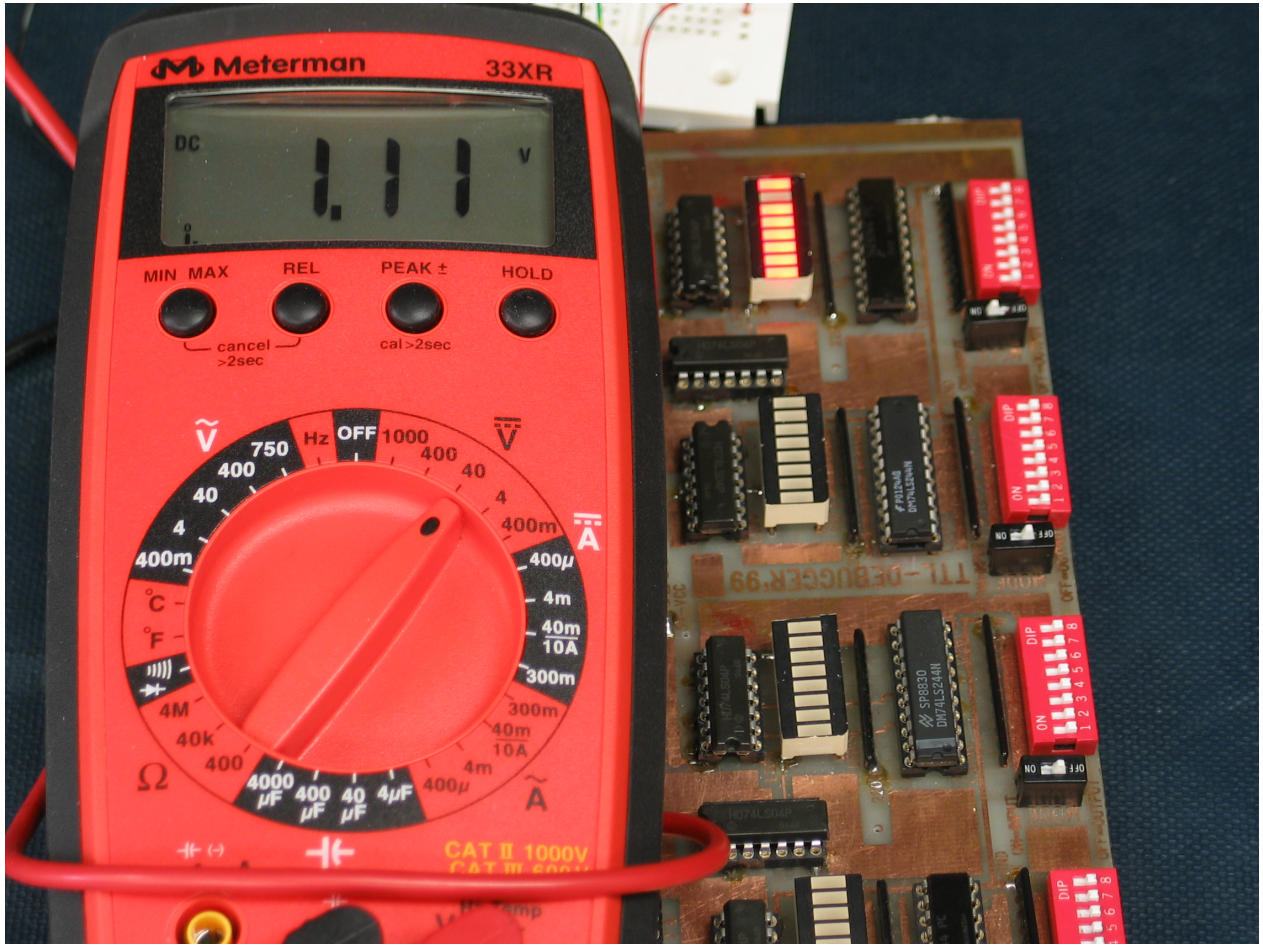

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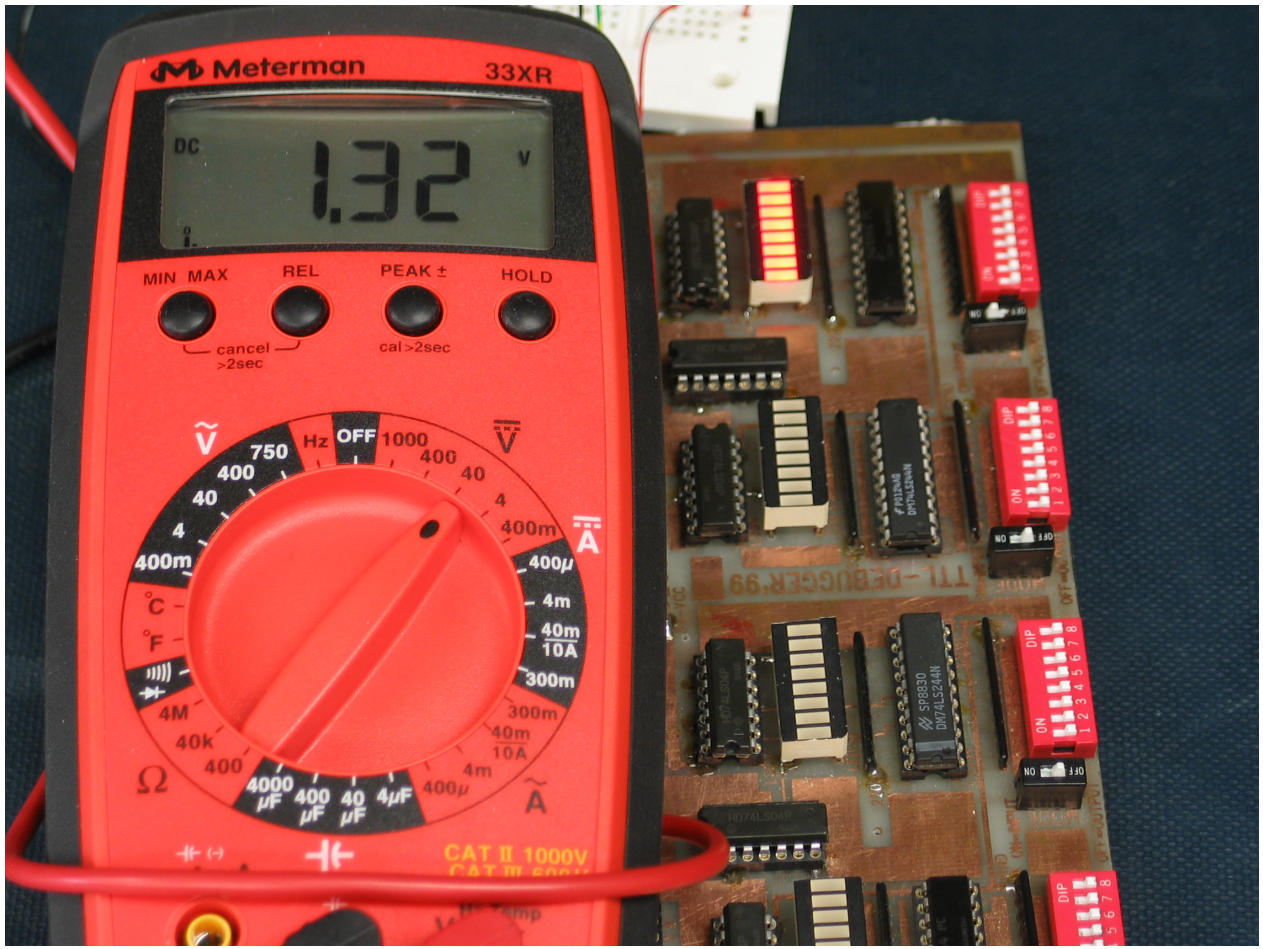

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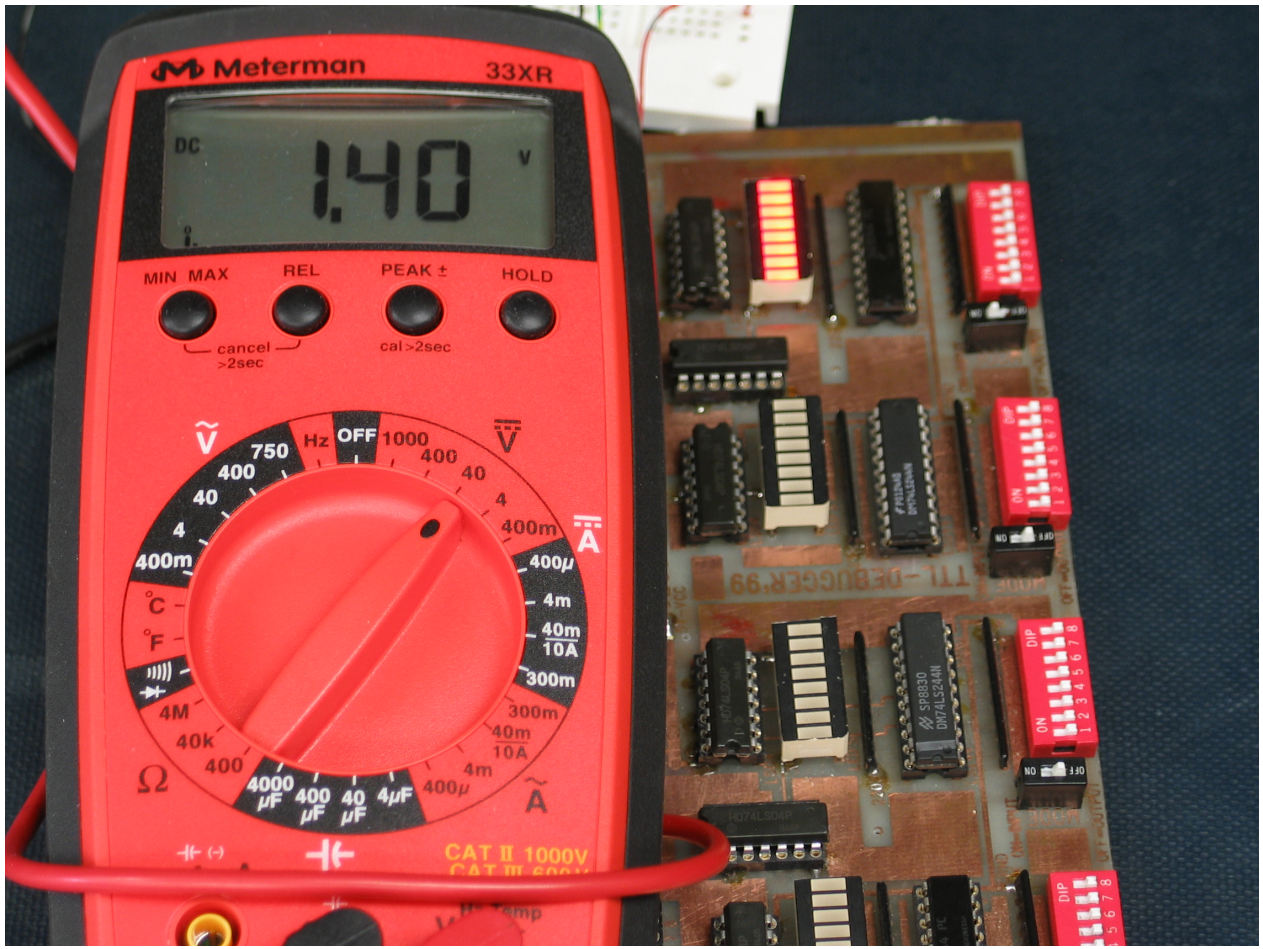

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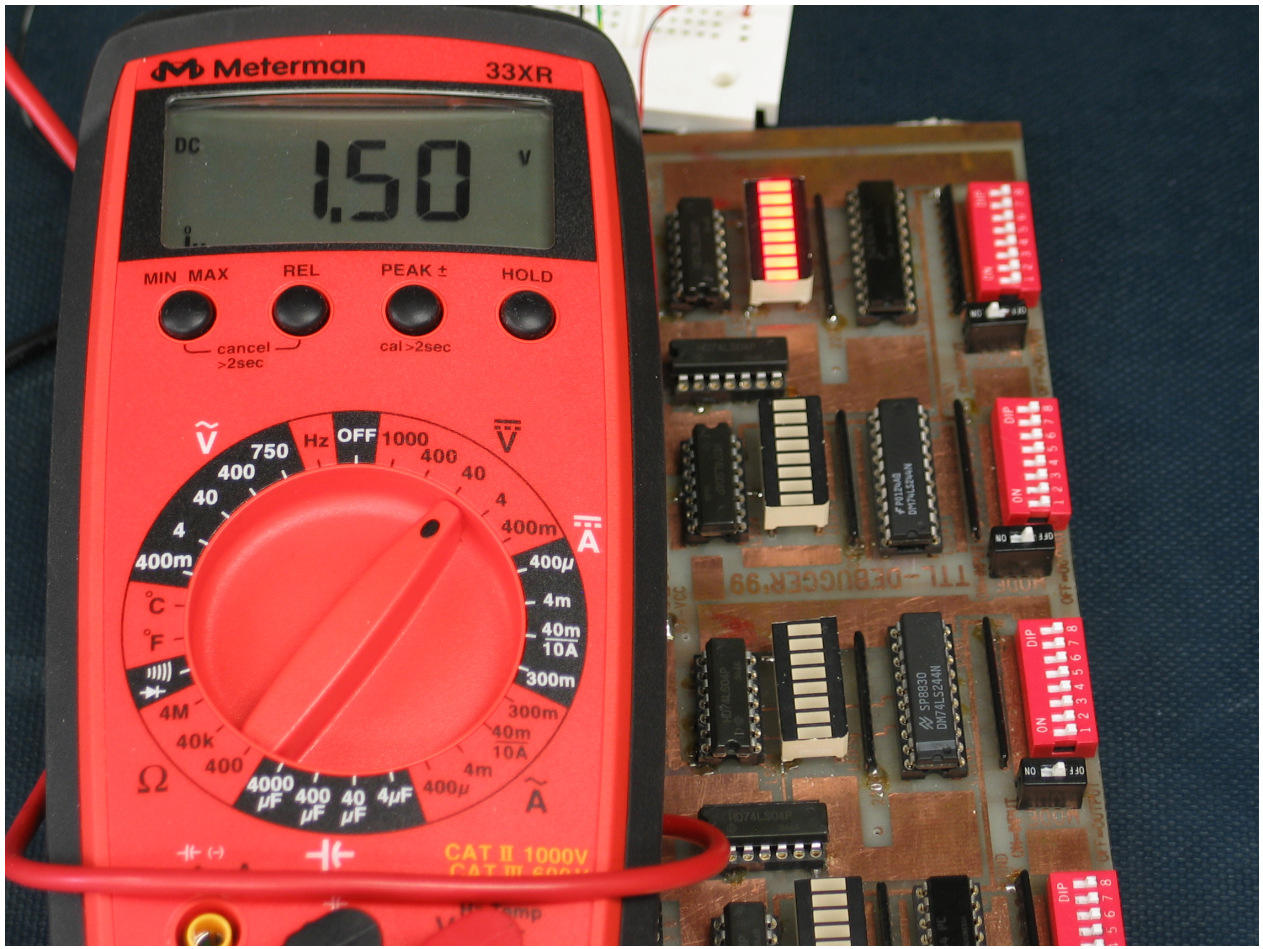

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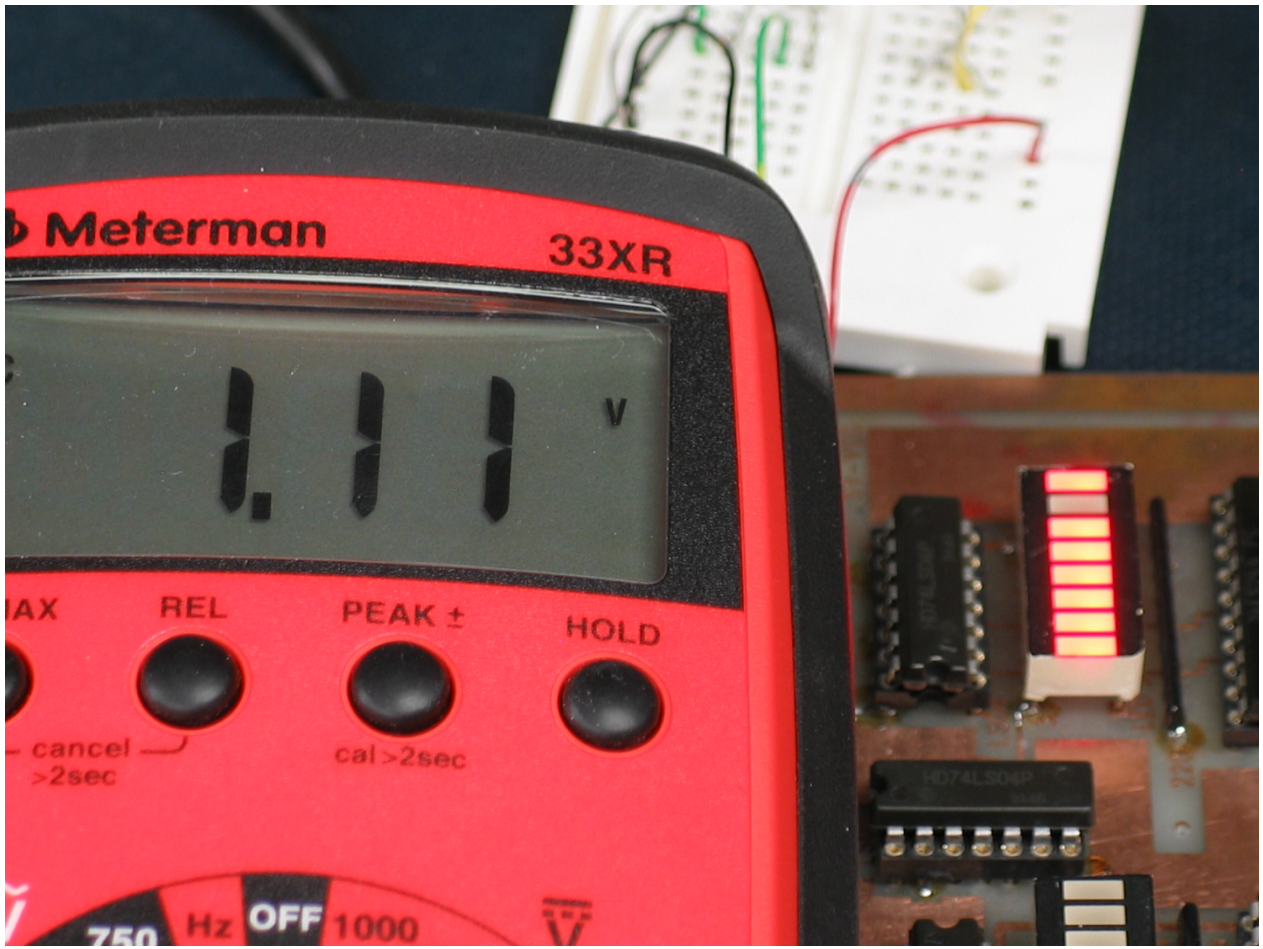
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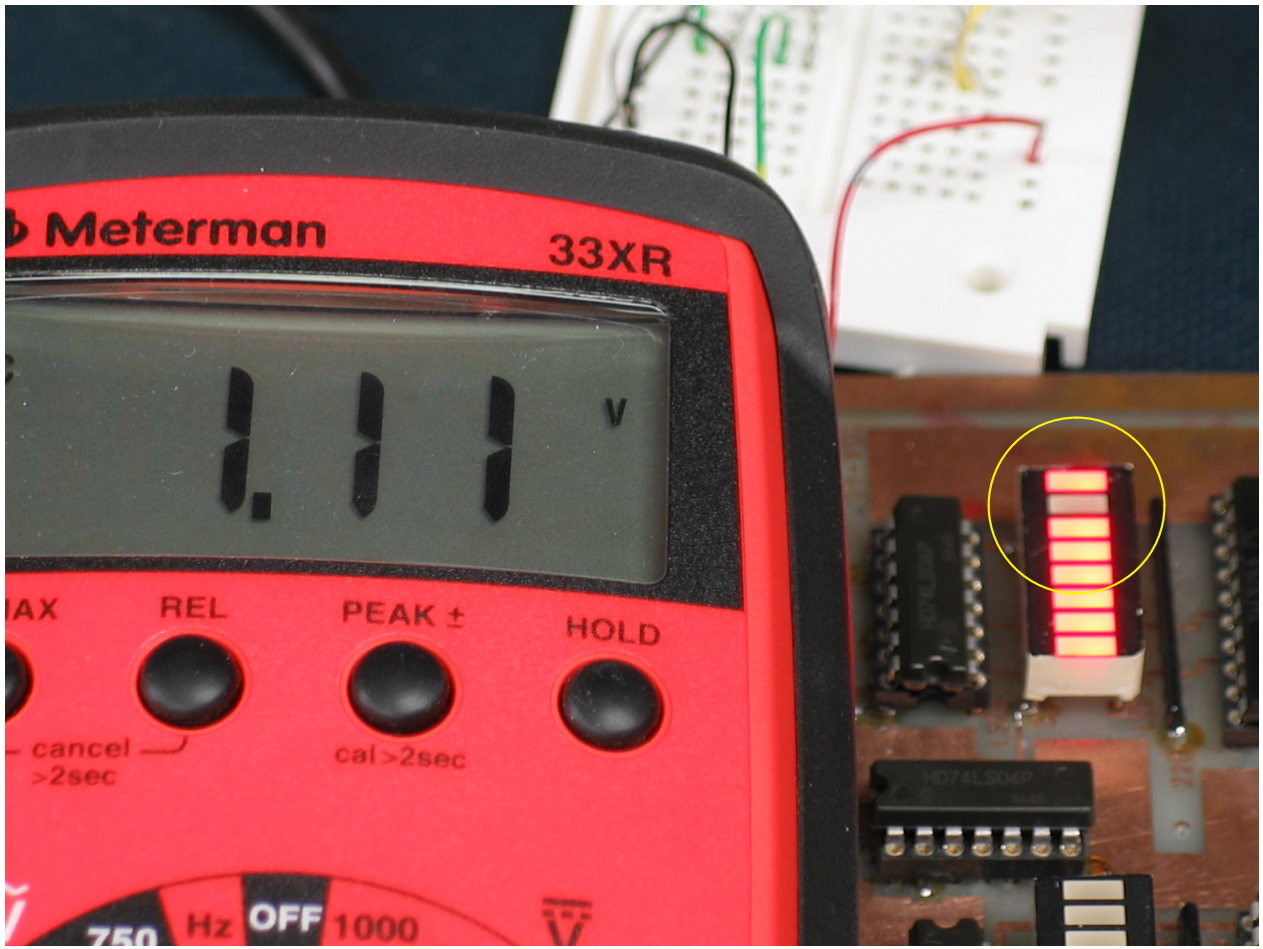
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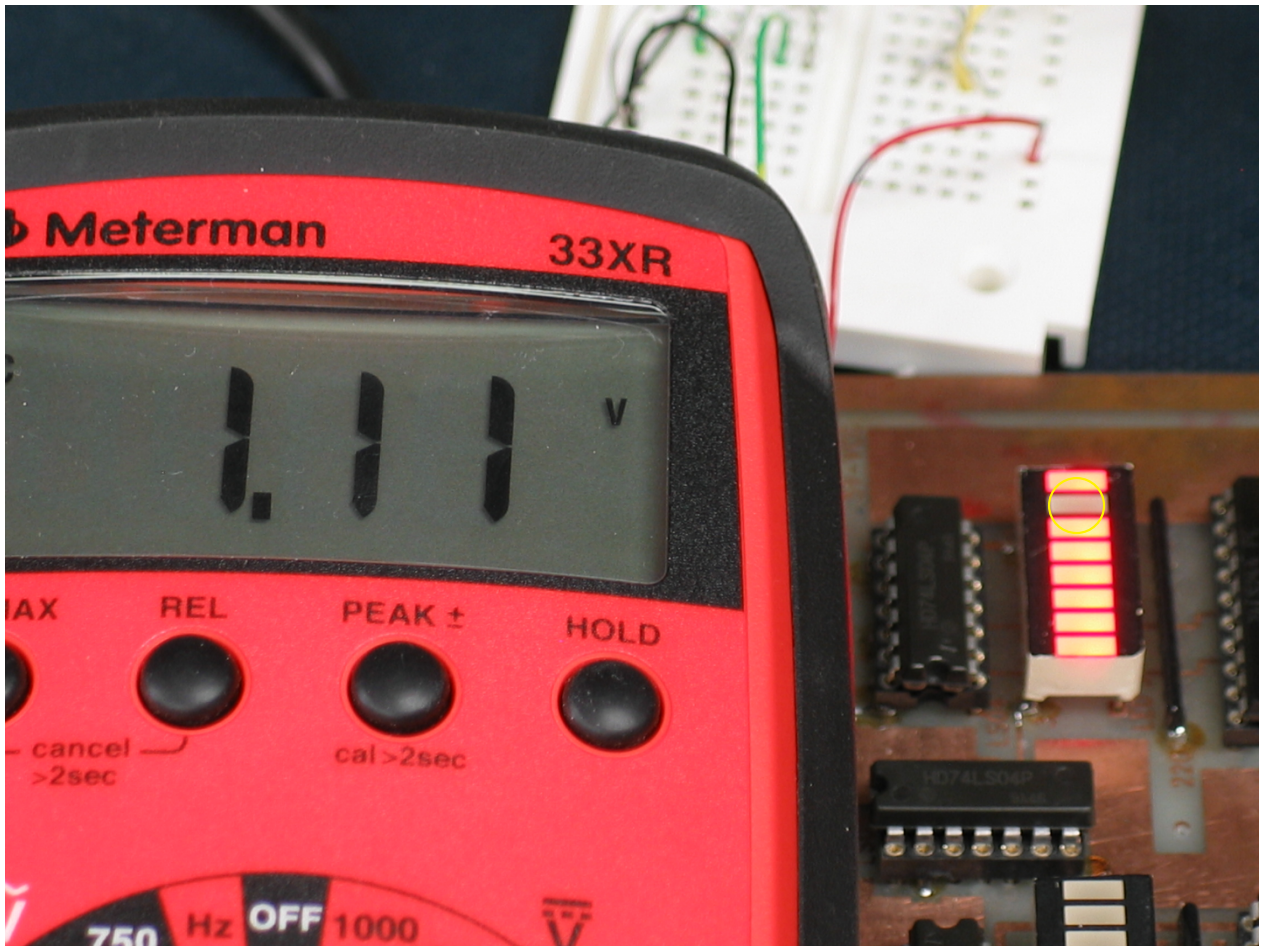
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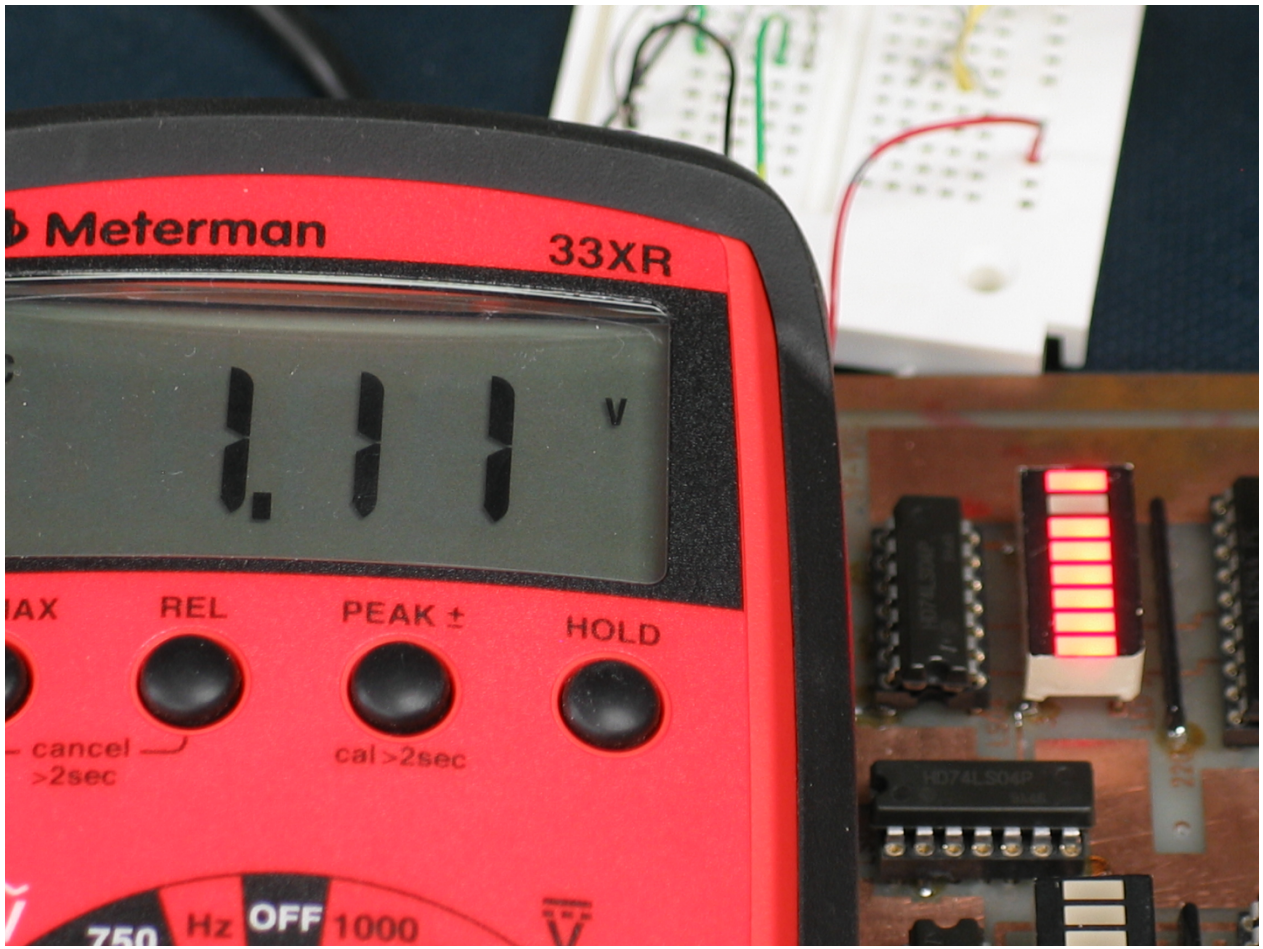
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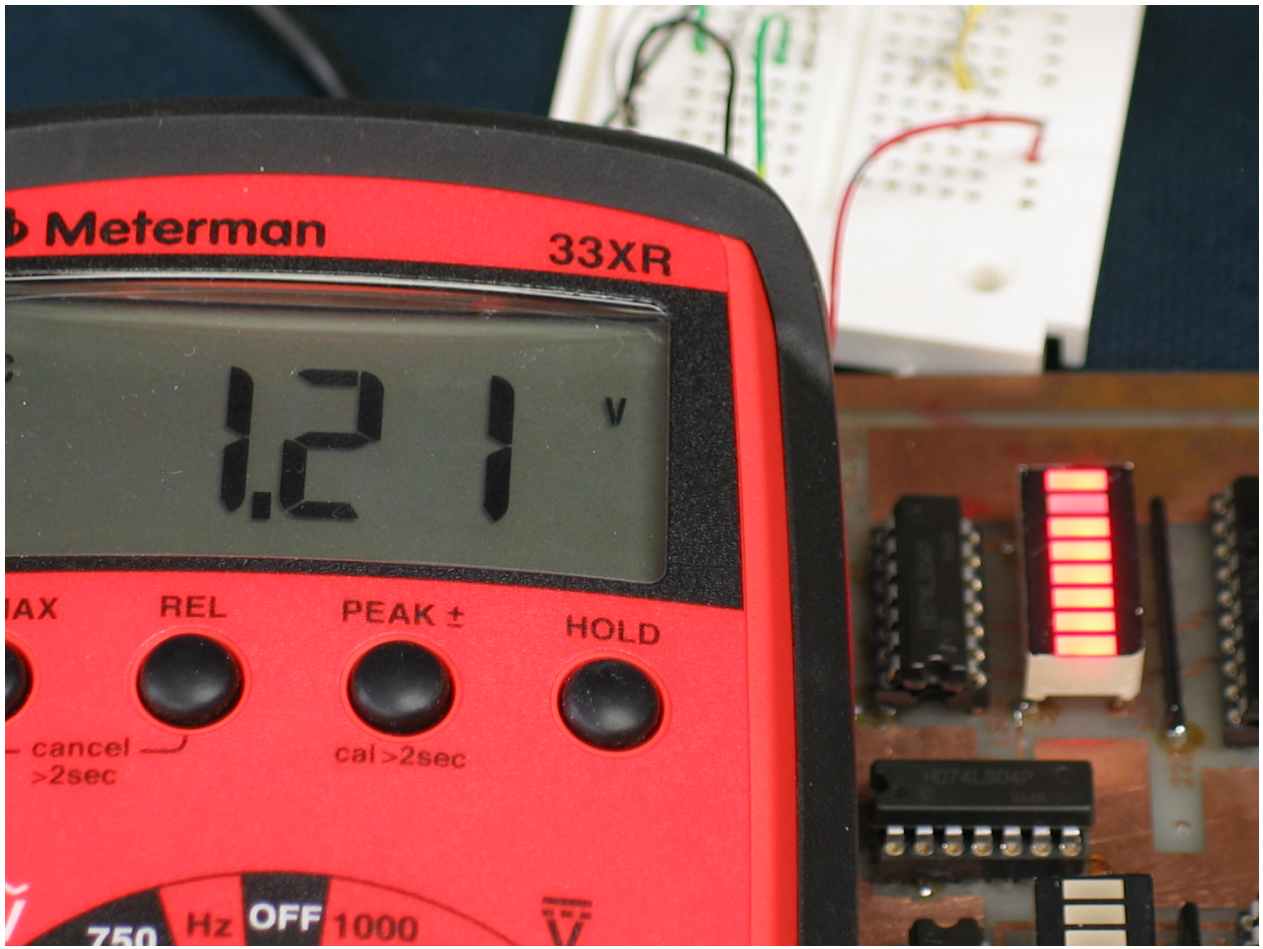
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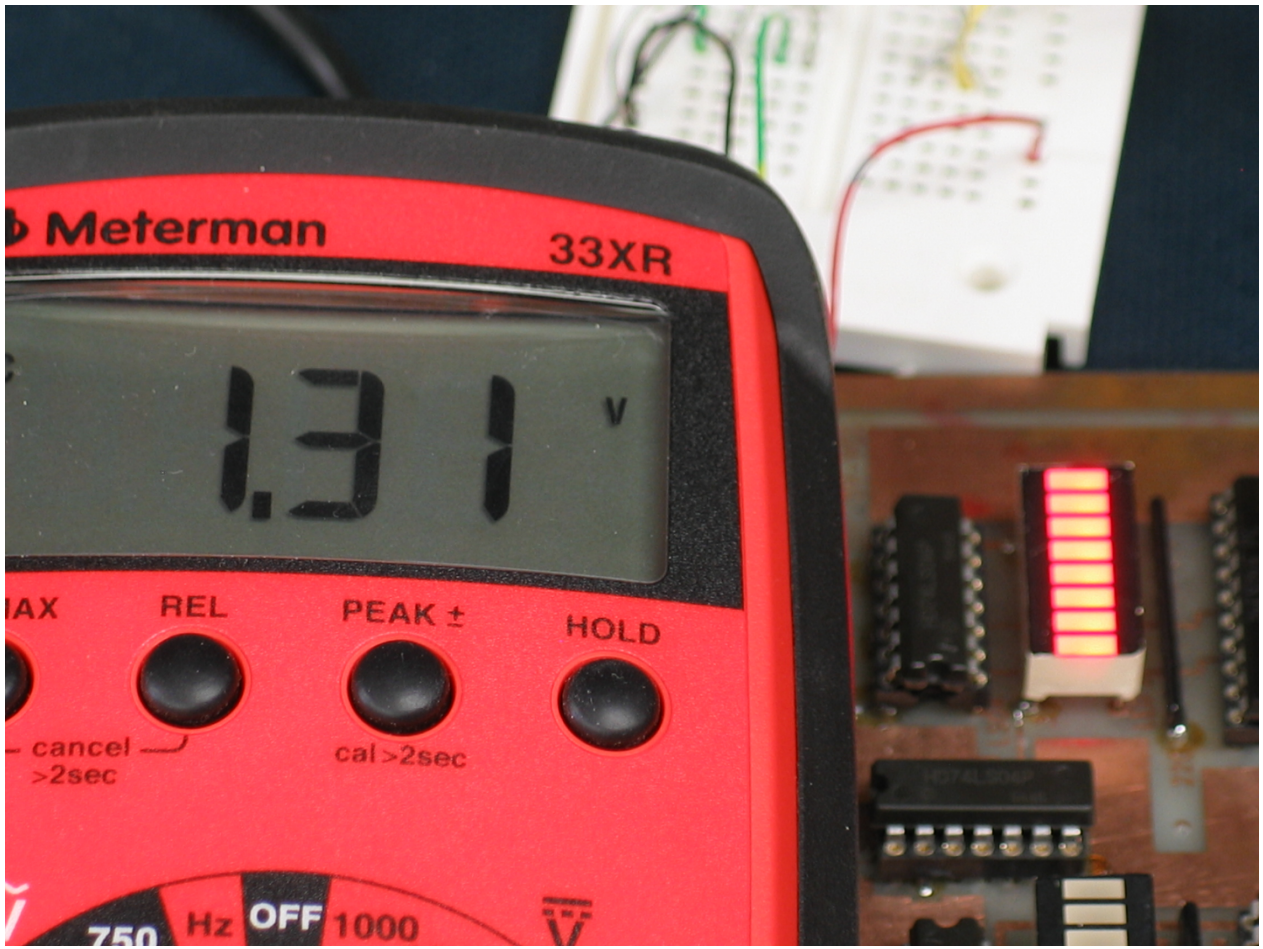
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Reading Data sheets

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Different manufacturers arrange their data sheets differently, and use different names.

Logic families

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- *With digital logic chips, however, rather than having a single "ideal" value for a parameter, the manufacturers give* ***bounds*** *for it instead.*

  This is because these ***specifications*** *are not values that should be matched, but rather they are values that should be considered as limits that one should achieve even in the "worst case" during real operation.*

- *For instance, if a family has a nominal input "high" voltage of 5 volts, then any voltage above some voltage will be considered "high".*

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  If an actual gate accepts a slightly lower voltage as a high, then that is not surprising and in fact is desirable.

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Which one is given will make sense if you understand what each parameter means.

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  For instance, TTL gates are made with **bipolar** transistors, which have a **c**ollector and an **e**mitter,

  the supply voltages are $\mathrm{V_{CC}}$ and GROUND is occasionally given as $\mathrm{V_{EE}}$.
- On the other hand, CMOS gates are built with **field–effect** transistors which have a **d**rain and a **s**ource,

  the supply voltages are $\mathrm{V_{DD}}$ and $\mathrm{V_{SS}}$.

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Four particular quantities are of interest in specifying the tolerance:

- $V_{IH_{min}}$

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  the *minimum* input voltage which will be accepted as a logic 1.

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- $V_{IL_{max}}$

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  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{max}}$

  the *maximum* input voltage which will be accepted as a logic 0.

- $V_{IH_{min}}$

  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{max}}$

  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{min}}$

- $V_{IH_{min}}$

  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{max}}$

  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{min}}$

  the *minimum* output voltage representing a logic 1 state.

- $V_{IH_{min}}$

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- $V_{IL_{max}}$

  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{min}}$

  the *minimum* output voltage representing a logic 1 state.
- $V_{OL_{max}}$

- $V_{IH_{min}}$

  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{max}}$

  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{min}}$

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- $V_{OL_{max}}$

  the *maximum* output voltage representing a logic 0 state.

For the 3 logic families to be studied, the *specified* values of these parameters are given in the following table.

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Family	$V_{IH_{min}}$	$V_{IL_{max}}$	$V_{OH_{min}}$	$V_{OL_{max}}$
TTL	2.0	0.8	2.4	0.4
LSTTL	2.0	0.8	2.7	0.5
CMOS	$0.7V_{DD}$	$0.3V_{DD}$	$0.99V_{DD}$	$0.01V_{DD}$
V_{DD}=5V	3.5	1.5	4.95	0.05

What the above information means is that, (for instance), if both *inputs* to a 7400 TTL NAND gate are at greater than or equal to 2.4 volts, they will be considered “high”, and so the *output* should be “low”,

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$V_{OH_{min}}$

$V_{IH_{min}}$

$V_{IL_{max}}$

$V_{OL_{max}}$

TTL

$V_{OL_{max}}$

Anything below here is a valid LOW *output*

TTL

$V_{IL_{max}}$

Anything below here is a valid LOW *input*

TTL

$V_{IH_{min}}$

Anything above here is a valid HIGH *input*

TTL

TTL

$V_{OH_{min}}$

Anything above here is a valid HIGH *output*

$V_{OH_{min}}$

Anything above here is a valid HIGH *output*

$V_{OL_{max}}$

Anything below here is a valid LOW *output*

TTL

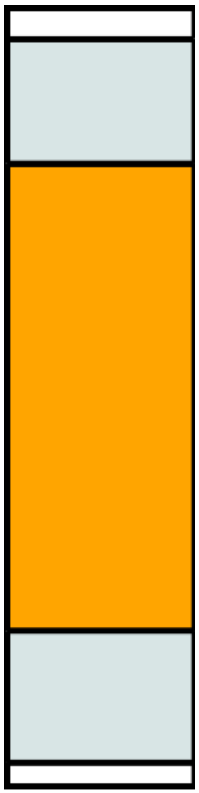
$V_{IH_{min}}$

Anything above here is a valid HIGH *input*

$V_{IL_{max}}$

Anything below here is a valid LOW *input*

TTL



$V_{OH_{min}}$

$V_{IH_{min}}$

$V_{IL_{max}}$

$V_{OL_{max}}$

CMOS

CMOS logic

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Note: For CMOS logic V_{DD} can be as low as 3.5V and as high as 15V.

Noise immunity

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  In other words, if a bit of noise (i.e. voltage fluctuation) were added to the output of one gate, it should not affect a gate which follows this one.
- Imagine what would happen if the limits were the same.

$V_{OH_{min}}$

$V_{IH_{min}}$

$V_{IL_{max}}$

$V_{OL_{max}}$

TTL

$V_{OH_{min}}$

$V_{IH_{min}}$

$V_{IL_{max}}$

$V_{OL_{max}}$

Output here will still be seen as HIGH

TTL

$V_{OH_{min}}$

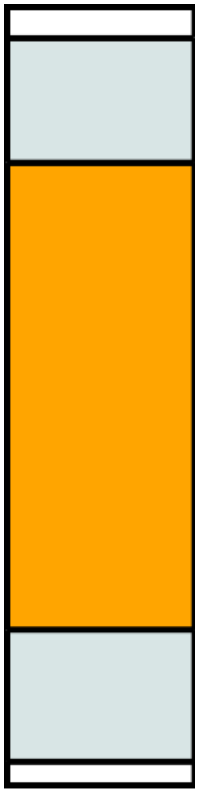
$V_{IH_{min}}$

$V_{IL_{max}}$

$V_{OL_{max}}$

Output here will still be seen as LOW

TTL



$V_{OH_{min}}$

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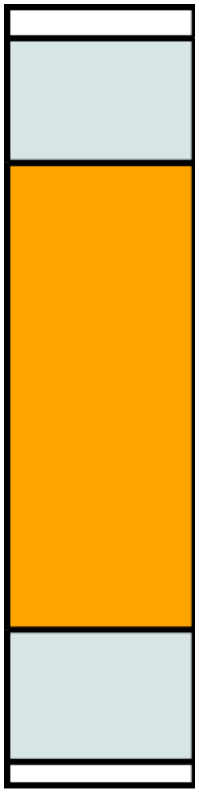
CMOS



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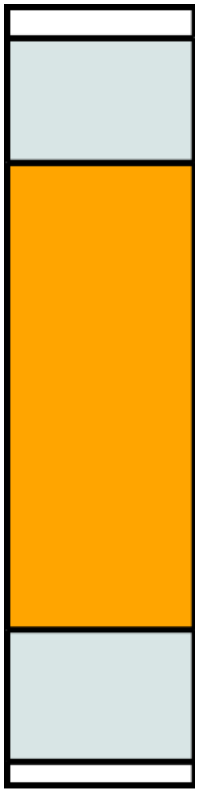

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Output here will still be seen as LOW

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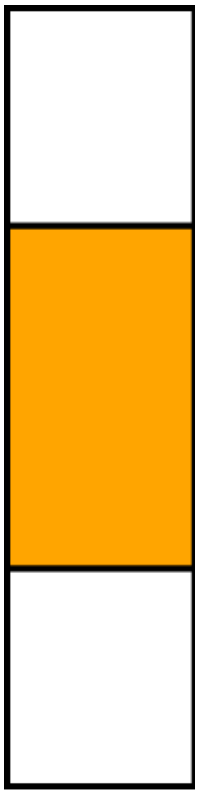
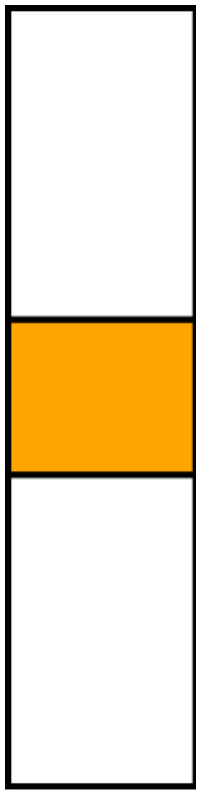
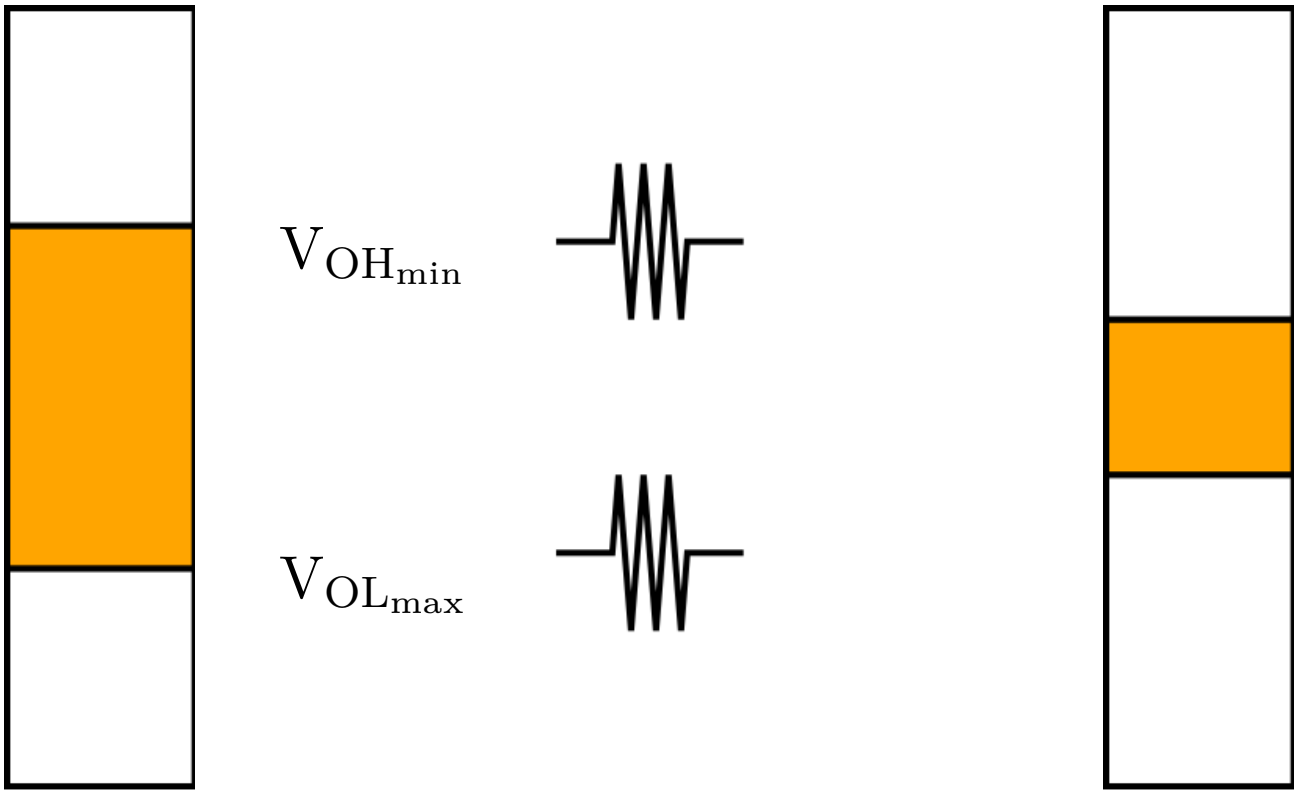
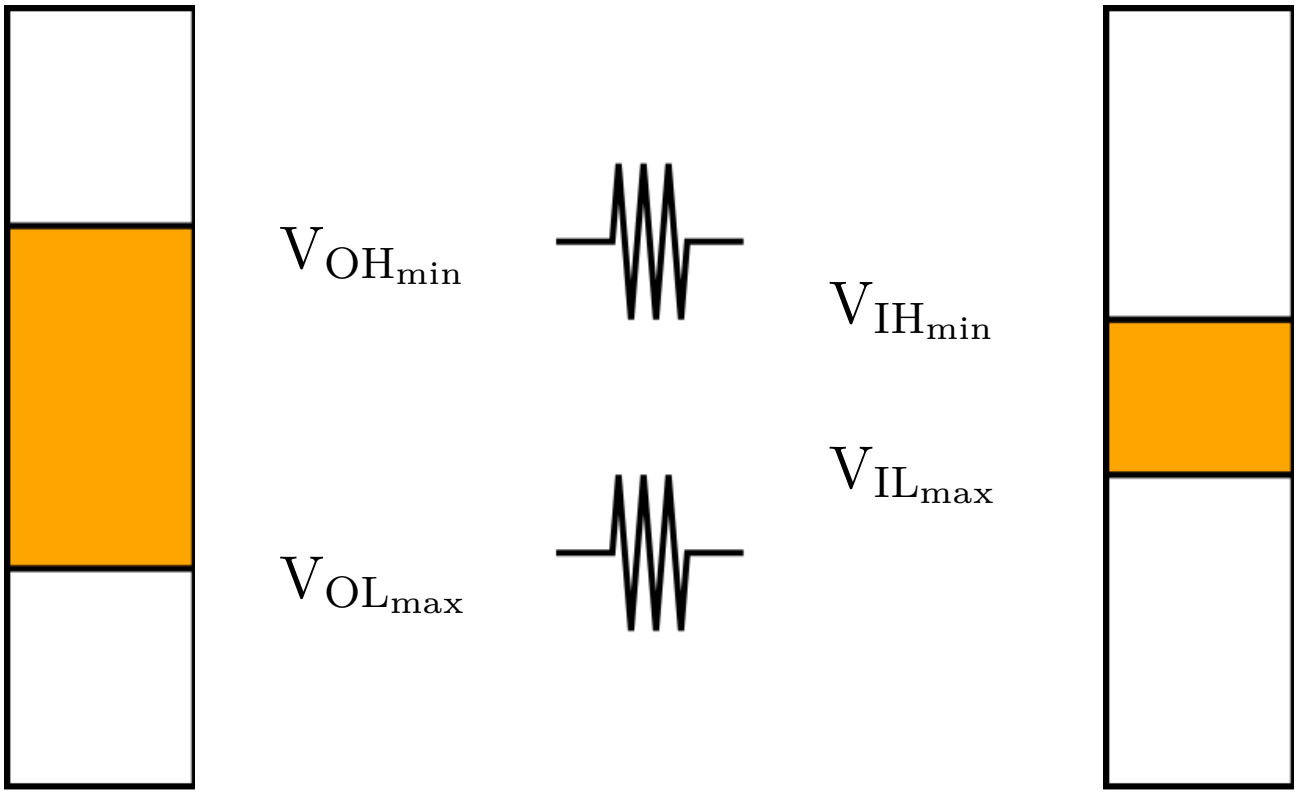




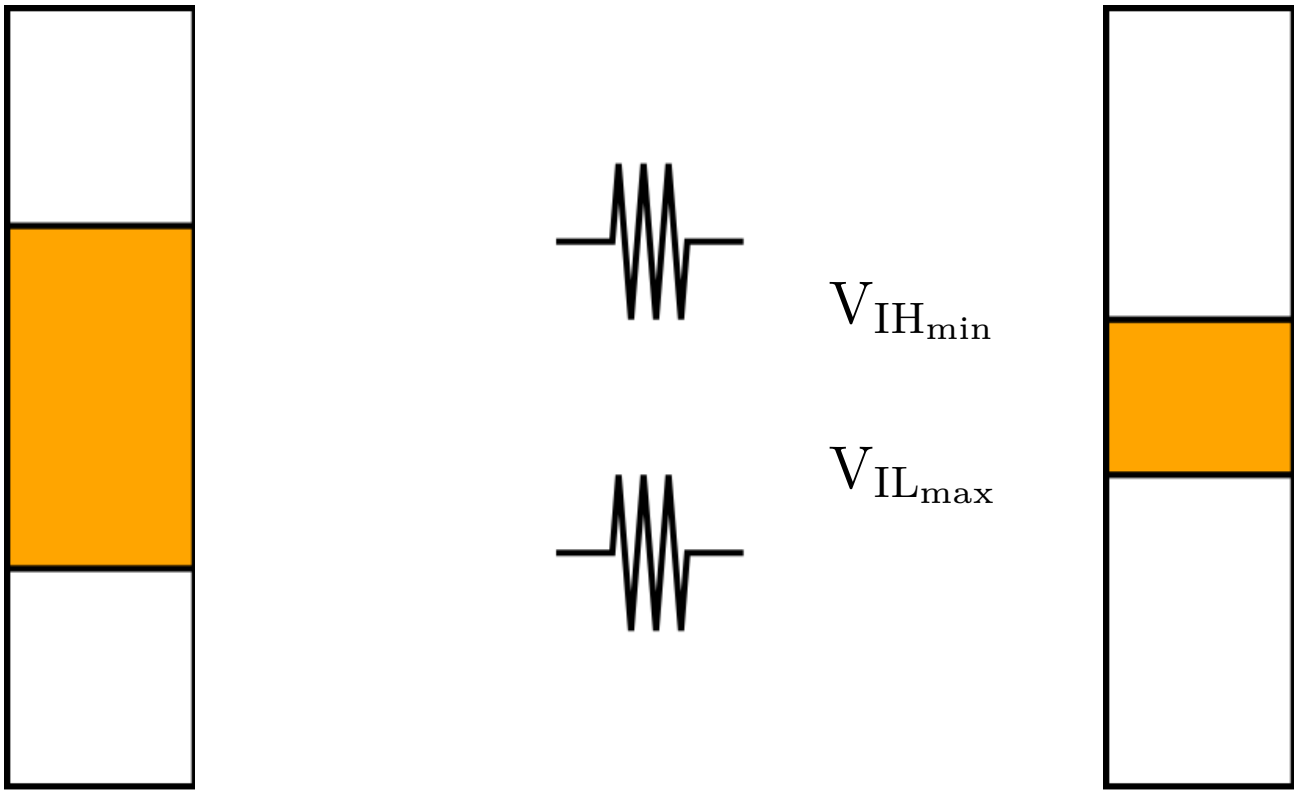
Consider one gate feeding into another.



If a signal gets *noise* added to it, the voltage will fluctuate up and down.



A certain amount of noise will still leave the resulting signal within the *input* limits of the second gate.



The difference between the output and input limits is the **noise immunity**.