Electronics
Logic Gate Characteristics: Voltage and Time

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- Now the real (i.e. non-ideal) operating characteristics of different logic families will be studied.
- The operation of an *ideal* logic gate can be summarized by the following rules:

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- Any change of an input will immediately be reflected on the output.

Real logic gates

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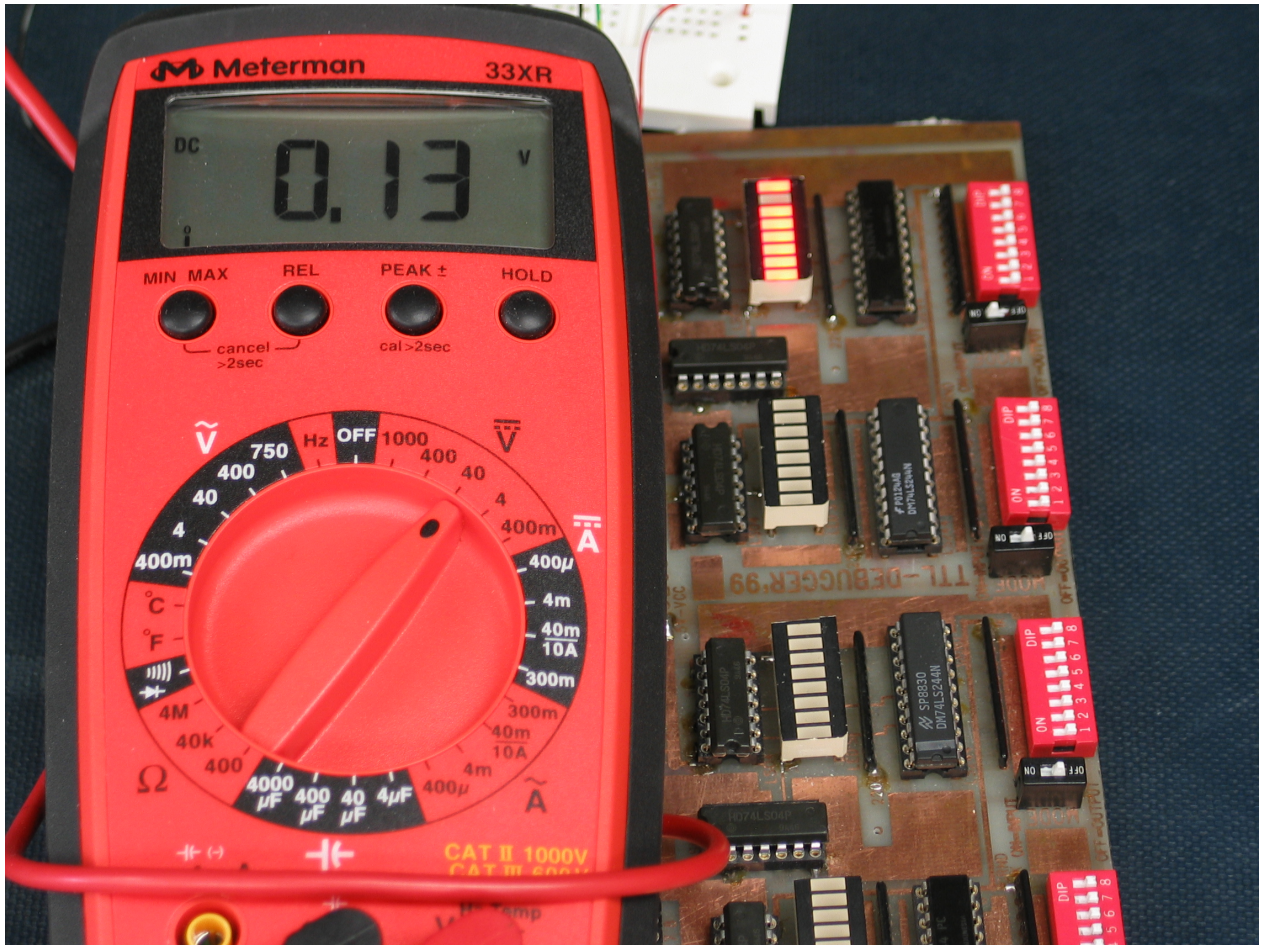

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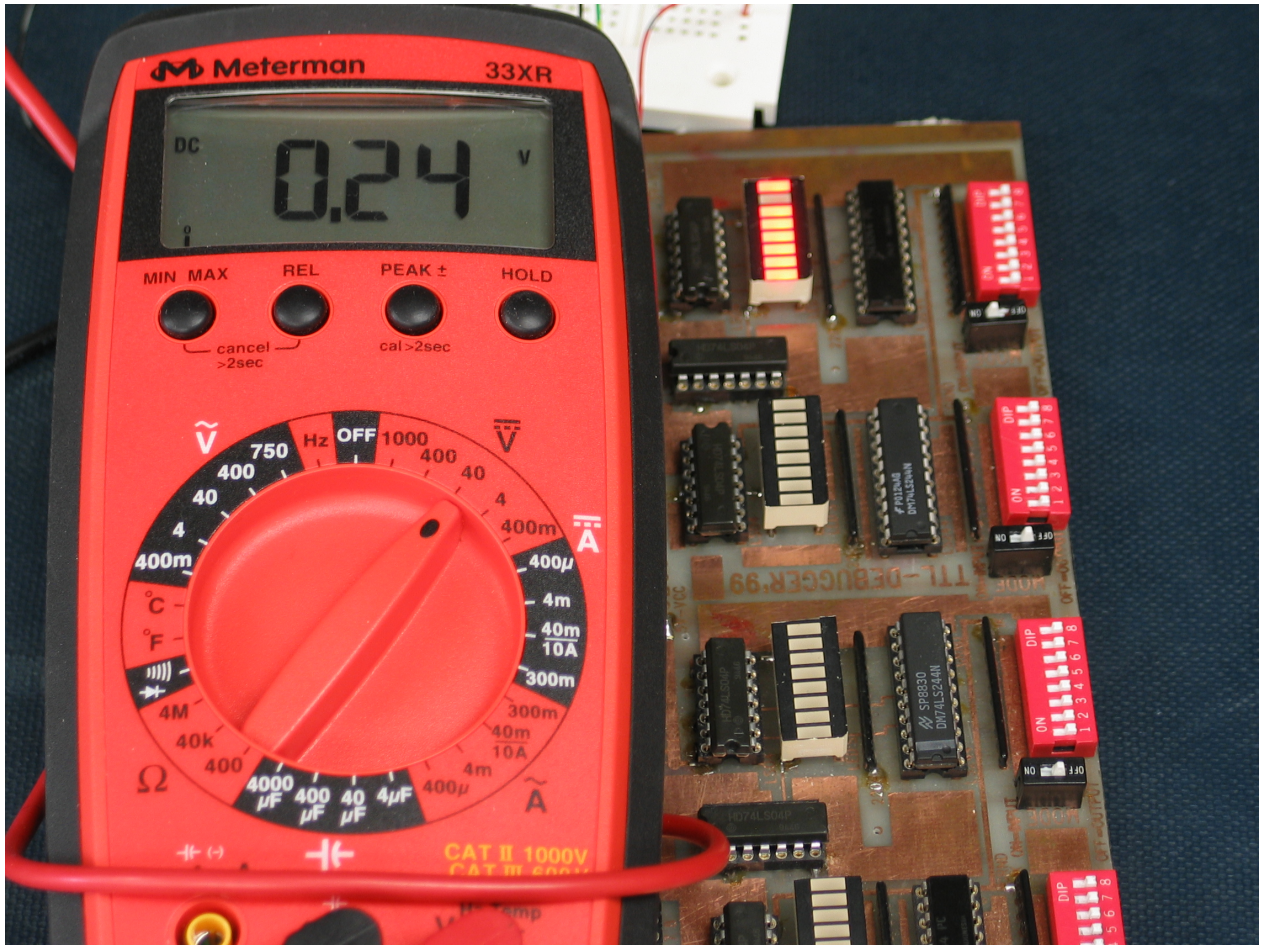

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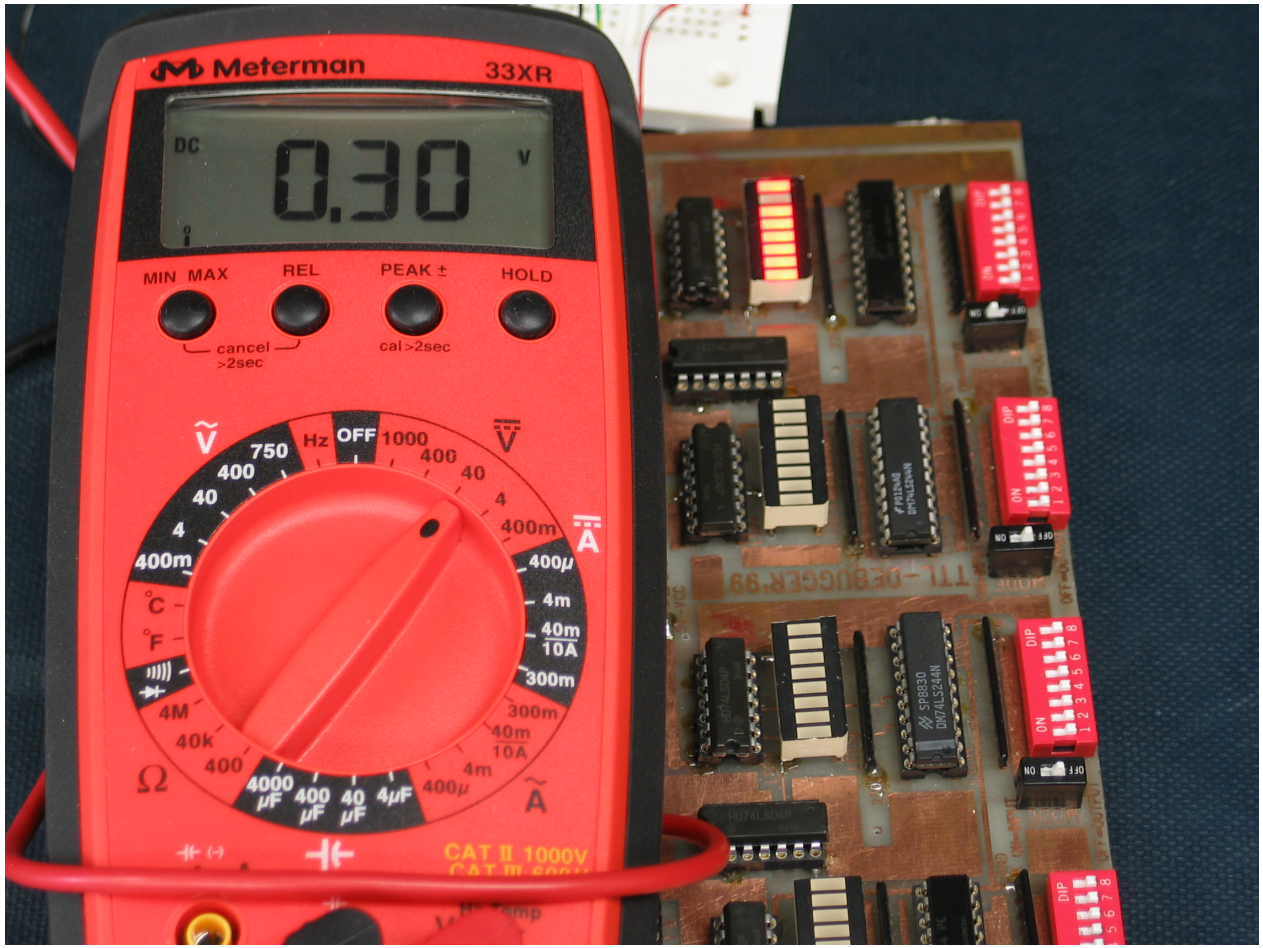

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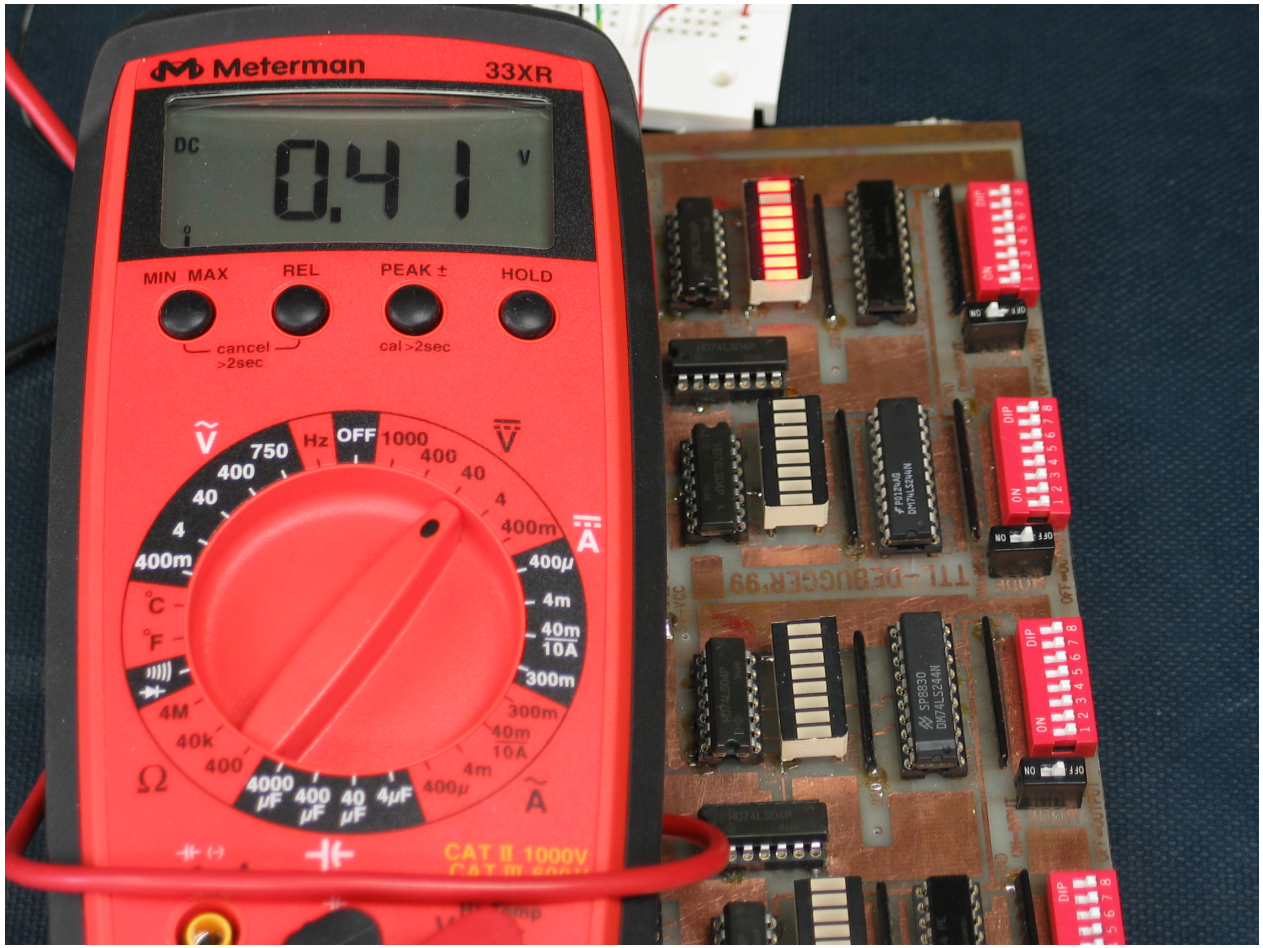

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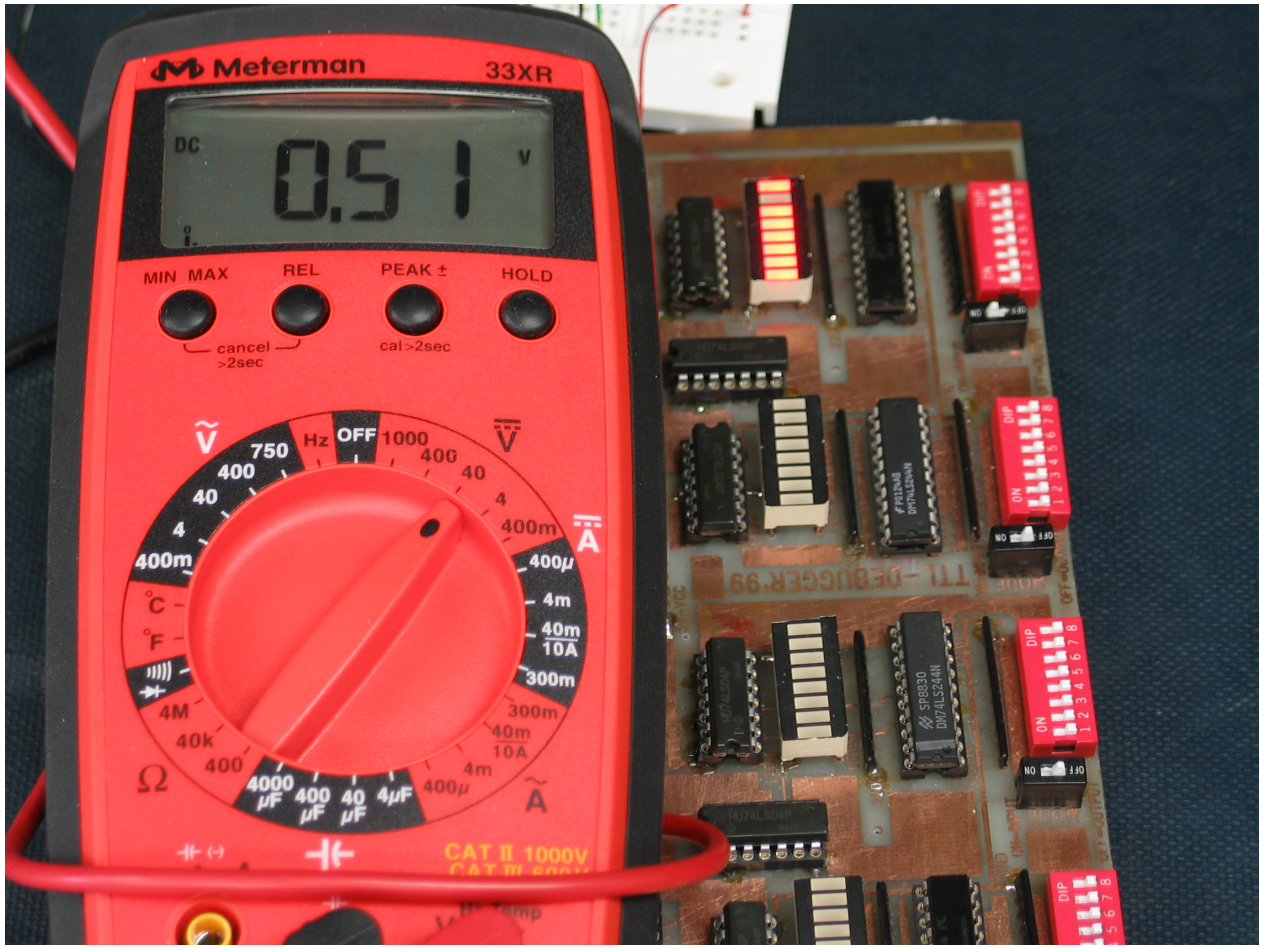

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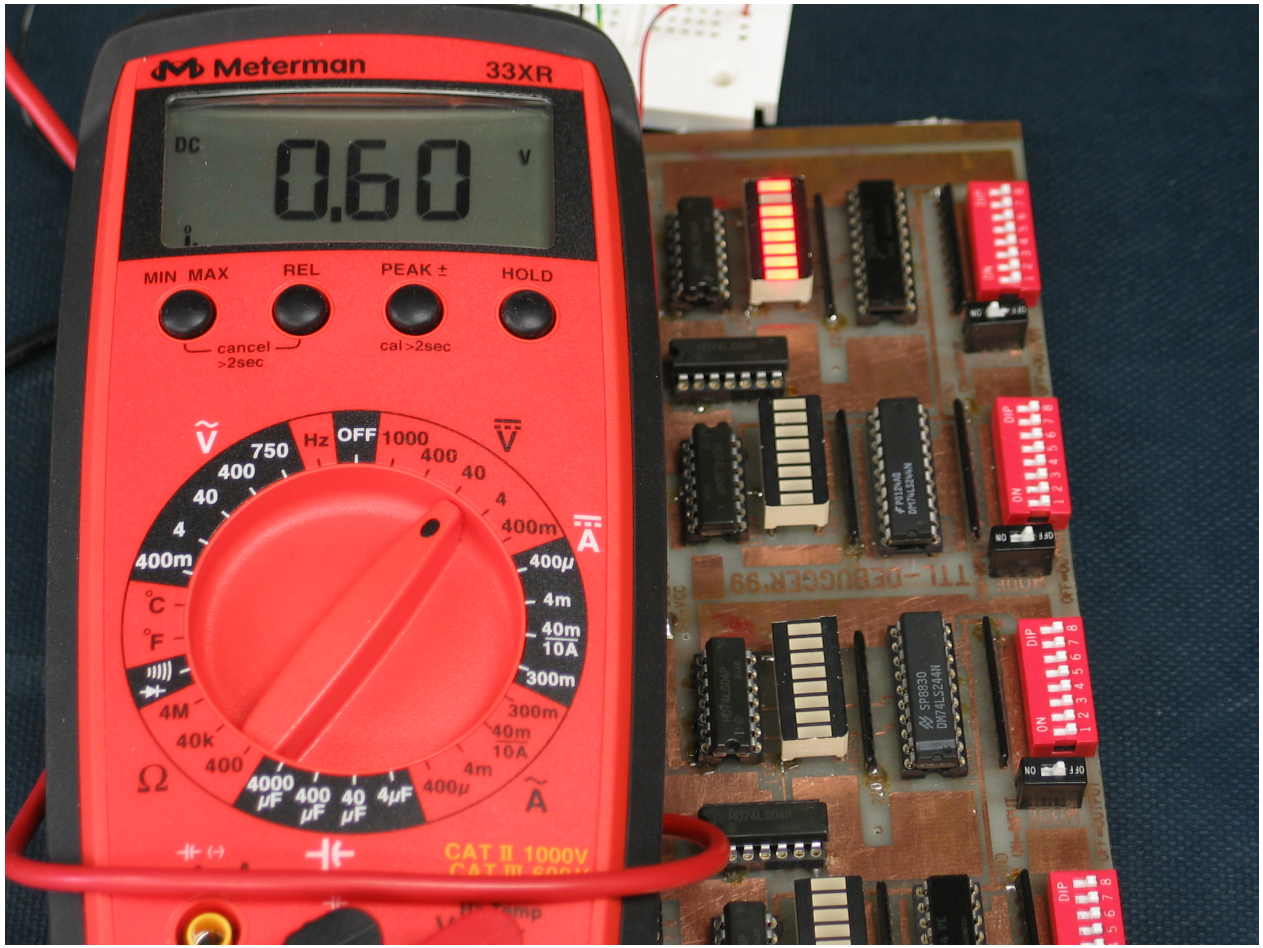

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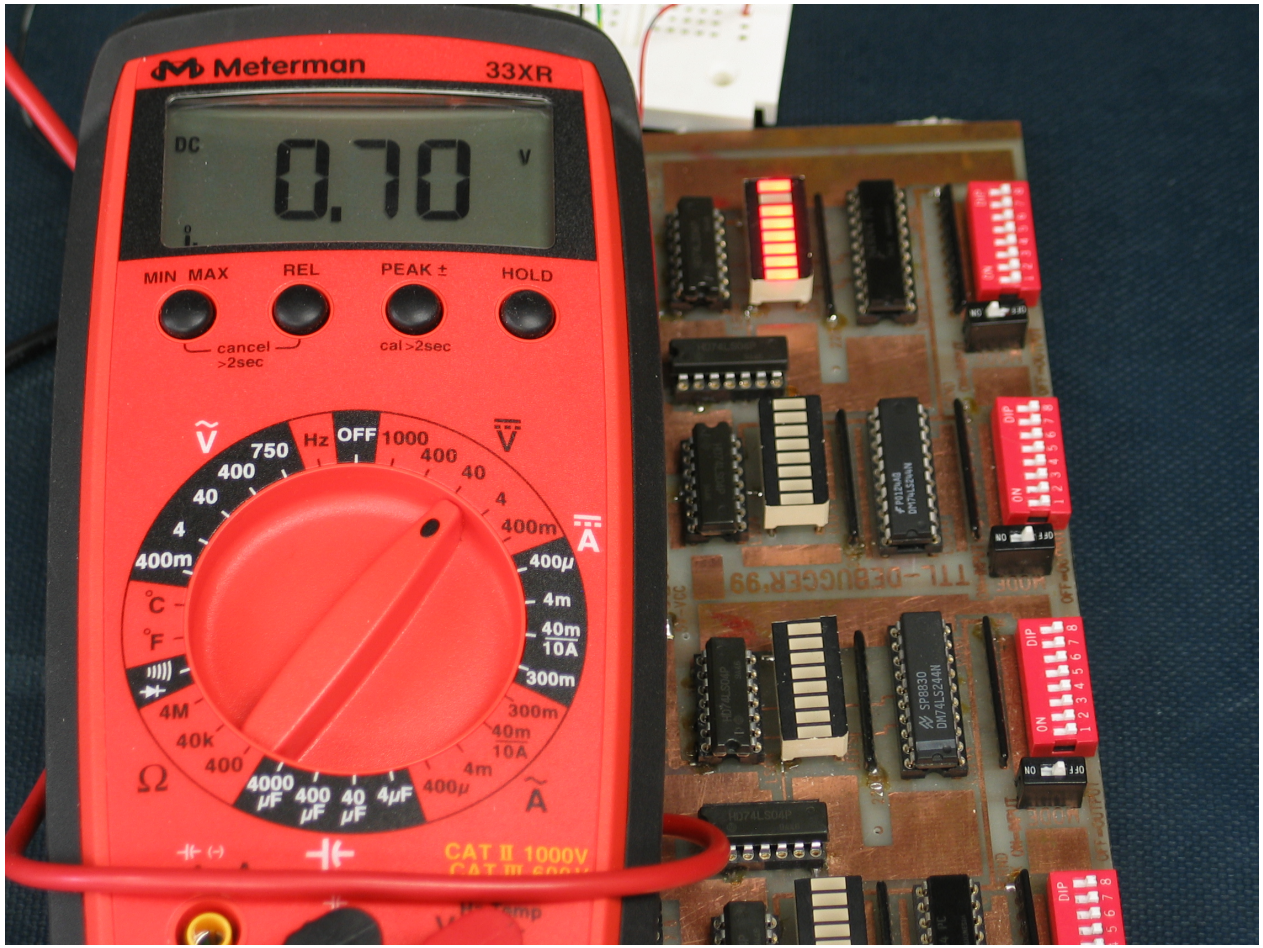

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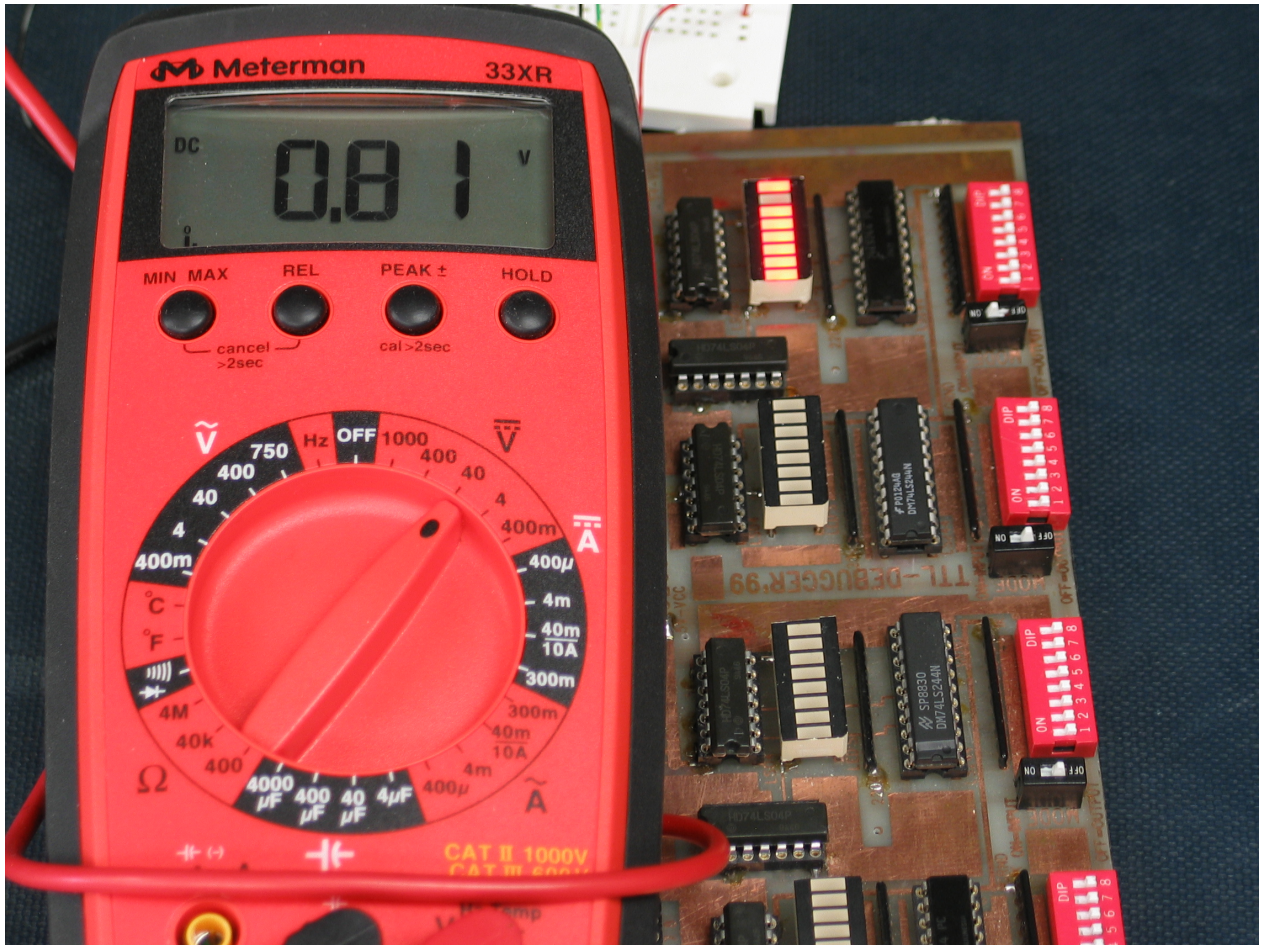

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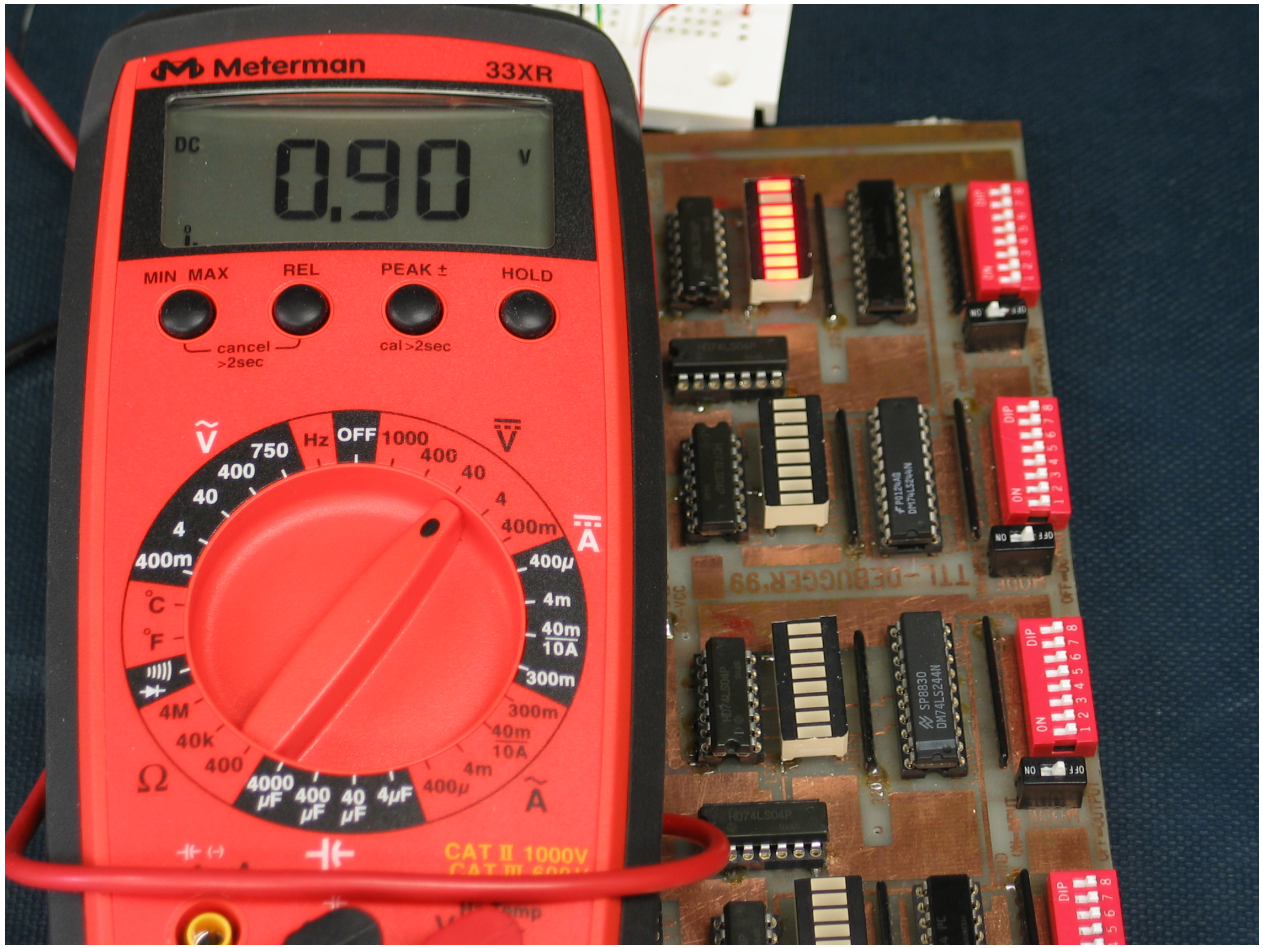

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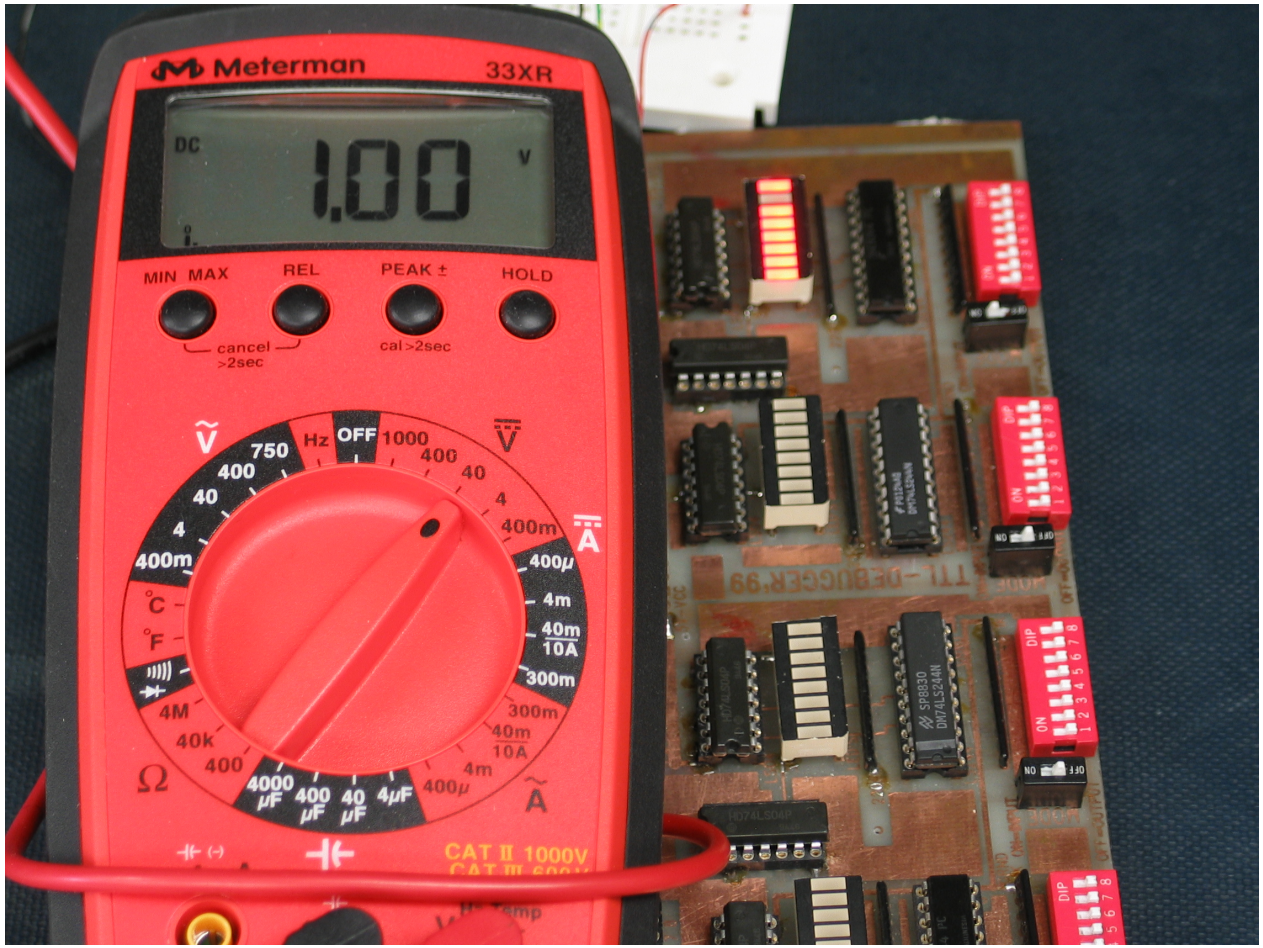

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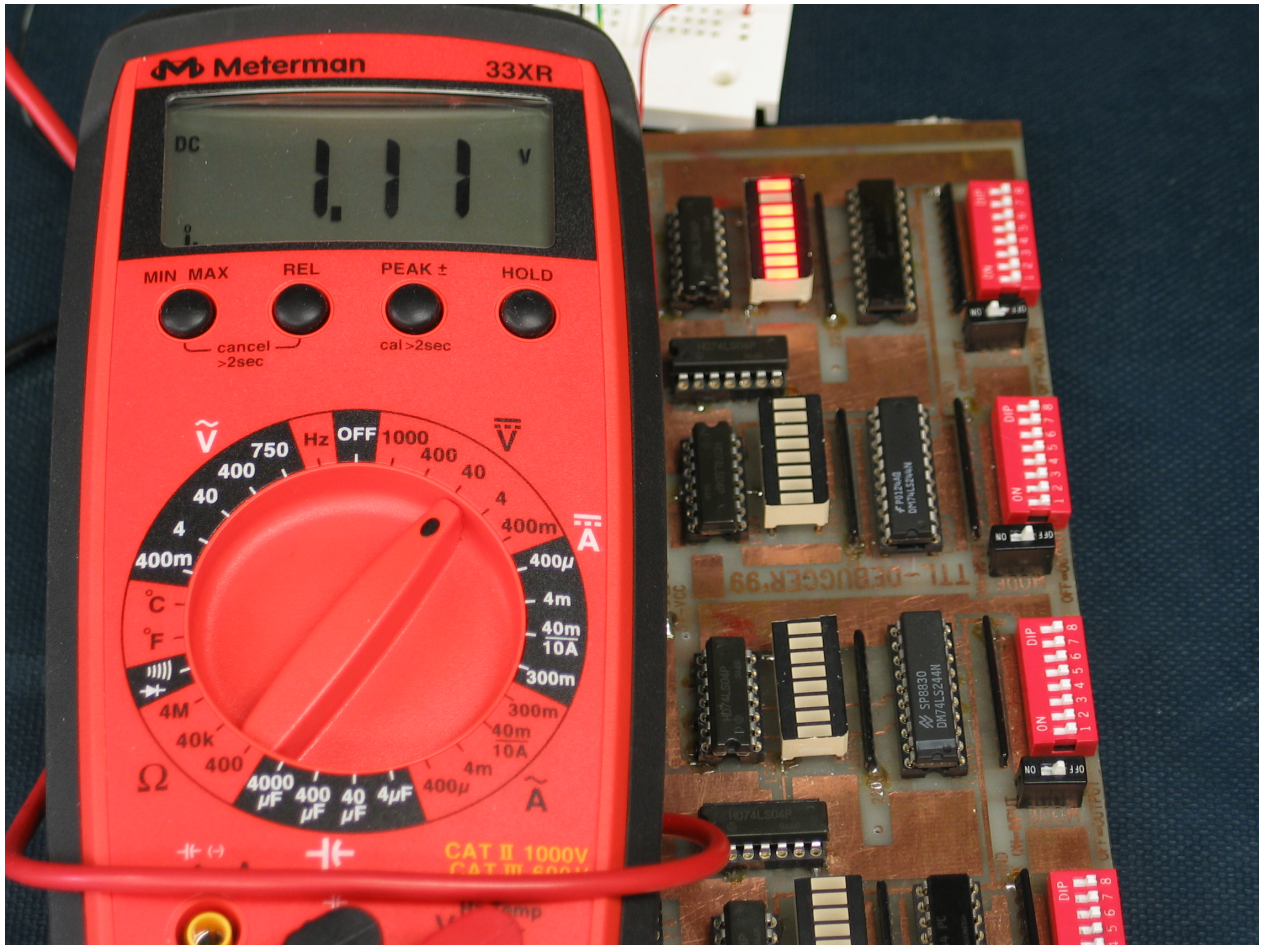

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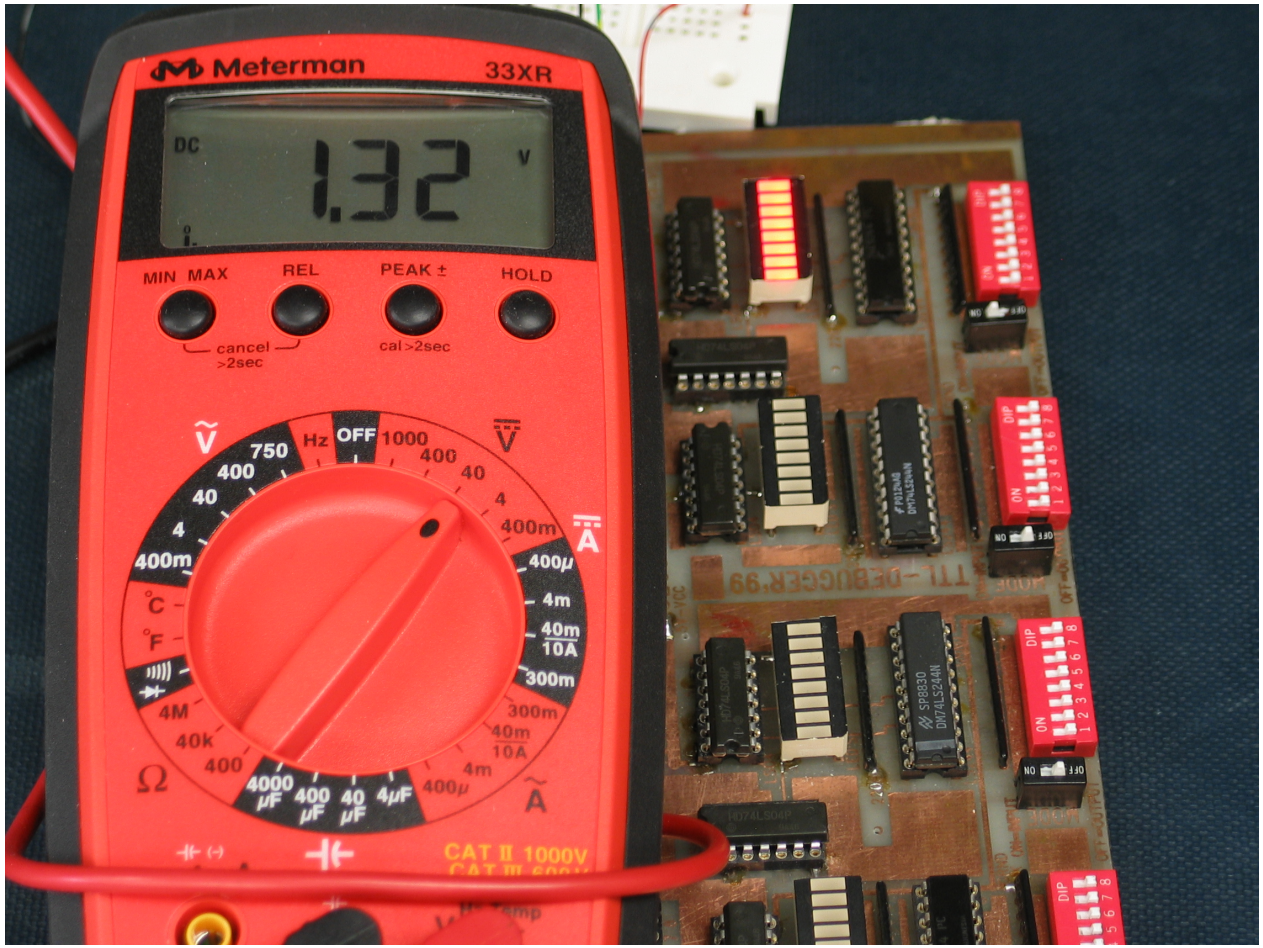

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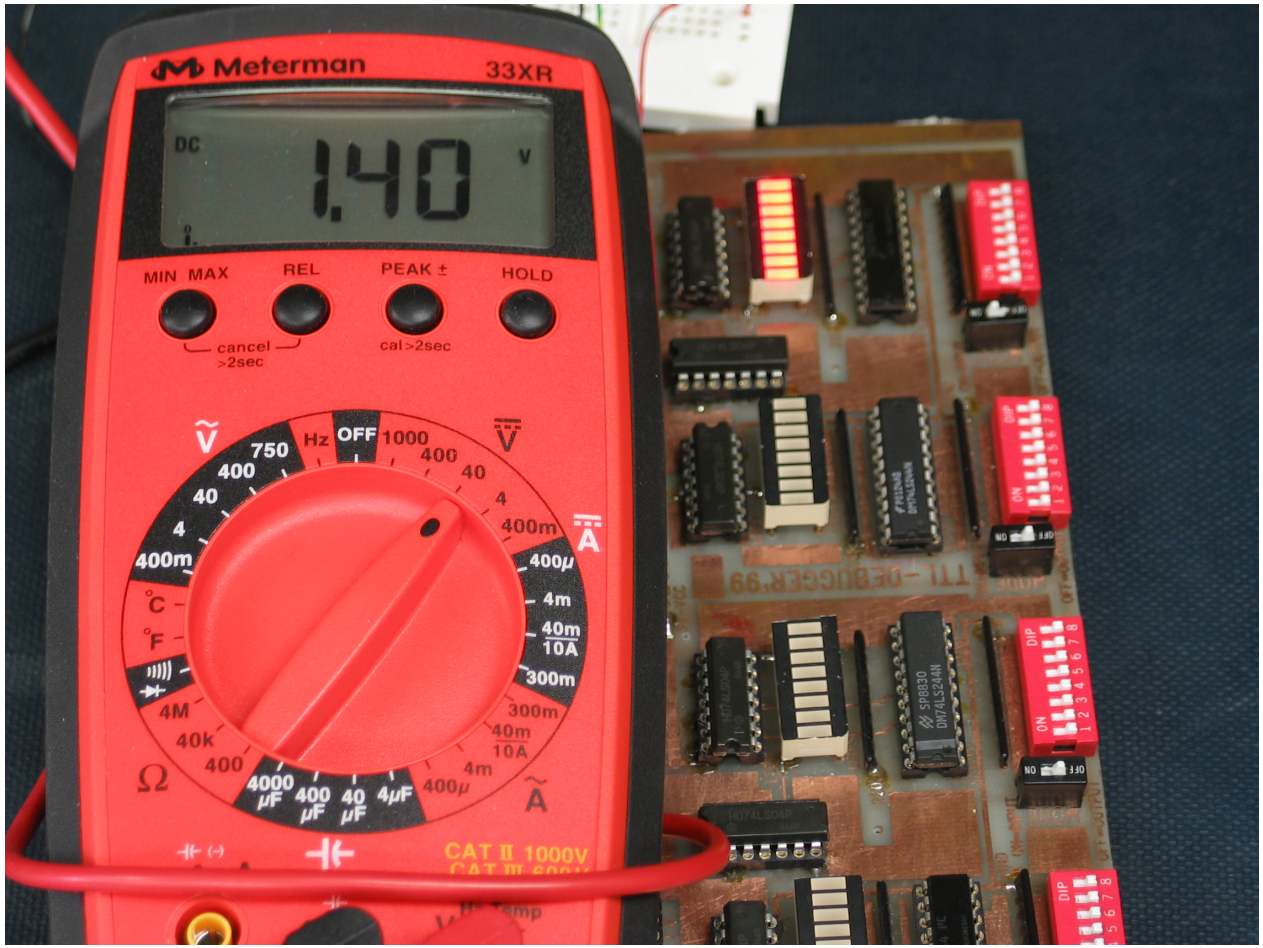

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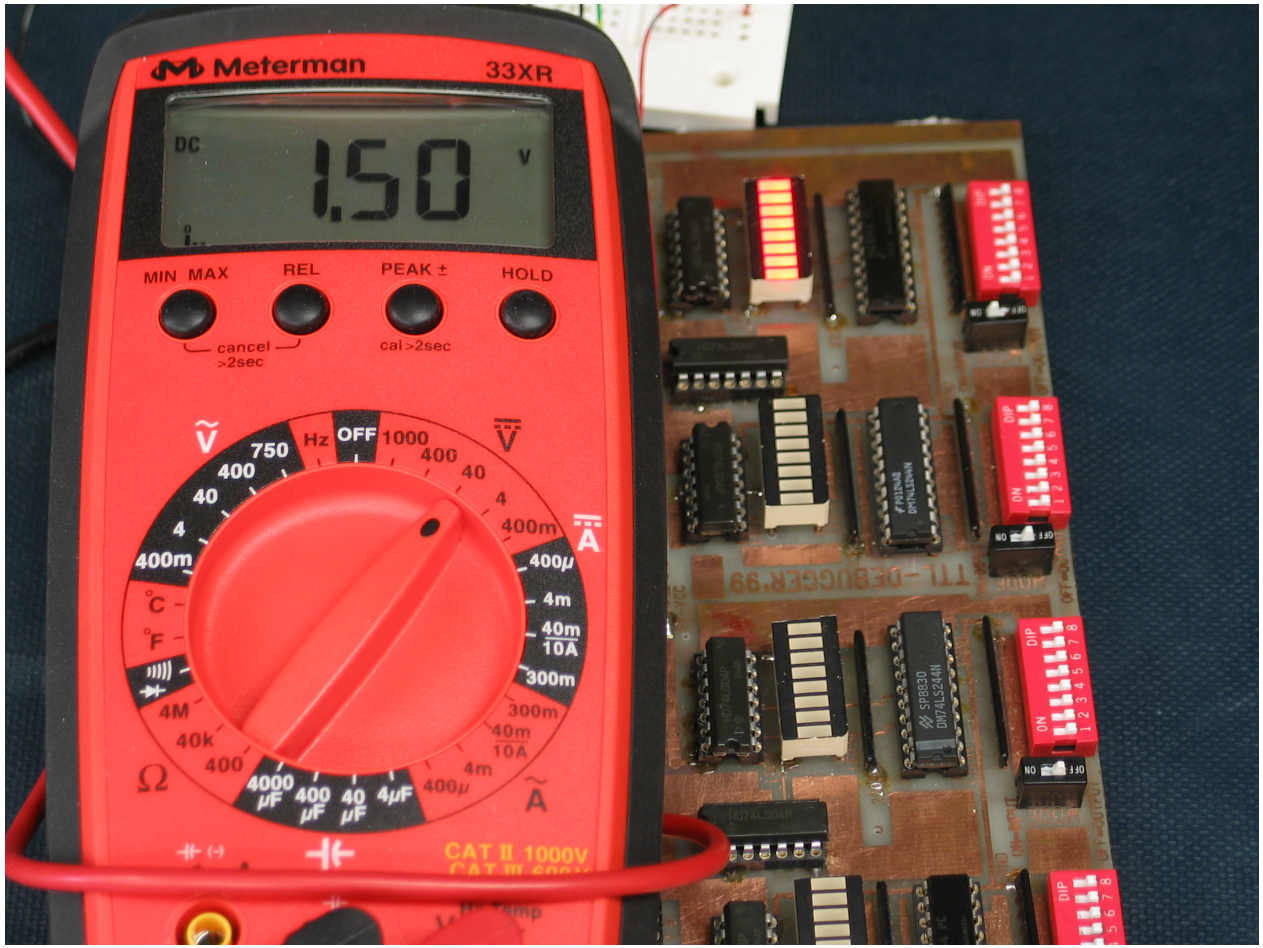

More detail

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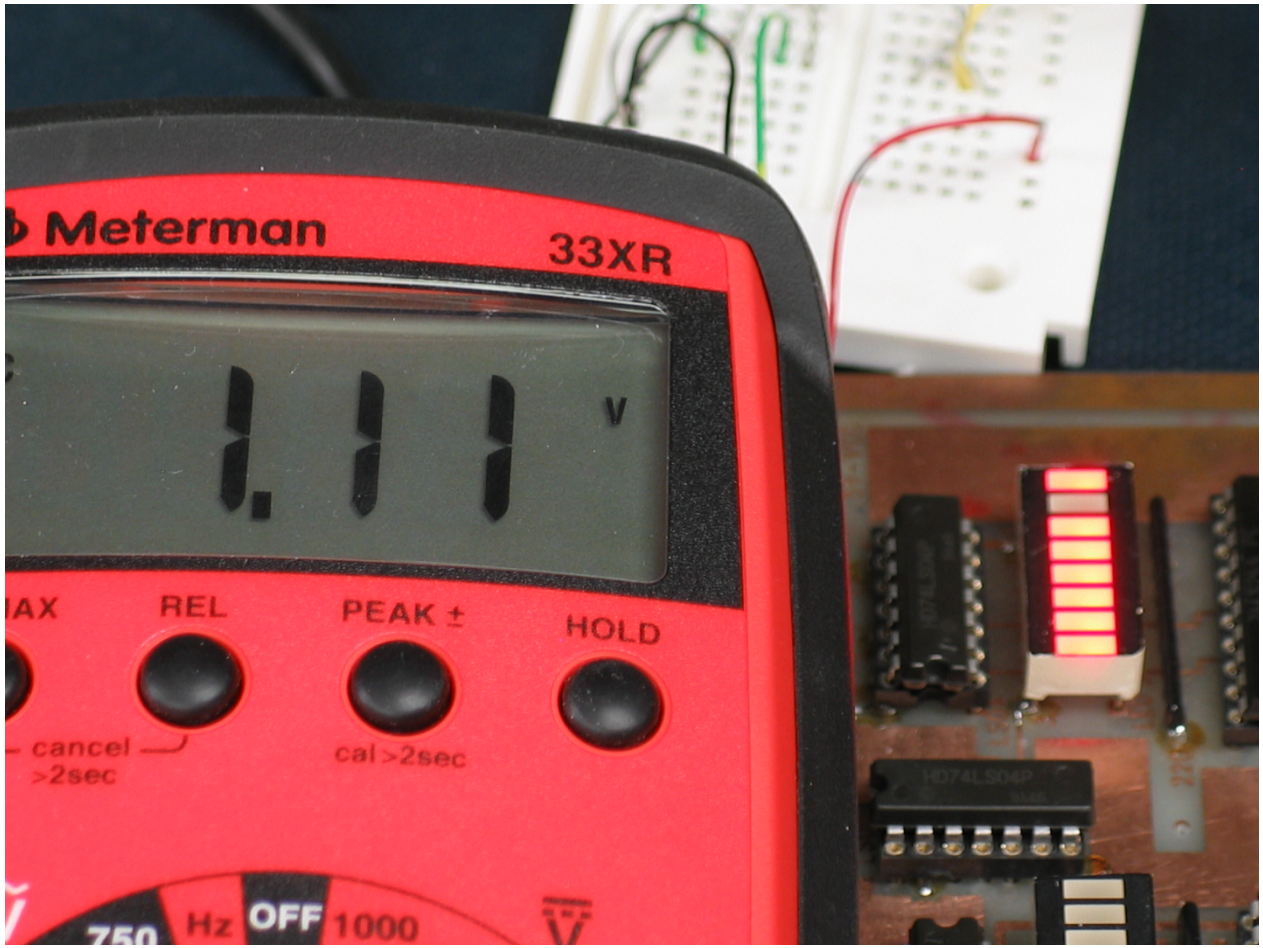
Meterman
33XR
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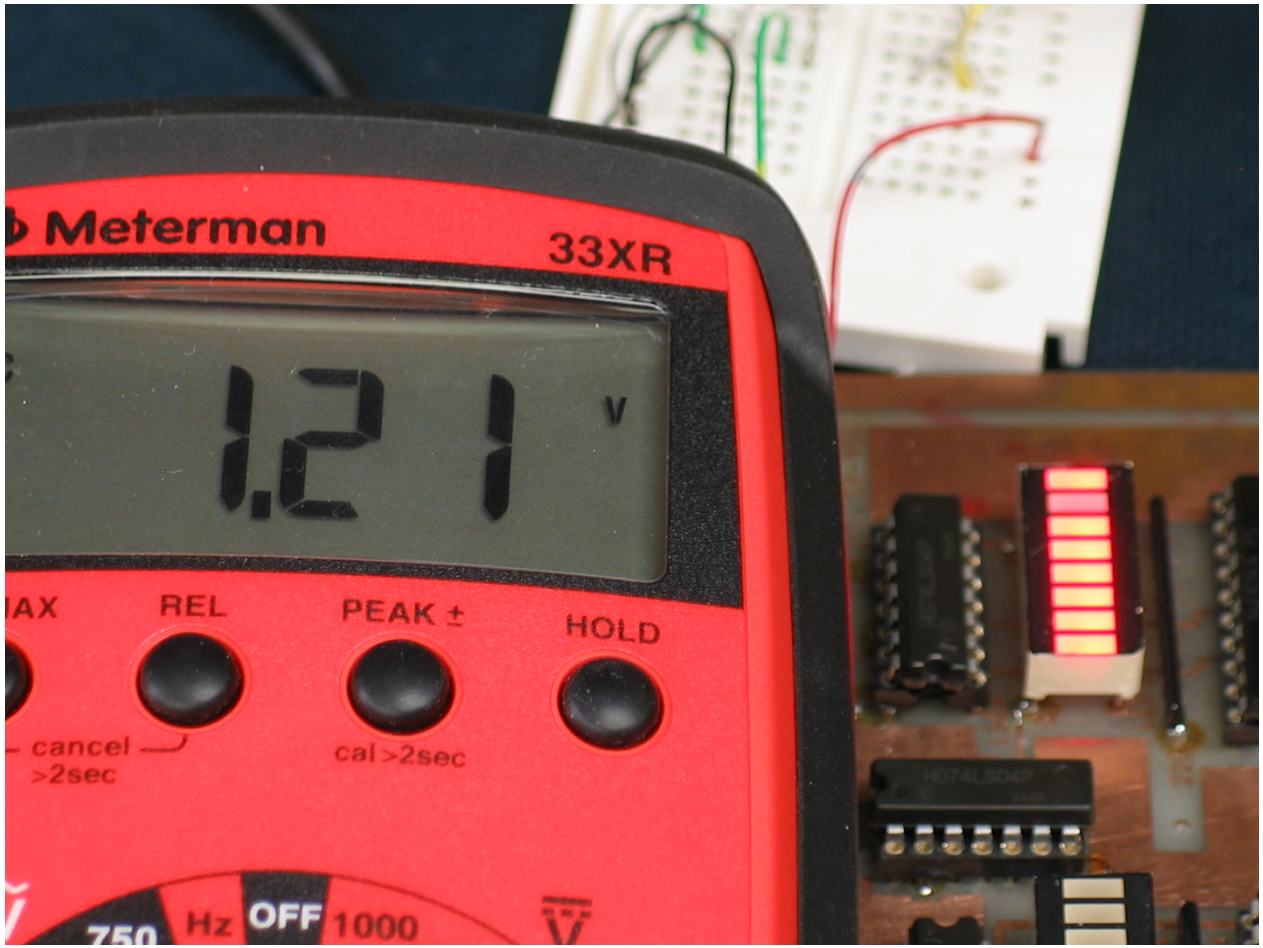
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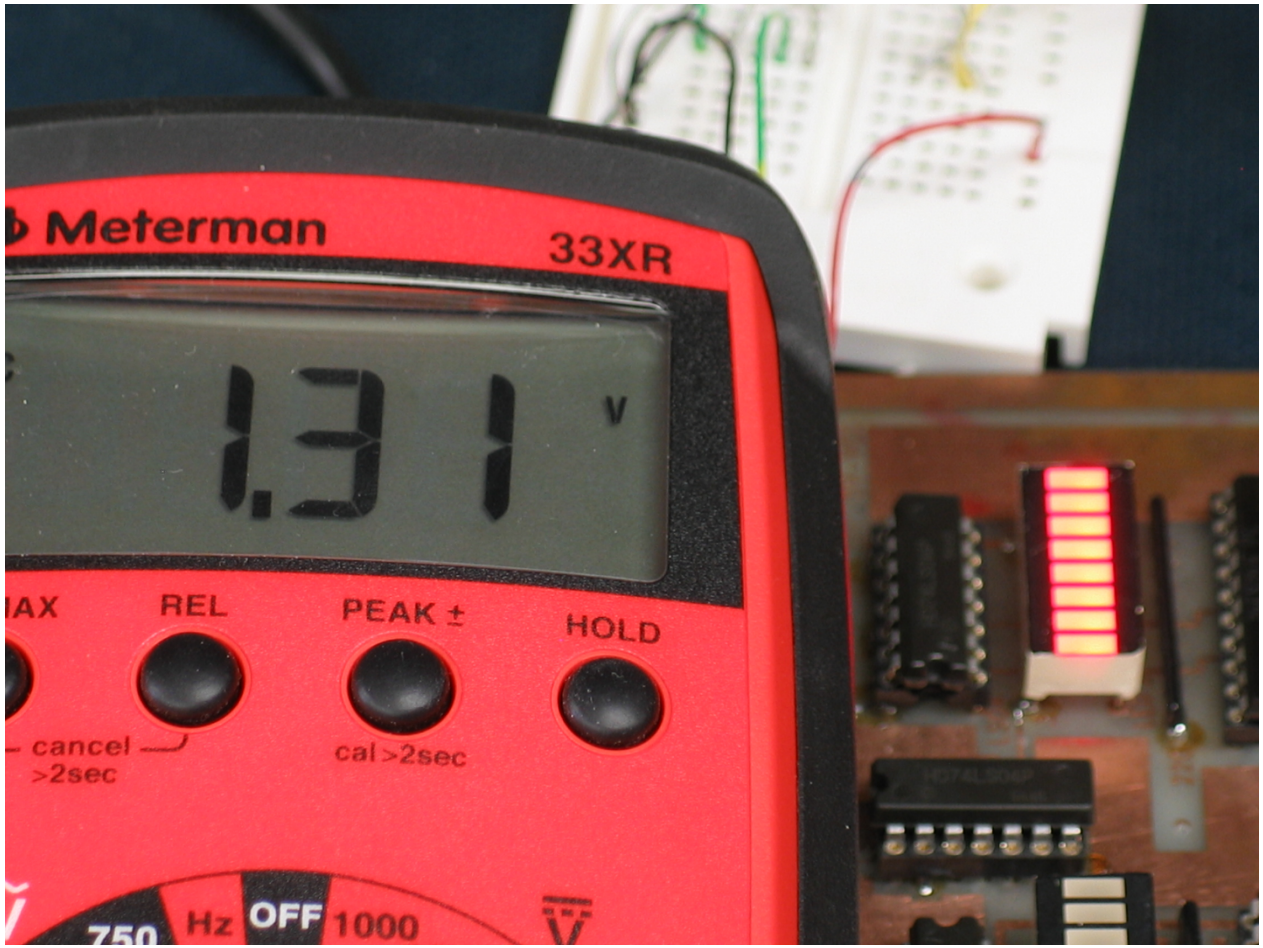
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- Outputs have a limited current capacity for maintaining the output voltage at the desired level.

Reading Data sheets

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Different manufacturers arrange their data sheets differently, and use different names.

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- *With digital logic chips, however, rather than having a single "ideal" value for a parameter, the manufacturers give* ***bounds*** *for it instead.*

  This is because these ***specifications*** *are not values that should be matched, but rather they are values that should be considered as limits that one should achieve even in the "worst case" during real operation.*

- *For instance, if a family has a nominal input "high" voltage of 5 volts, then any voltage above some voltage will be considered "high".*

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  If an actual gate accepts a slightly lower voltage as a high, then that is not surprising and in fact is desirable.

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Which one is given will make sense if you understand what each parameter means.

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Four particular quantities are of interest in specifying the tolerance:

- $V_{IH_{min}}$

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  the *minimum* input voltage which will be accepted as a logic 1.

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- $V_{IH_{min}}$

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- $V_{IL_{max}}$

  the *maximum* input voltage which will be accepted as a logic 0.
- $V_{OH_{min}}$

- $V_{IH_{min}}$

  the *minimum* input voltage which will be accepted as a logic 1.
- $V_{IL_{max}}$

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  the *minimum* output voltage representing a logic 1 state.

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- $V_{OL_{max}}$

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  the *maximum* input voltage which will be accepted as a logic 0.
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For the 3 logic families to be studied, the *specified* values of these parameters are given in the following table.

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Family	$V_{IH_{min}}$	$V_{IL_{max}}$	$V_{OH_{min}}$	$V_{OL_{max}}$
TTL	2.0	0.8	2.4	0.4
LSTTL	2.0	0.8	2.7	0.5
CMOS	$0.7V_{DD}$	$0.3V_{DD}$	$0.99V_{DD}$	$0.01V_{DD}$
V_{DD}=5V	3.5	1.5	4.95	0.05

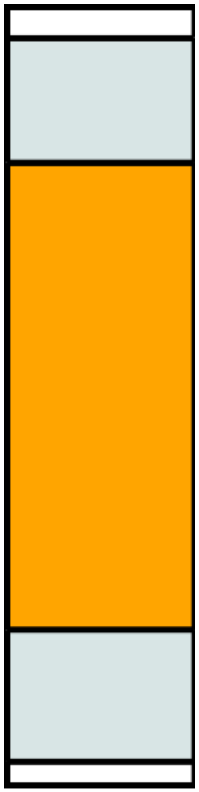
$V_{OH_{min}}$

$V_{IH_{min}}$

$V_{IL_{max}}$

$V_{OL_{max}}$

TTL



$V_{OH_{min}}$

$V_{IH_{min}}$

$V_{IL_{max}}$

$V_{OL_{max}}$

CMOS

CMOS logic

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Note: For CMOS logic V_{DD} can be as low as 3.5V and as high as 15V.

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  For instance, TTL gates are made with **bipolar** transistors, which have a **c**ollector and an **e**mitter,

  the supply voltages are $\mathrm{V_{CC}}$ and GROUND is occasionally given as $\mathrm{V_{EE}}$.
- On the other hand, CMOS gates are built with **field–effect** transistors which have a **d**rain and a **s**ource,

  the supply voltages are $\mathrm{V_{DD}}$ and $\mathrm{V_{SS}}$.

What the above information means is that, (for instance), if both *inputs* to a 7400 TTL NAND gate are at greater than or equal to 2.4 volts, they will be considered “high”, and so the *output* should be “low”,

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Noise immunity

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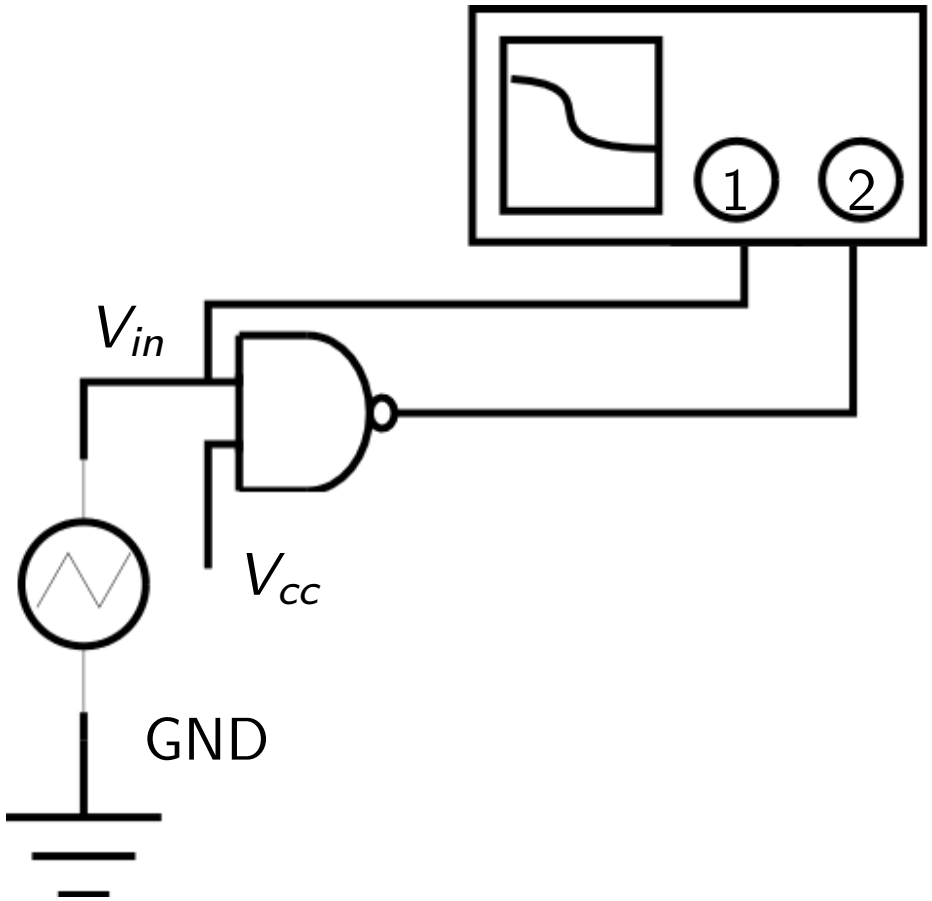
  In other words, if a bit of noise (i.e. voltage fluctuation) were added to the output of one gate, it should not affect a gate which follows this one.
- Imagine what would happen if the limits were the same.

Measuring voltage limits

Measuring voltage limits

In order to measure the voltage limits, you can connect up the circuit as in the following figure.


1
2
V_{in}
V_{cc}
GND

Using a sine wave input with the oscilloscope operating in the X–Y mode, a trace similar to the one shown in the following figure should be obtained.

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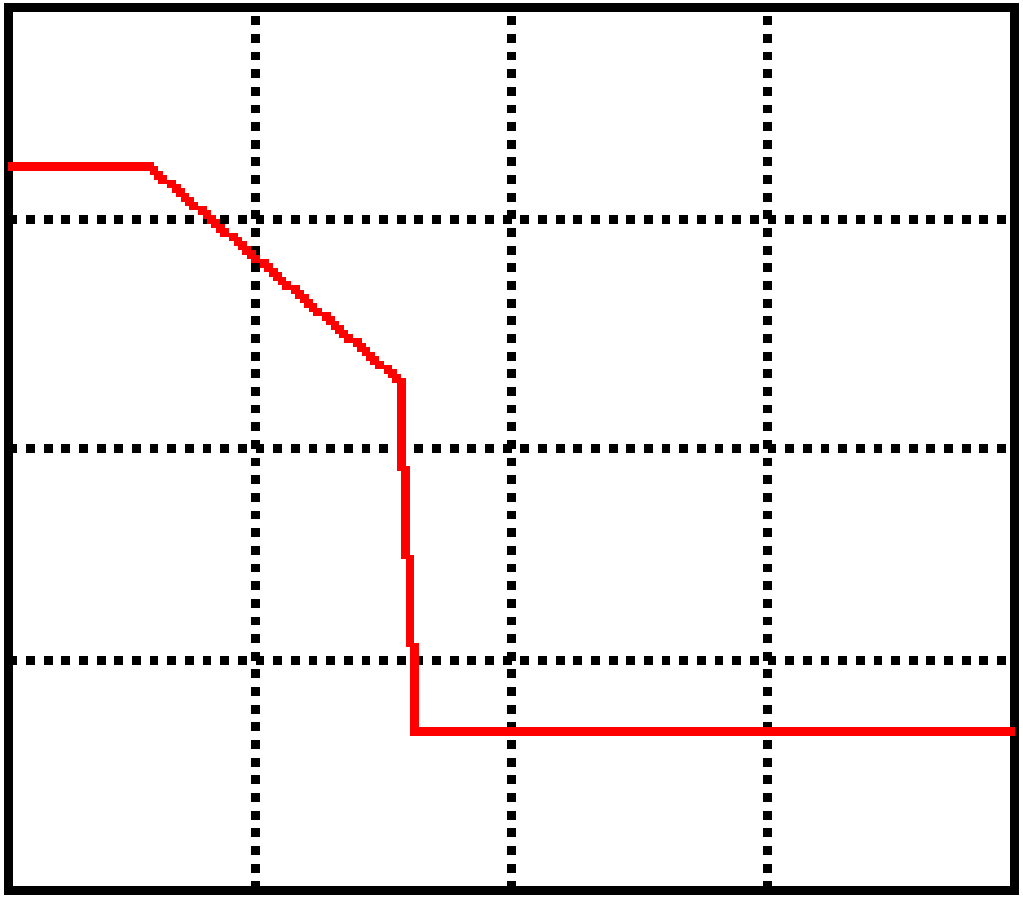
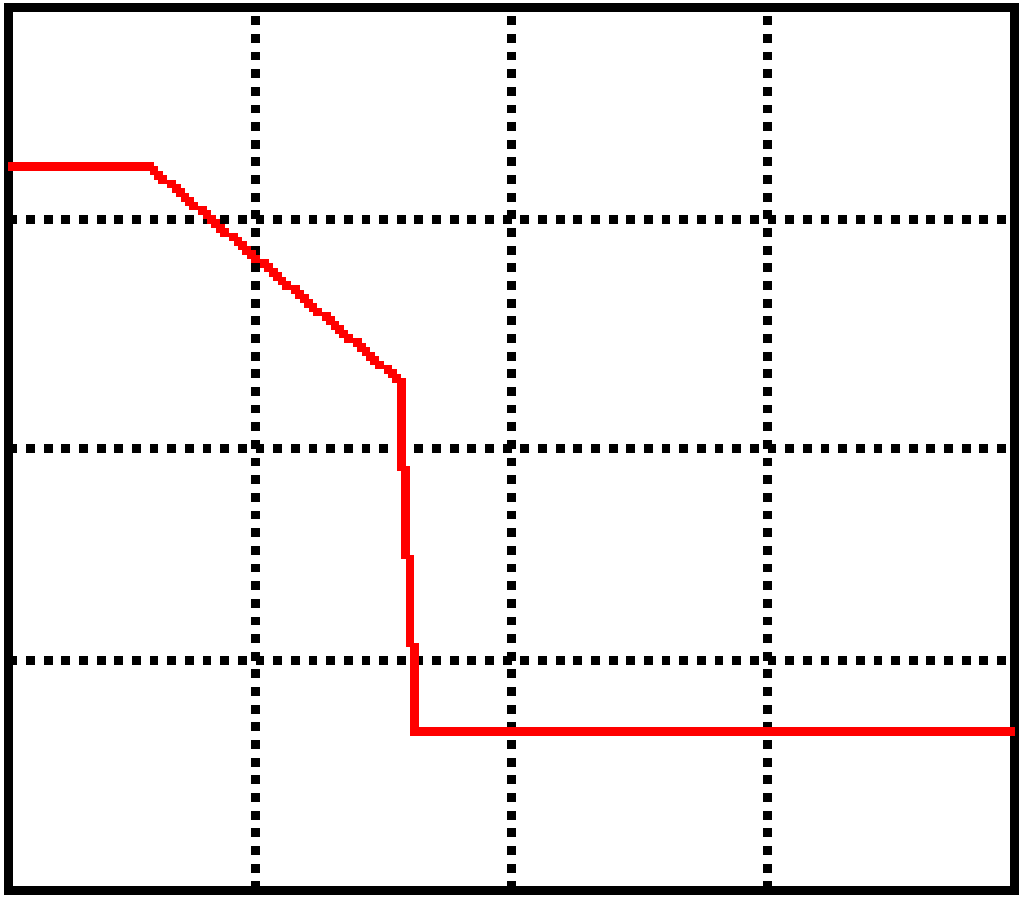
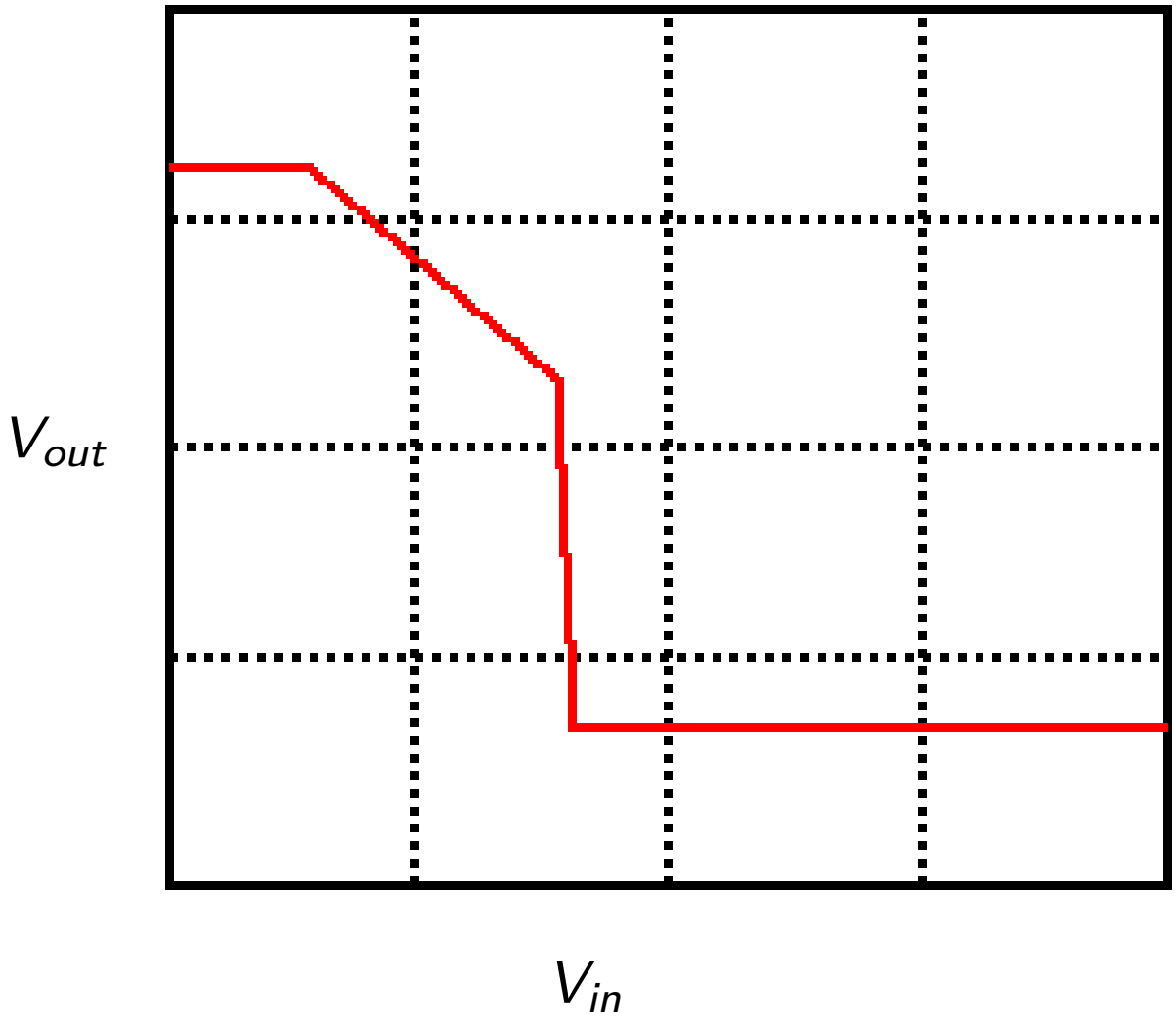
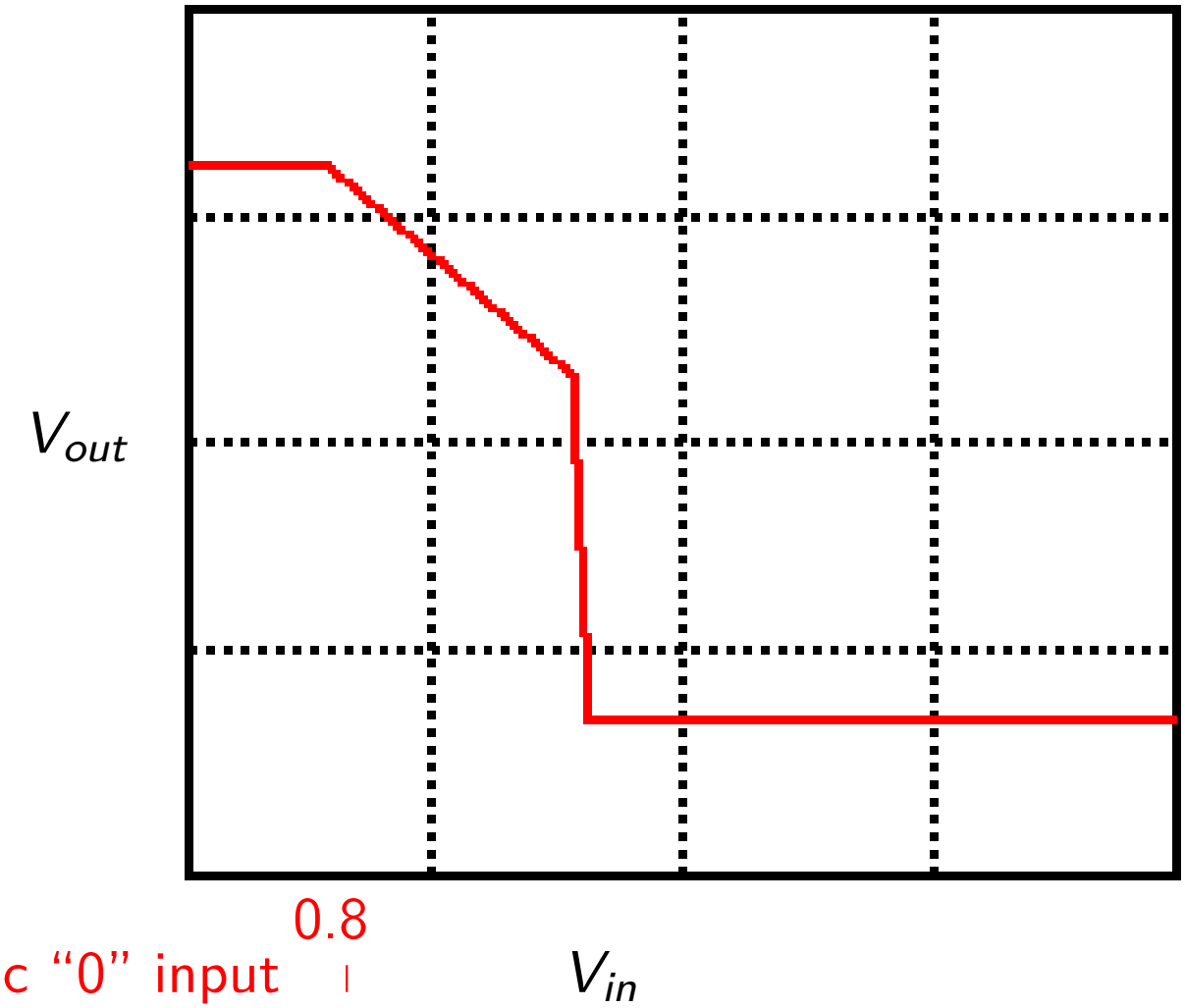
(The output shown is for an LSTTL *inverting* gate.)

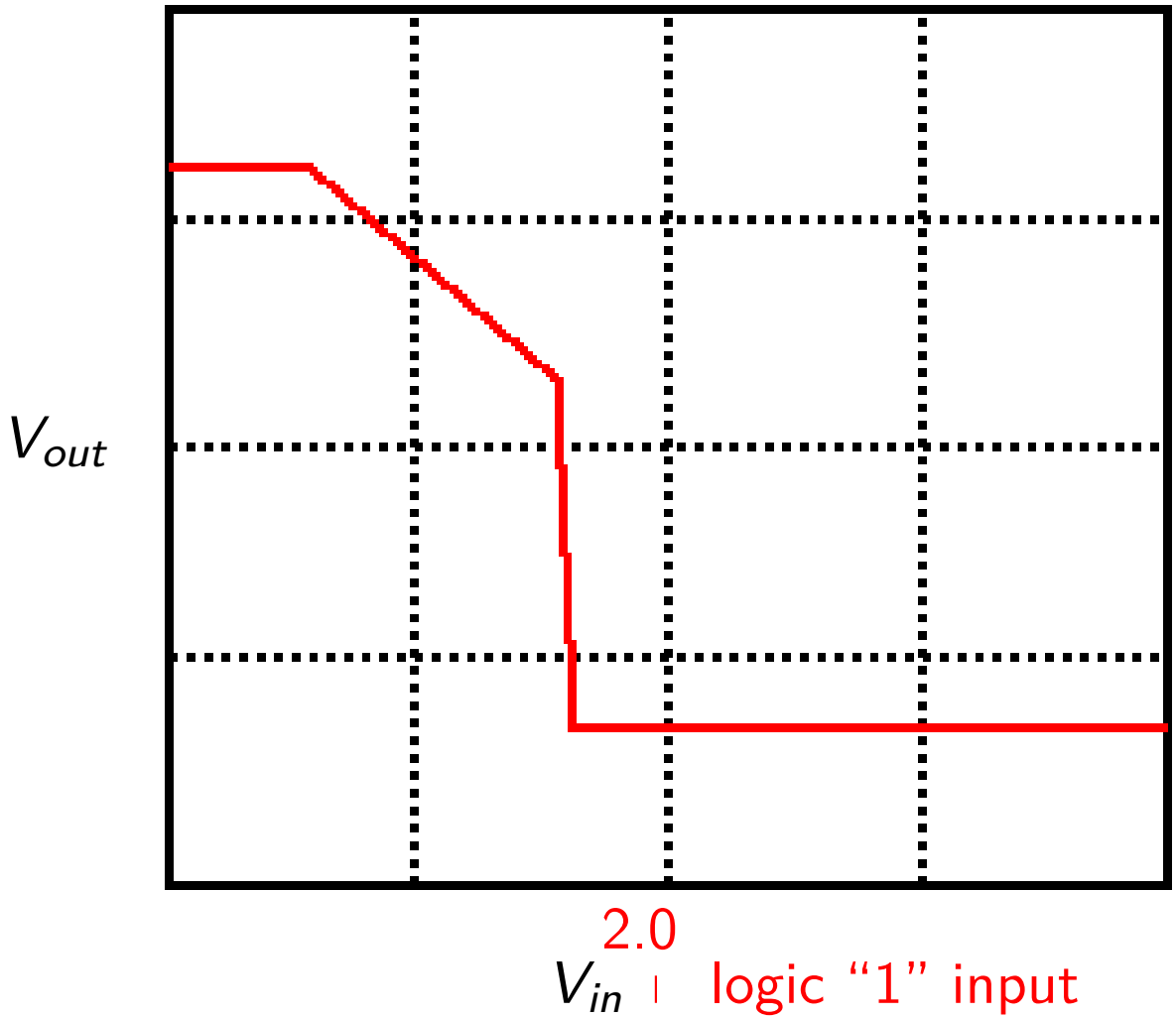


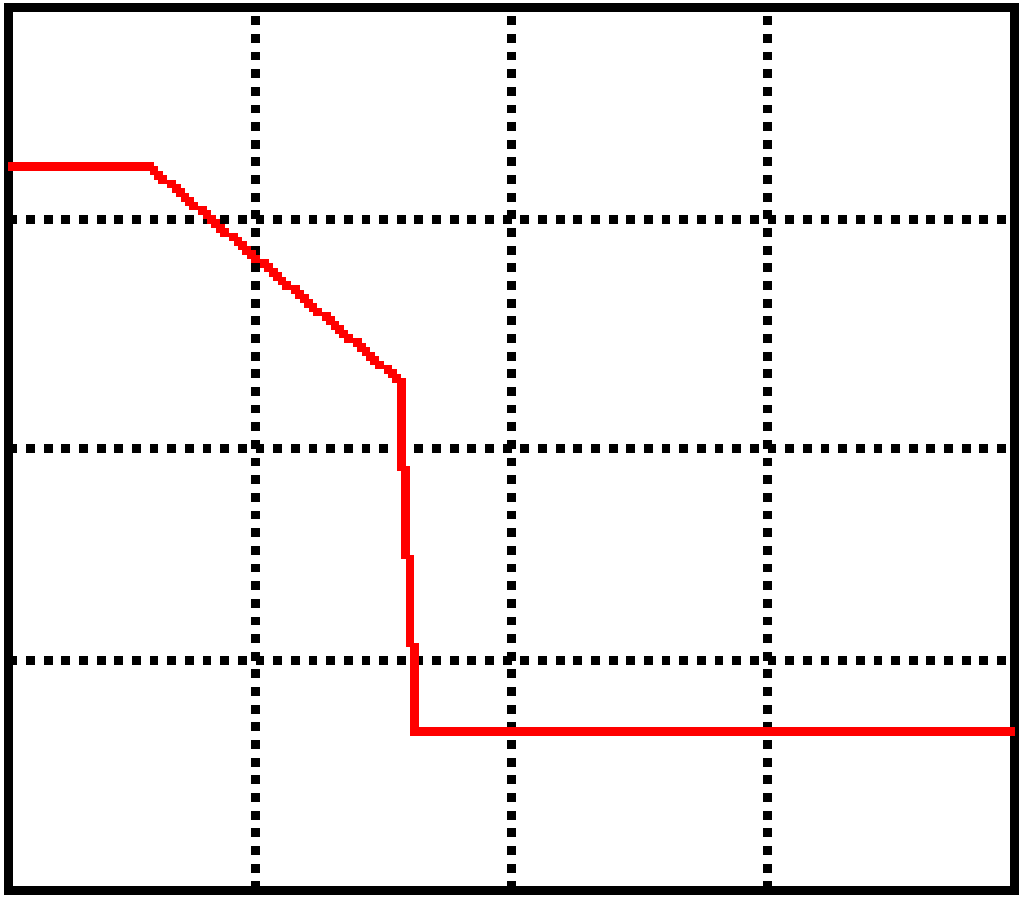


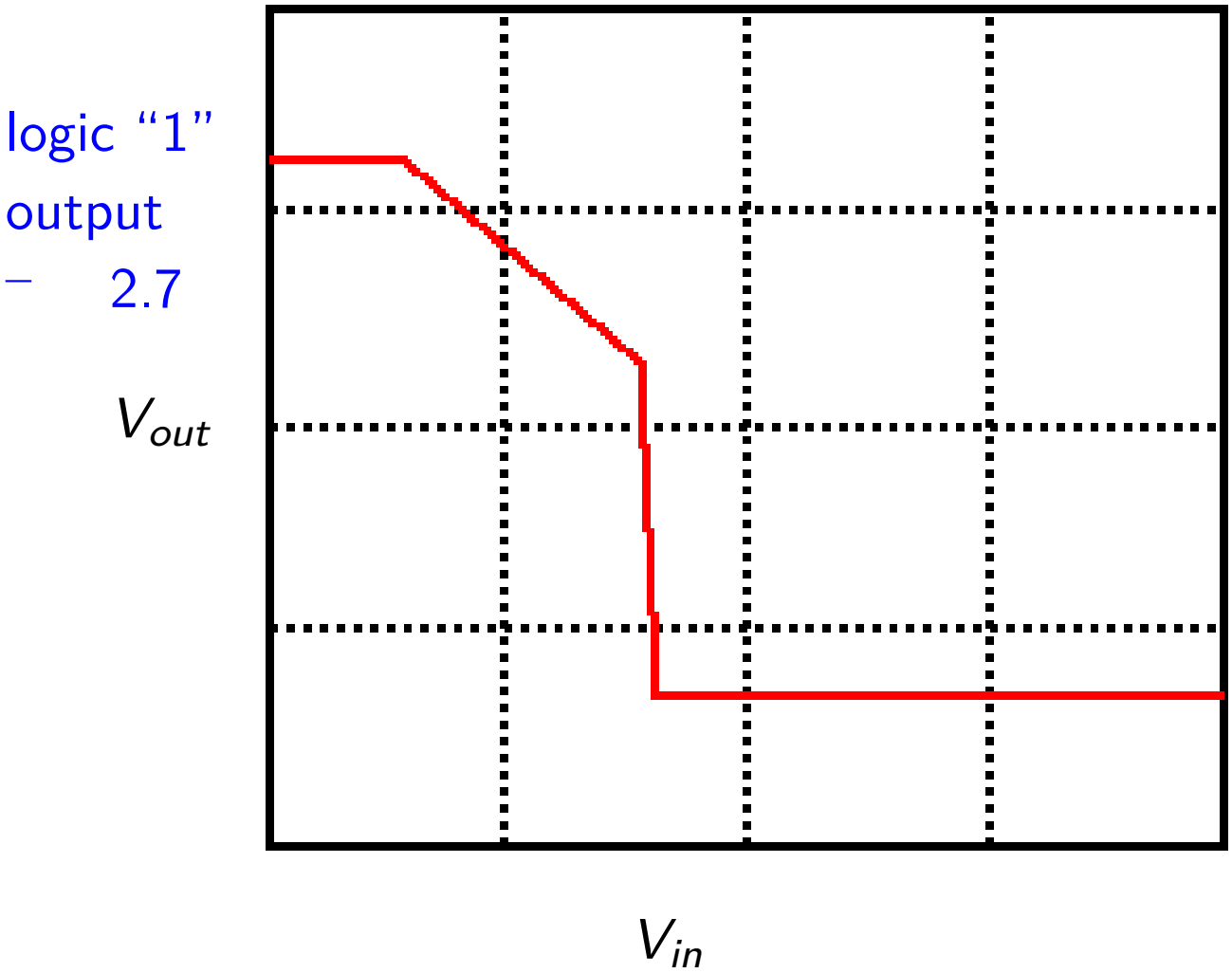
V_{in}


V_{out}
V_{in}


V_{out}
0.8
logic "0" input
V_{in}


V_{out}
2.0
V_{in}
logic "1" input


V_{out}
– 0.5
logic "0"
output
V_{in}


logic “1”
output
–
2.7
V_{out}
V_{in}

This is called the **transfer characteristic** of the gate.

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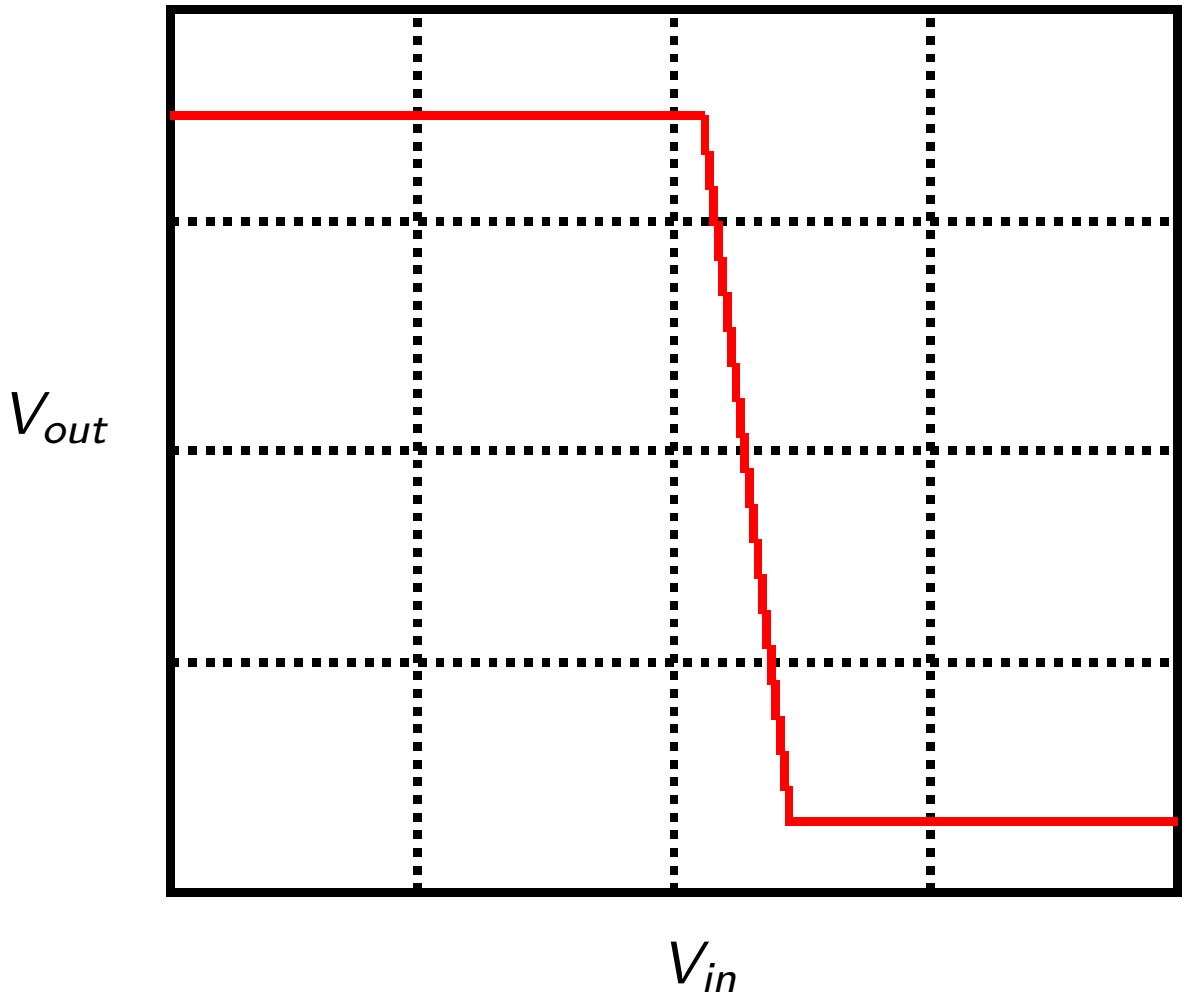
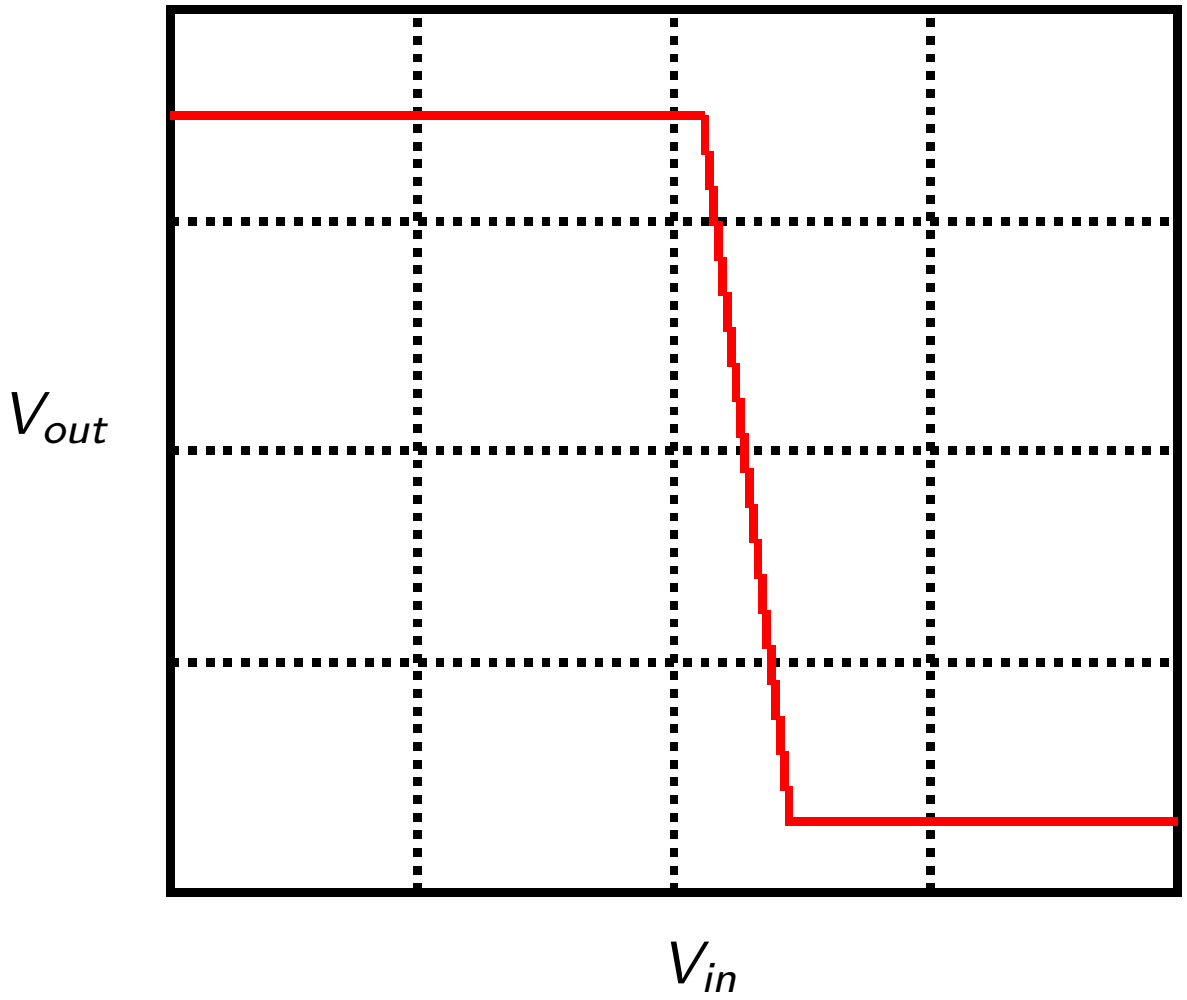
Note that the input voltage, $\mathrm{V_{in}}$, is on the X axis and the output voltage, $\mathrm{V_{out}}$, on the Y axis.


V_{out}
V_{in}



CMOS will look slightly different.

Measuring Output Voltage Limits

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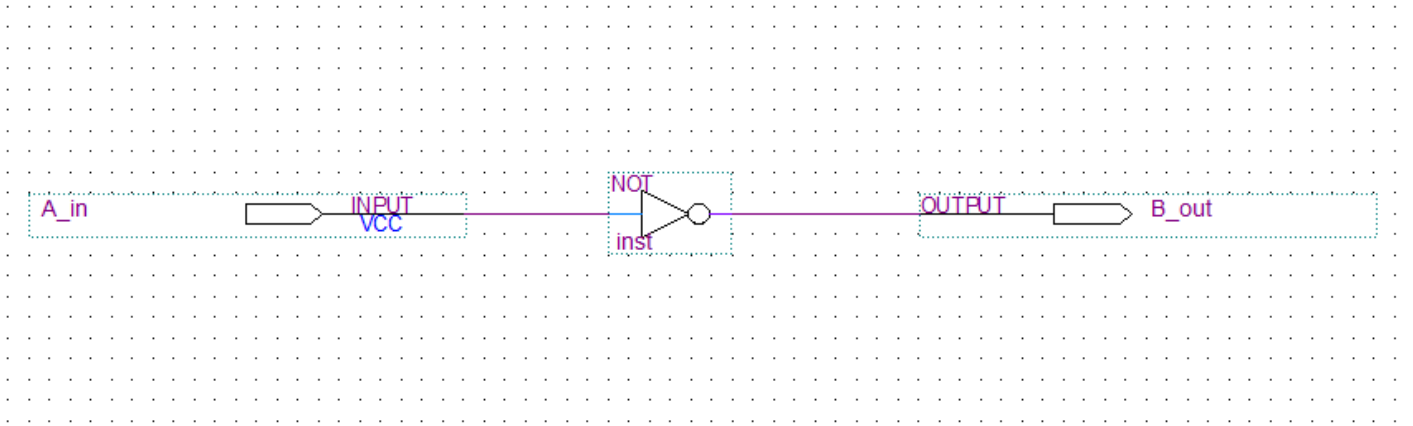
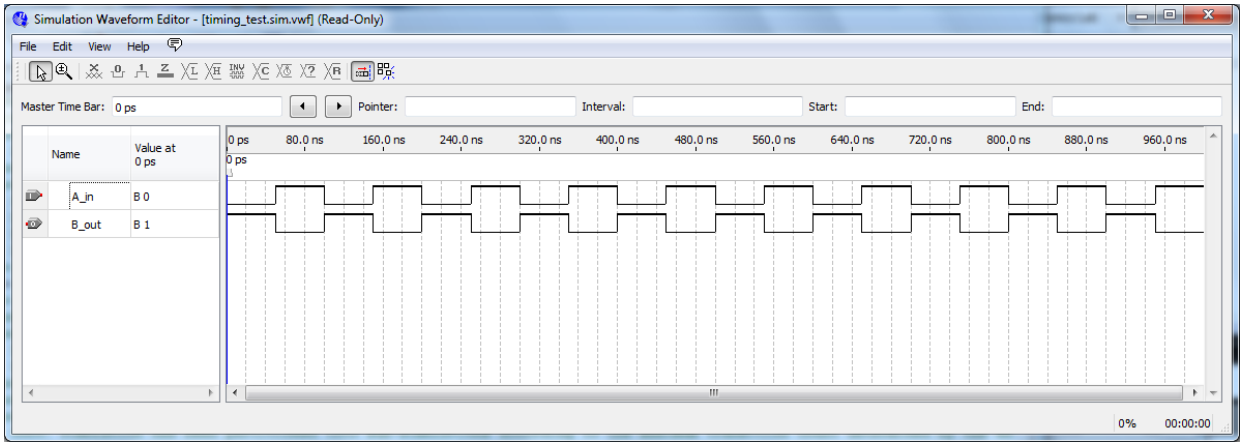
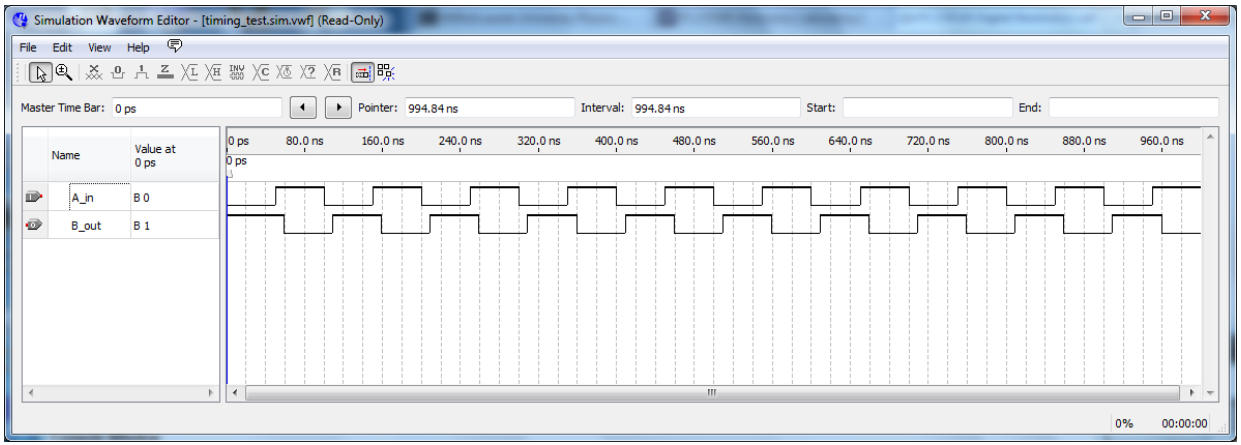


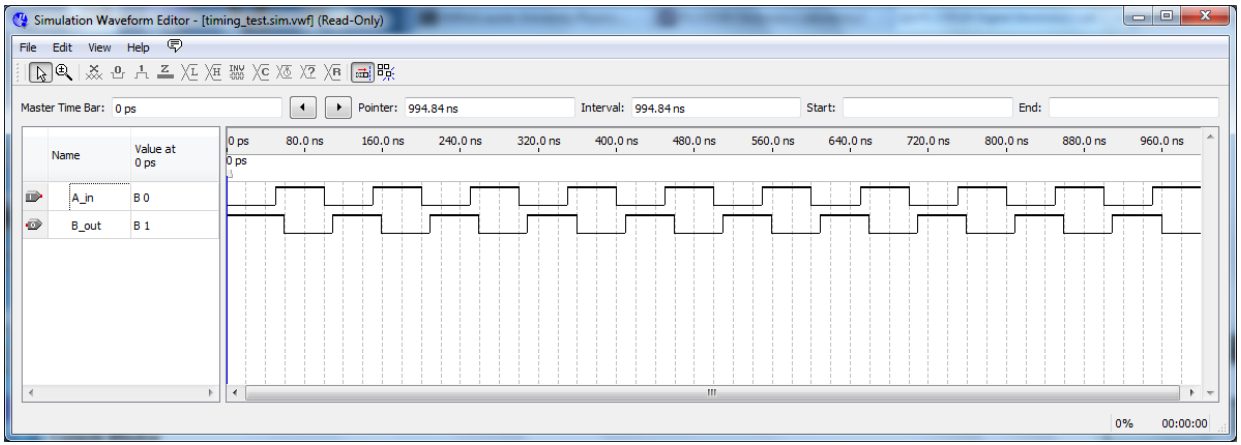
Here's a very simple circuit; a single inverter.



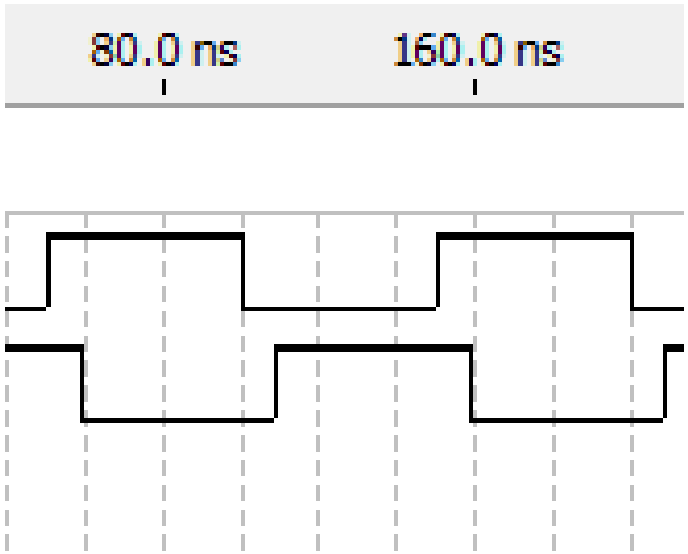
This is what you *expect* the output to look like...



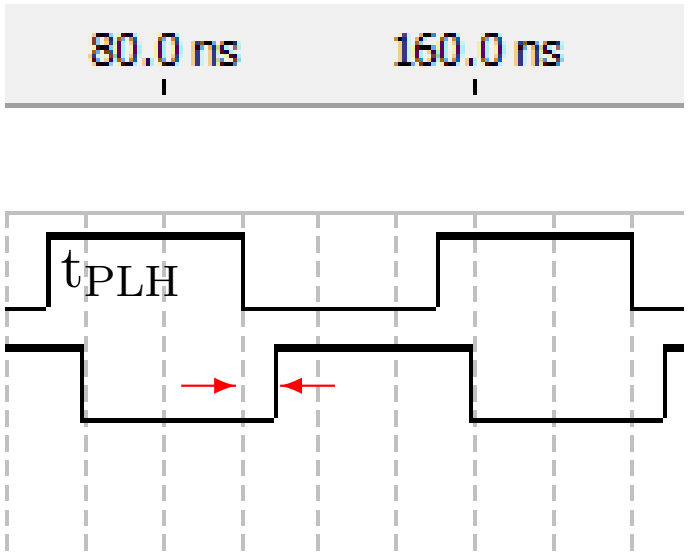
This is what the output *actually* looks like.



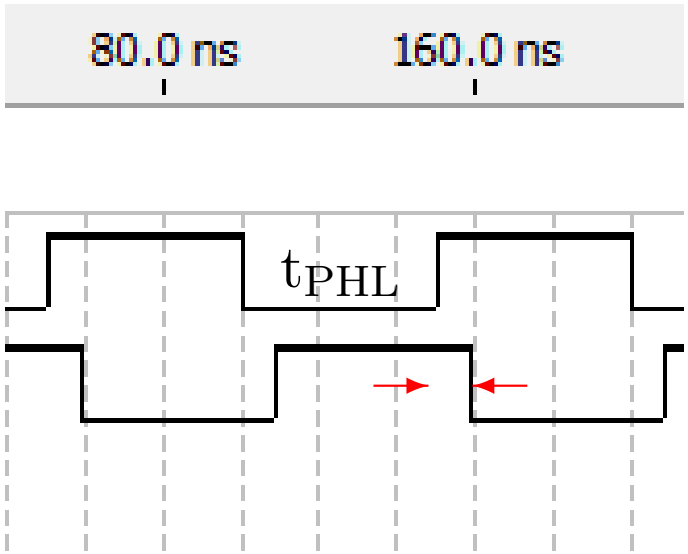
Note the output is shifted right due to the **propagation delay** of the gate.



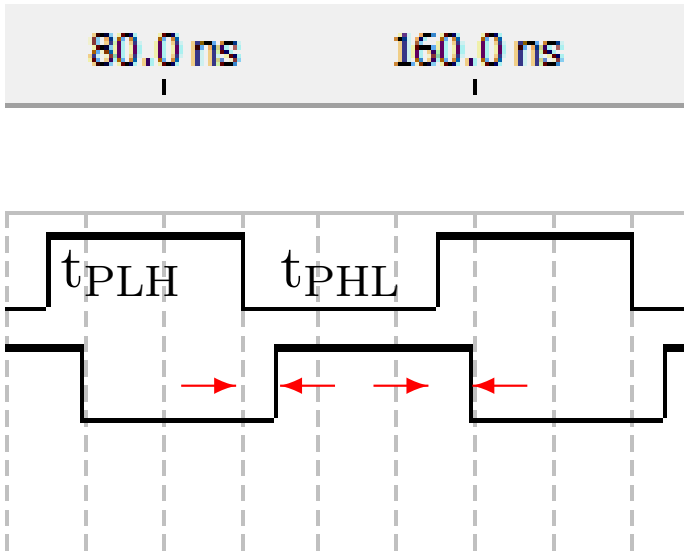
Zoomed in, the delay is around 10 nS.



Here the output is going from LOW to HIGH.



Here the output is going from HIGH to LOW.



In general, the two delays needn't be the same.

Timing Limits

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In general, the delay may be different depending on whether the gate's output is going from low to high or from high to low.
Furthermore, the transitions themselves are not instantaneous, so they are defined as being at the 50% point of the voltage transitions.
Thus there are two quantities of interest:

- t_{PLH}

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  the time interval between the change of an input and the resulting change in output, when the *output* must change from low to high.

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- t_{PHL}

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  the time interval between the change of an input and the resulting change in output, when the *output* must change from low to high.

- t_{PHL}

  the time interval between the change of an input and the resulting change in output, when the *output* must change from high to low.

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Note that in both cases above, the direction of the *input* transition is immaterial.

Measuring timing limits

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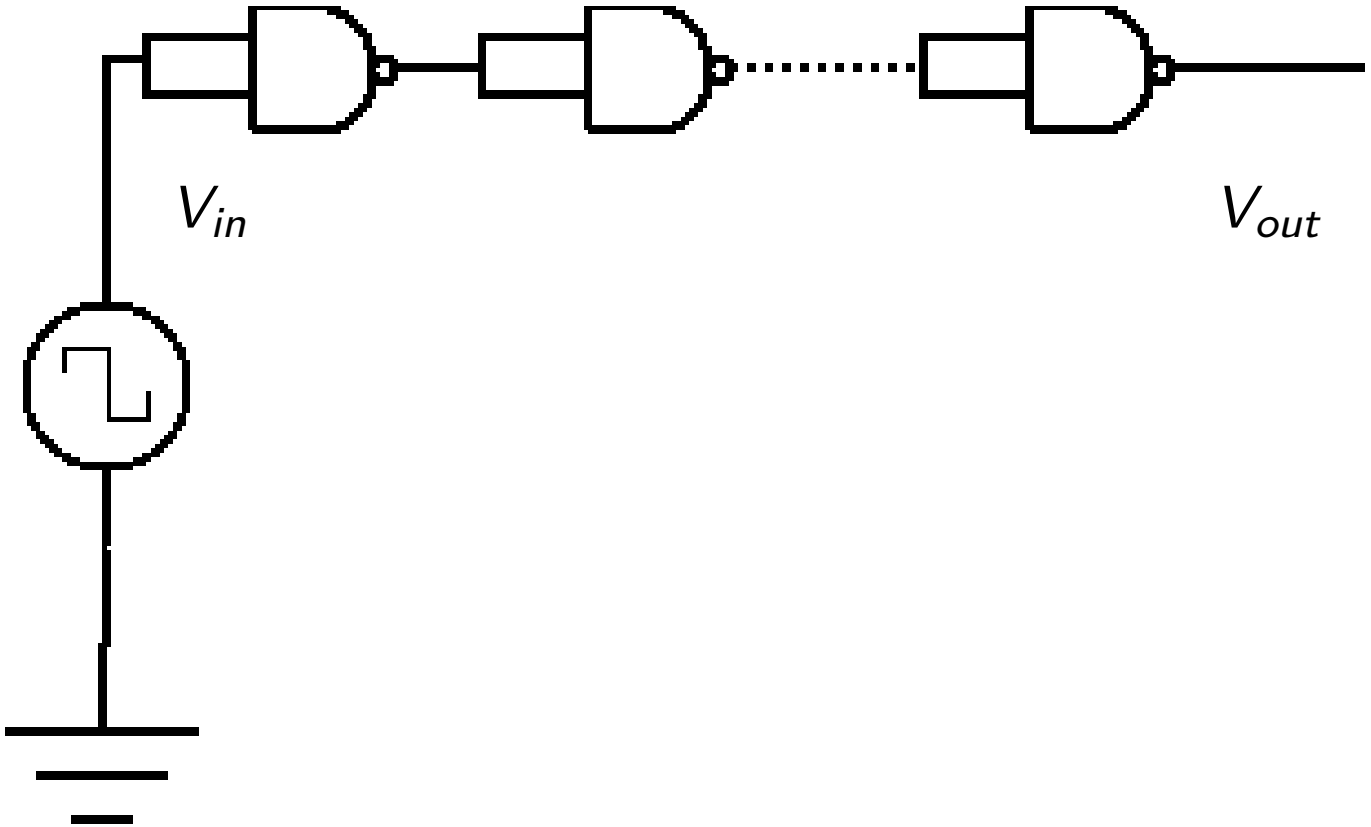
In order to measure timing limits, you can wire up the circuit as in the following figure and use the oscilloscope to measure $\mathrm{V_{in}}$ and $\mathrm{V_{out}}$.


V_{in}
V_{out}

If necessary use a **Schmitt Trigger** on the clock to provide good square wave pulses.

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Use a chain of gates (n $= 8$) as shown to determine the propagation delay $\mathrm{t_p}$ of a given family.
Why can we not measure both $\mathrm{t_{PHL}}$ *and* $\mathrm{t_{PLH}}$ *from the circuit shown?*

In order to obtain a good measurement of the delay time, a frequency of operation should be chosen sufficiently high so that the total delay in the chain ($\mathrm{nt_p}$) is comparable to the period of the input clock.

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The propagation delay of a CMOS gate is not only a function of the load capacitance but also the supply voltage $\mathrm{V_{DD}}$.