Electronics
Logic Gate Characteristics: Current

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Current convention

By convention, current into a chip is positive, so current out of a chip is negative.

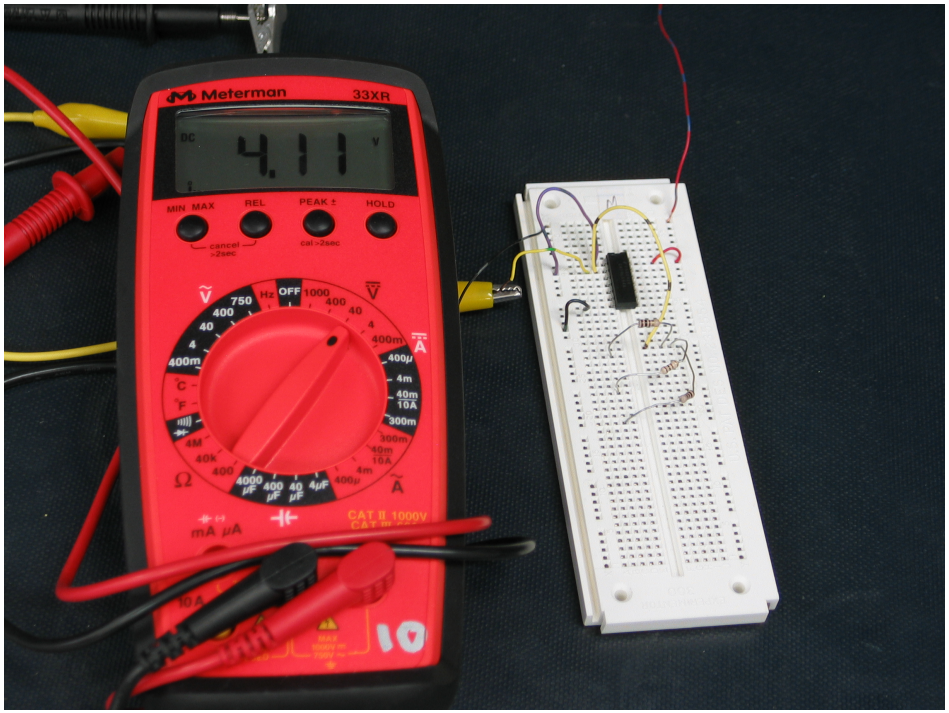
Operating current limits

Gates have current limits as well as voltage limits.

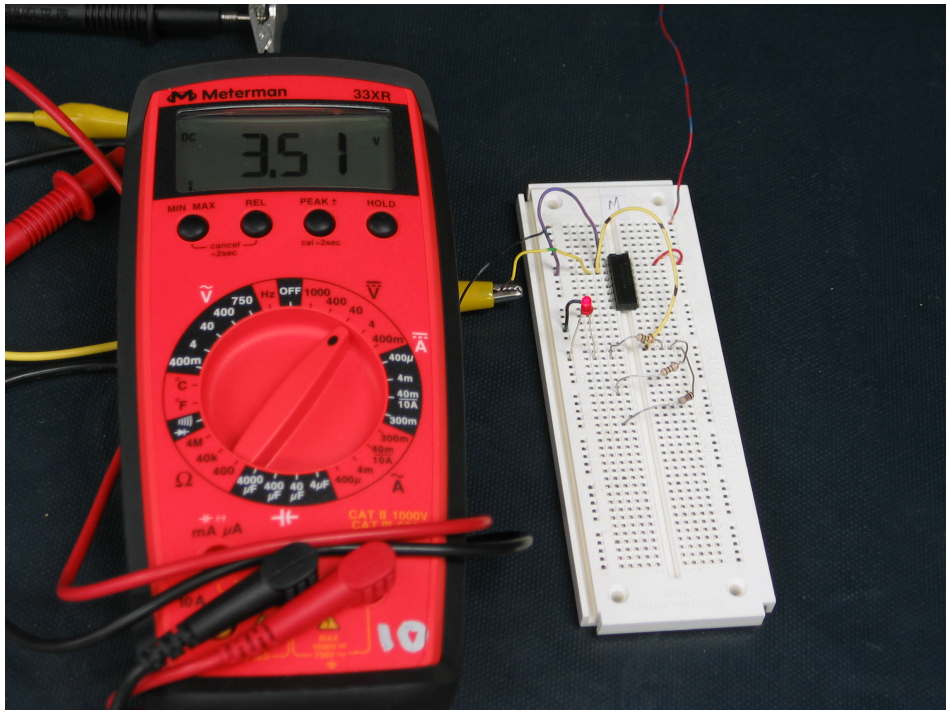
There are limits to the input and output currents of each individual gate.

In addition, there is some current required by the chip itself, as long as power is applied.

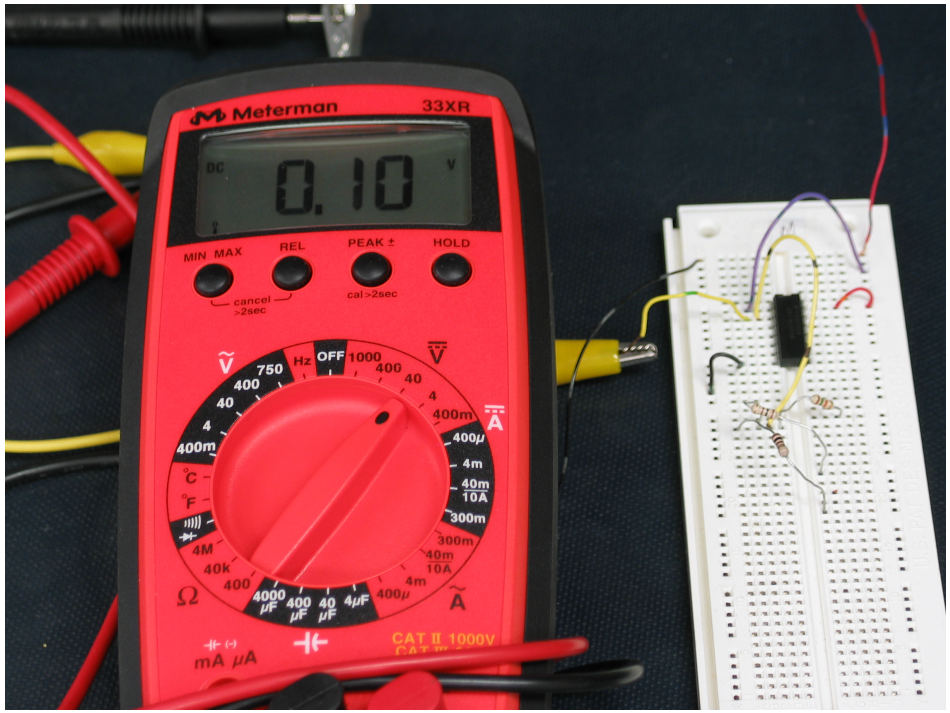
Output current limits; example



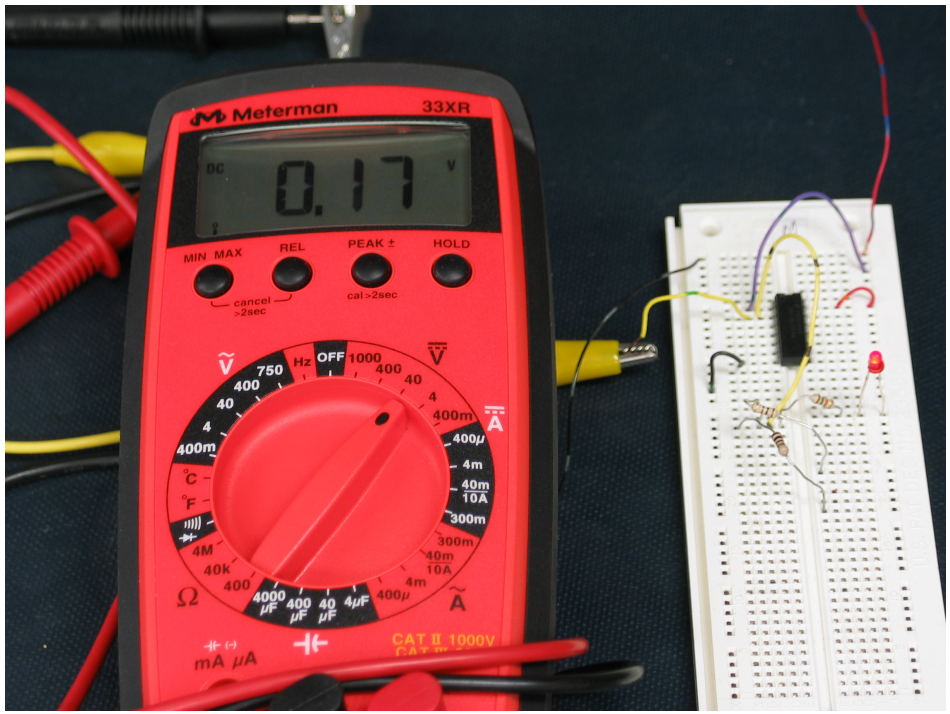
Here's a TTL gate (LS04) producing a HIGH output with no load.



With an LED with a $5.1k\Omega$ resistor, the output voltage has dropped.



Here's the same TTL gate (LS04) producing a LOW output with no load.



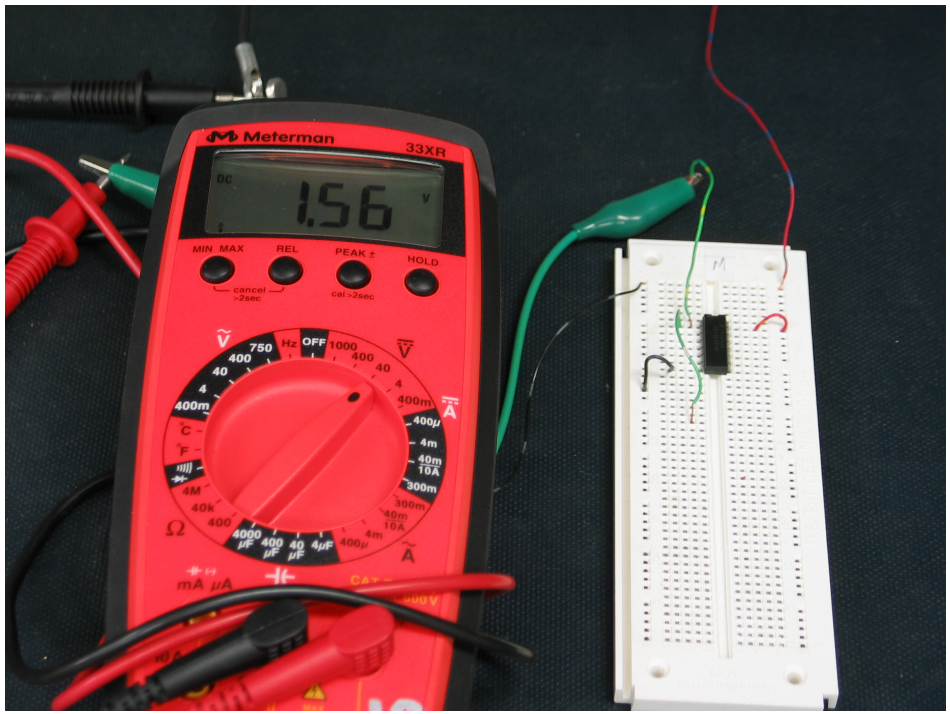
With an LED with a 5.1$k\Omega$ *pull-up* resistor, the output voltage has risen.

Input current requirements

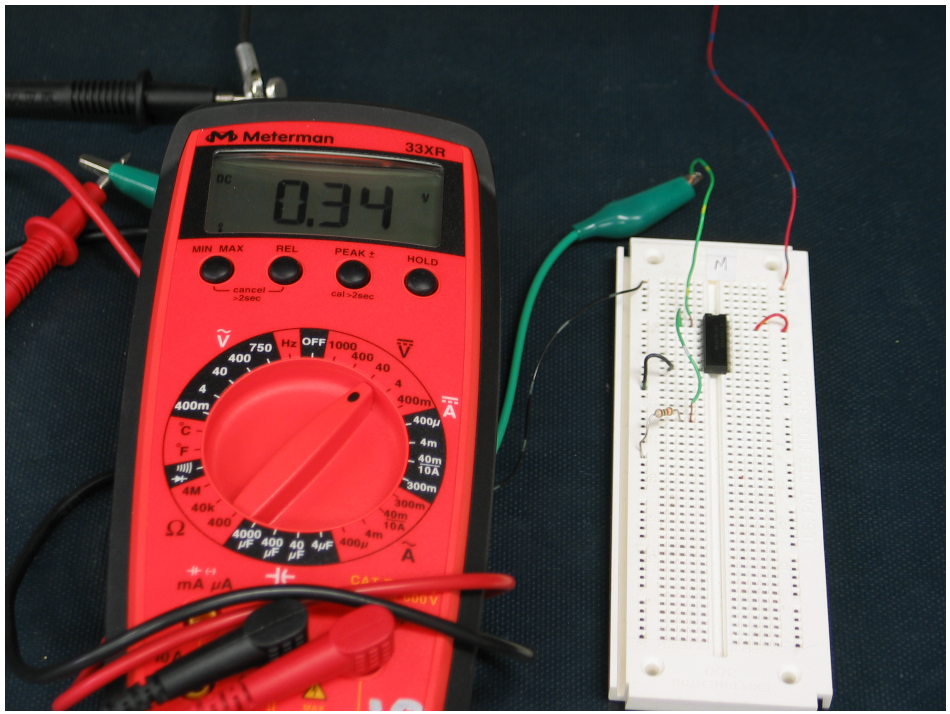
When the inputs of a gate are unconnected, they are neither HIGH nor LOW.

They are said to be **floating**.

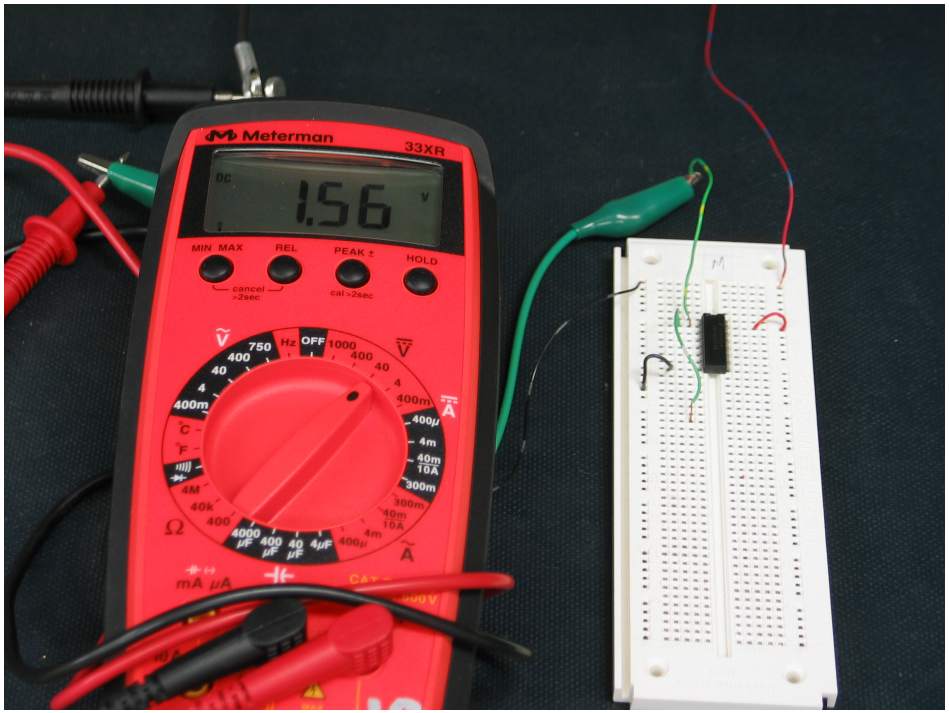
Input current limits; example



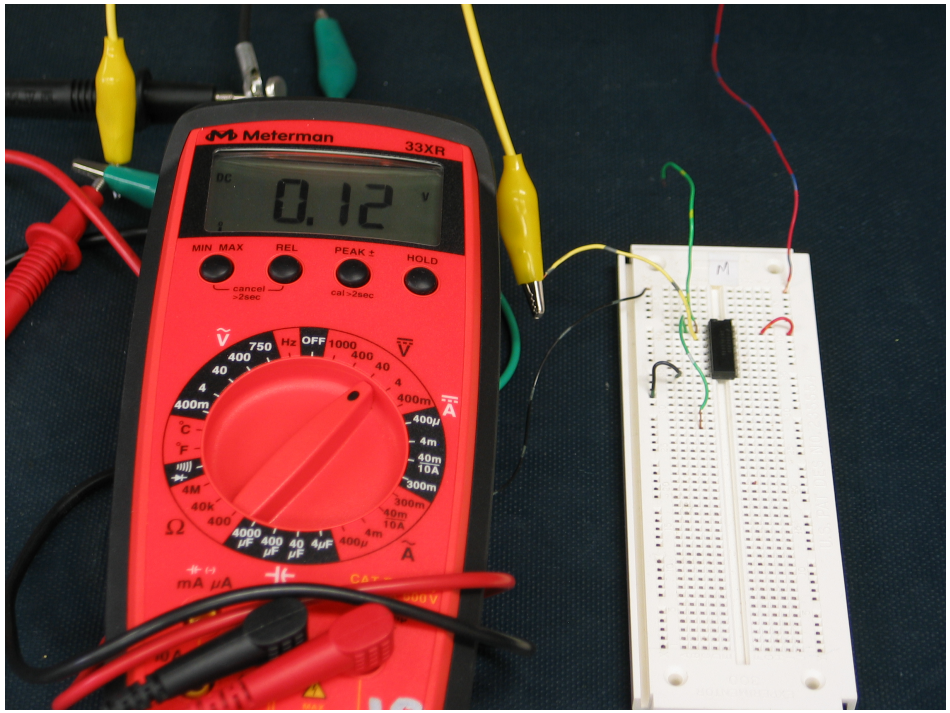
Here's the voltage on the input of a TTL gate (LS04) when left floating.



With a $5.1k\Omega$ resistor to GROUND the input **is** a valid LOW.



What's the output when the inputs are floating?



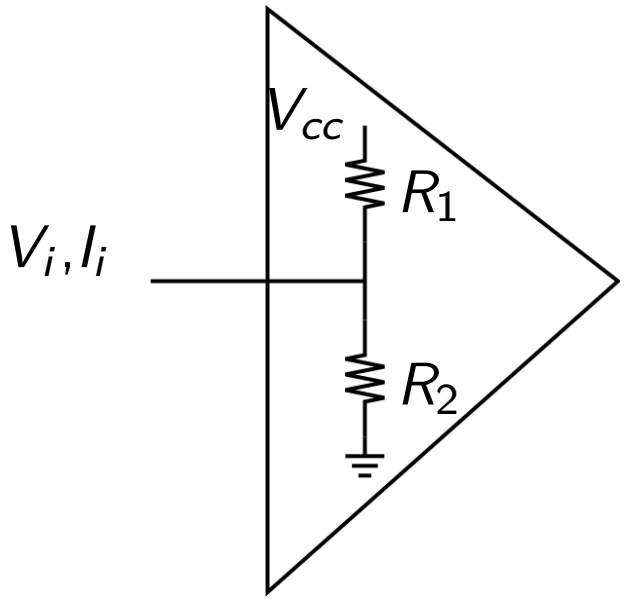
The output (in this case) is a valid LOW, *as though* the input were a valid HIGH.

Output current limits; Connecting gates

When the output of one gate is used as the input of another gate, the *output* section of the first gate must source (or sink) enough current so that the *input* voltage of the second gate is within the proper range.

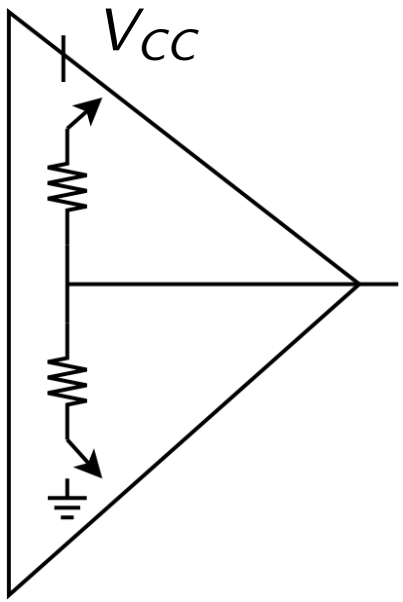
The output of different types of gates is more similar than the inputs functionally, and an equivalent circuit is given in the following figure.

TTL input current limits



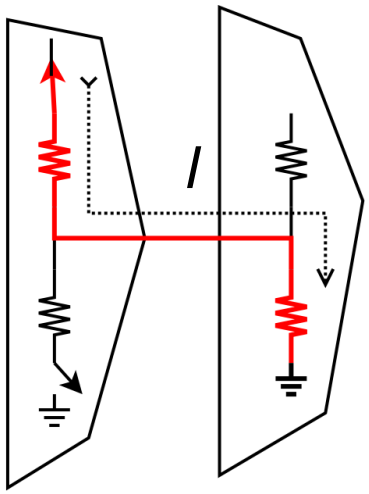
This is an equivalent circuit for a TTL gate *input*.

TTL connections



This is an equivalent circuit for a gate *output*.

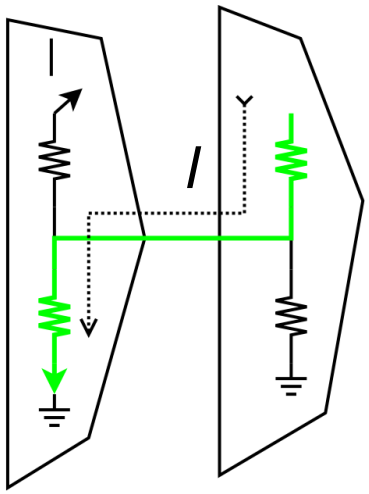
Here's what happens when a TTL HIGH output feeds into another TTL input.



Current flows *out of* gate

Voltage must stay above $V_{IH_{min}}$

Here's what happens when a TTL LOW output feeds into another TTL input.



Current flows *into* gate

Voltage must stay below $V_{IL_{max}}$

The input to a logic gate is not like an ideal voltmeter.

Consider the equivalent circuit shown in the following figure.

The actual voltage going into the gate, V_i, depends on the current input like this:

$$V_i = \left(\frac{V_{cc} - V_i}{R_1} + I_i \right) R_2$$

and thus

$$V_i = \left(V_{cc} \frac{R_2}{R_1} + I_i R_2 \right) \frac{R_1}{R_1 + R_2}$$

(Note that in order to make V_i low, I_i will have to be negative.)

TTL

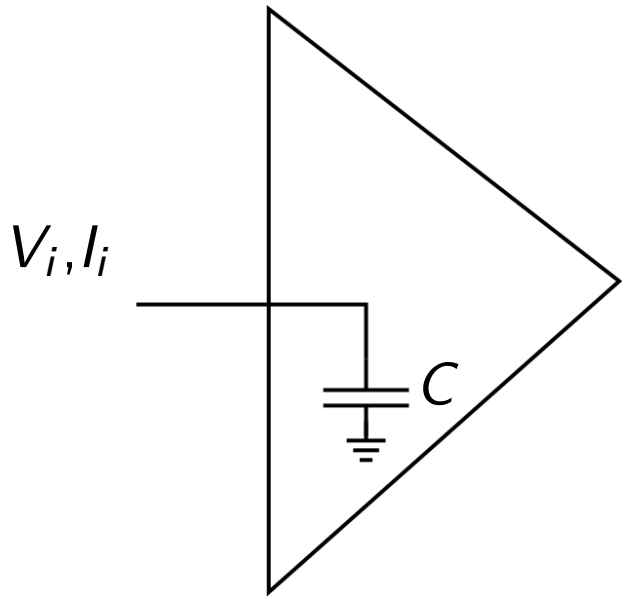
For TTL, the amount of current drawn by producing a high output is not the same as the amount drawn by a low output.

Thus there are two quantities, I_{CCH} and I_{CCL}.

Since CMOS is based on FETs rather than BJTs, the input current required is very small, but the input capacitance of the gate must be considered.

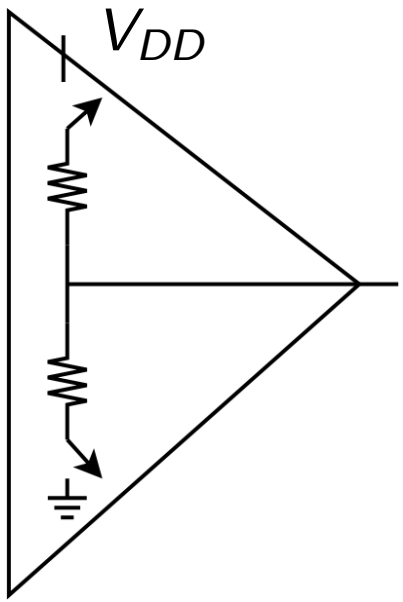
The following figure shows the equivalent circuit for a CMOS input.

CMOS input current limits



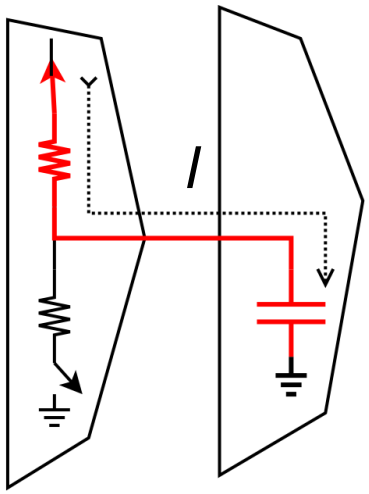
This is an equivalent circuit for a CMOS gate *input*.

CMOS connections



The equivalent circuit for a CMOS *output* is similar to TTL.

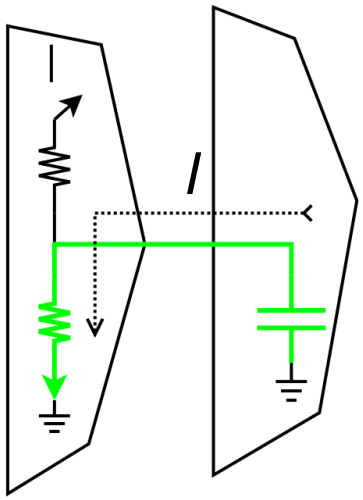
Here's what happens when a CMOS HIGH output feeds into another CMOS input.



Current flows *out of* gate

Voltage must rise above $V_{IH_{min}}$

Here's what happens when a CMOS LOW output feeds into another CMOS input.



Current flows *into* gate

Voltage must fall below $V_{IL_{max}}$

For CMOS, even though the output equivalent circuit is similar to that of a TTL gate, when one gate is connected to another there is a limit to the *speed* at which the second gate will change due to the time it takes for the input capacitor to charge or discharge.

Since the gate input is capacitive, then the current drawn from the previous gate will start big and get smaller as the capacitor reaches its intended voltage.

CMOS

For CMOS, the symmetry of the internals means that the current needed to produce a high output is the same as the amount drawn by a low output.

Thus there is only one quantity, $I_{DD_{max}}$

Total power consumption

The power consumption of the device is given by

$$P = V_{supply} \times I_{total}$$

where I_{total} is the sum of the currents drawn by each of the gates on the device.

The power drawn by a circuit is the sum of the power drawn by each device in the circuit.

The supply must be able to provide as much as needed by the whole circuit.

Quiescent current

As long as power is applied to a chip, it will be drawing a small amount of current.

Definition of terms can sometimes become tricky.

An output limit, for instance, can be seen as either how much is guaranteed to be *supplied*, or as how much can be safely *demanded*.

In other words, the limit can be seen as either belonging to the *device* or the the *surrounding* circuit.

While they are functionally equivalent, the first view will give a *minimum* for a quantity while the second will give a *maximum*.

Different manufacturers may take either view, and so it is important to understand this so that you can make sense of whichever you are given.

Four particular quantities are of interest in specifying the tolerance:

1. $I_{IL_{max}}$

   the *maximum* input current which must be drawn from a gate's input to ground to guarantee the input will be low.

2. $I_{IH_{max}}$

   the *maximum* input current which must be supplied to a gate's input to guarantee the input will be high.

3. $I_{OH_{max}}$

   the *maximum* current which the gate can source through its output and still keep the output high.

4. $I_{OL_{max}}$

   the *maximum* current which the gate can sink through its output and still keep the output low.

$I_{IL_{max}}$ and $I_{IH_{max}}$ may require some explanation.

Most people assume that if the inputs of a gate are not attached to anything they will be treated as logic low.

This is a bad assumption.

An important piece of information about various logic families is what happens when inputs are left to **float**; i.e. remain unconnected.

They may float high, low or anywhere in between.

To have an input recognized as something other than its "floating" state will require that a finite amount of current be either supplied to the input (to make it high) or drawn from the input to ground (to make it low.)

Never assume anything about unconnected inputs.

If you want them to be in a particular state, tie them that way.

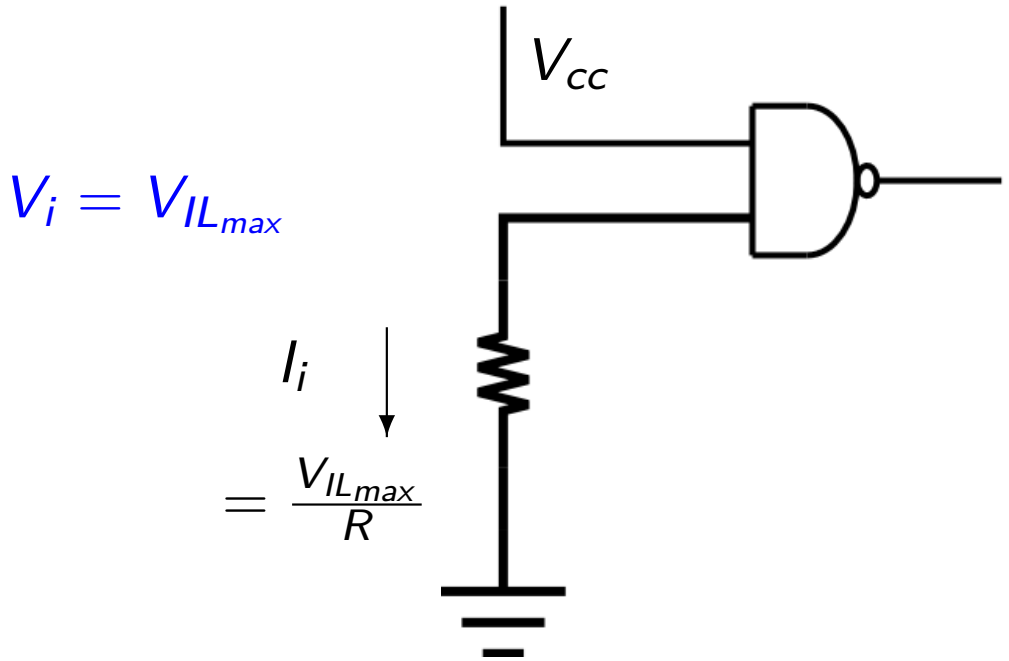
These current limits are referred to as the *fan–in* and *fan–out* characteristics of digital circuits.

Note that a given gate will occasionally have zero for either $\mathrm{I_{IL_{max}}}$ *or* $\mathrm{I_{IH_{max}}}$.

Floating inputs

If the input floats HIGH, then current will need to be drawn *to* ground to make it LOW.

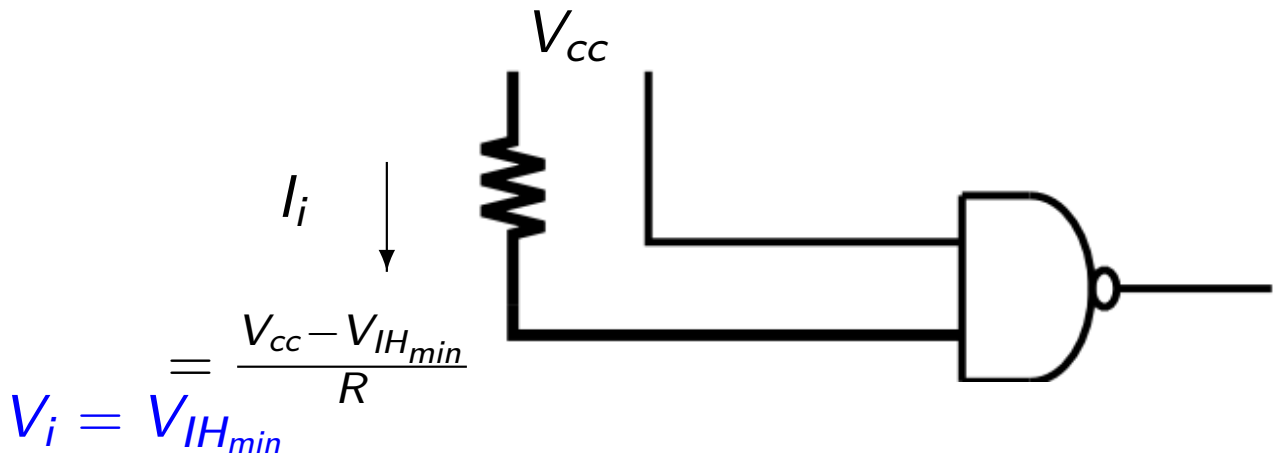
Input floating HIGH



The current *limit* is when $V_i = V_{IL_{max}}$.

If the input floats LOW, then current will need to be drawn *from* V_{cc} to make it HIGH.

Input floating LOW



The current *limit* is when $V_i = V_{IH_{min}}$.

In order to measure the input requirements for a gate, you could wire up the first circuit of the previous figure.

An oscilloscope could be used to measure $\mathrm{V_{in}}$ and $\mathrm{V_{out}}$.

Since one end of R is tied to a known voltage, and the other end is connected to the oscilloscope, then the voltage across R is known, and thus the current through R can be calculated using Ohm's Law.

With nothing connected to the inputs of a gate, so there is no current in, you may observe its output.

If the inputs of a device "float" so that they appear to be in a particular state with nothing connected, then by definition you don't need to supply *any* current to keep them in that state!

Actually it can be more complicated than that.

Sometimes the inputs float to voltage which is in the indeterminate region, so that sometimes they will appear to be high and other times they will appear to be low.

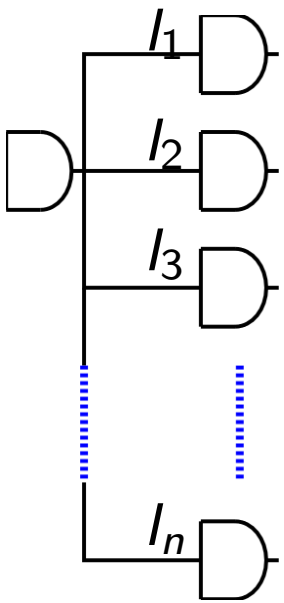
Starting with the lowest current possible, in the first circuit above, if you monitor the value of $\mathrm{V_{out}}$ as current is increased, you can determine when the output voltage just reaches the specified value of $\mathrm{V_{OL_{max}}}$ and thus determine $\mathrm{I_{IH_{min}}}$

Keep in mind the earlier note about whether a limit is called a "maximum" or a "minimum", it will be referred to here as a minimum.

If you wire up the second circuit above and starting with the lowest possible current, monitor the value of $\mathrm{V_{out}}$ as current is increased, you can observe when the output voltage just falls below the specified value of $\mathrm{V_{OH_{min}}}$. and thus determine $\mathrm{I_{IL_{min}}}$.

Fan–out

When one gate feeds into *many* gates, as in the figure below, the the first gate must be able to source (or sink) enough current for *all* of the gates it feeds.



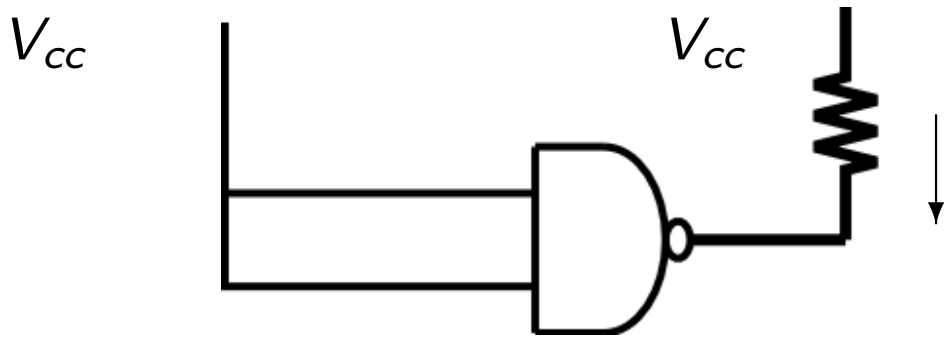
The **fan-out** of a gate is *the number of gates of that family which can be fed by a single gate*.

Keep in mind that the fan-out will be limited by the *lower* of the number for sourcing and sinking, since both must be possible.

CMOS fan–out

For CMOS, adding more gates will change the speed limit of the circuit.

Output low

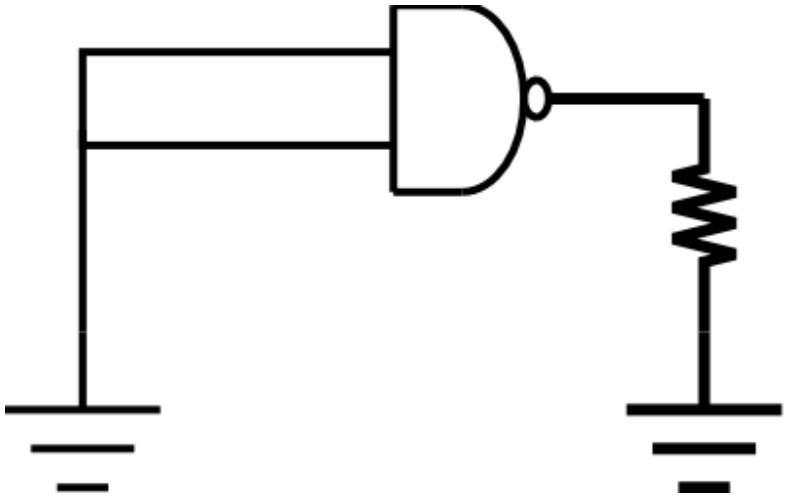


$$I_o = I_{OL_{max}} = \frac{V_{cc} - V_{OL_{max}}}{R}$$

$$V_o = V_{OL_{max}}$$

The current *limit* is when $V_o = V_{OL_{max}}$.

Output High



$$V_o = V_{OH_{min}}$$

$$I_o = I_{OH_{max}}$$

$$= \frac{V_{OH_{min}}}{R}$$

The current *limit* is when $V_o = V_{OH_{min}}$.

In order to measure the output current limits of a device, you can wire up the first circuit above.

The oscilloscope can be used to measure $\mathrm{V_{in}}$ and $\mathrm{V_{out}}$.

Since one end of R is tied to a known voltage, and the other end is connected to the oscilloscope, then the voltage across R is known, and thus the current through R can be calculated using Ohm's Law.

Using the value of the *output* ***sinking*** *current* $\mathrm{I_{OL_{max}}}$ from the data sheets, you can determine the maximum value of current which keeps the output in the low state and thus $\mathrm{I_{OL_{max}}}$.

If you set up the second circuit above, and obtain the value of the *output* ***sourcing*** *current* $\mathrm{I_{OH_{max}}}$ from the data sheets, then you can determine the maximum value of current which keeps the output in the high state and thus $\mathrm{I_{OH_{max}}}$ in a manner similar to the one previously described.

Interfacing families; CMOS to TTL and TTL to CMOS

Because different families have different current and voltage requirements, they can't simply be mixed as though they were all the same.

Each gate must stay within its required operating parameters.