Electronics
Logic Gate Characteristics: Current

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Current convention

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By convention, current into a chip is positive, so current out of a chip is negative.

Operating current limits

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There are limits to the input and output currents of each individual gate.

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In addition, there is some current required by the chip itself, as long as power is applied.

Output current limits; example

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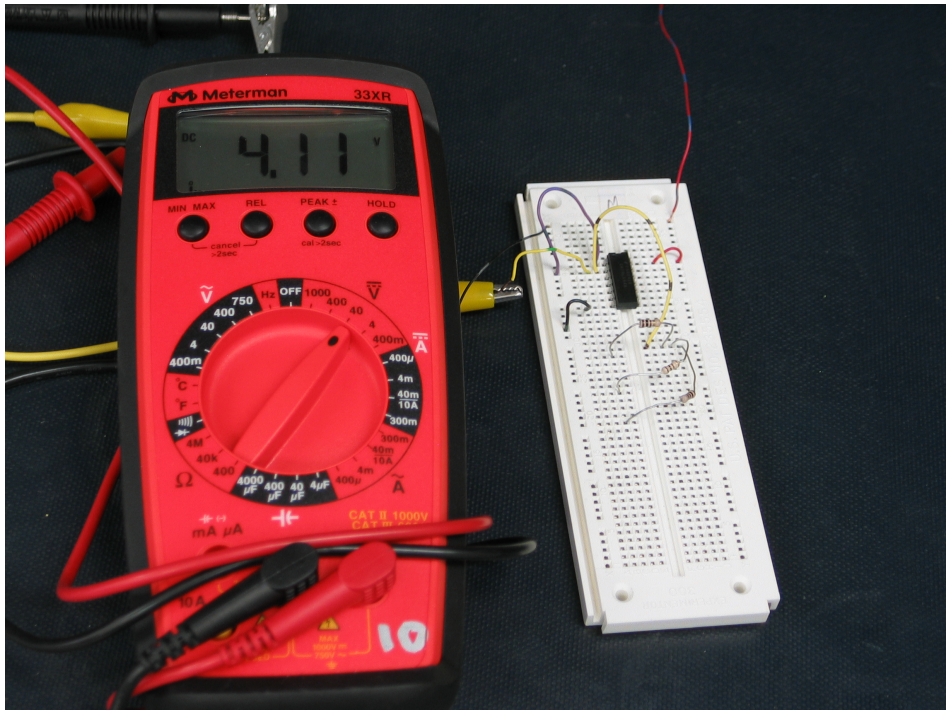
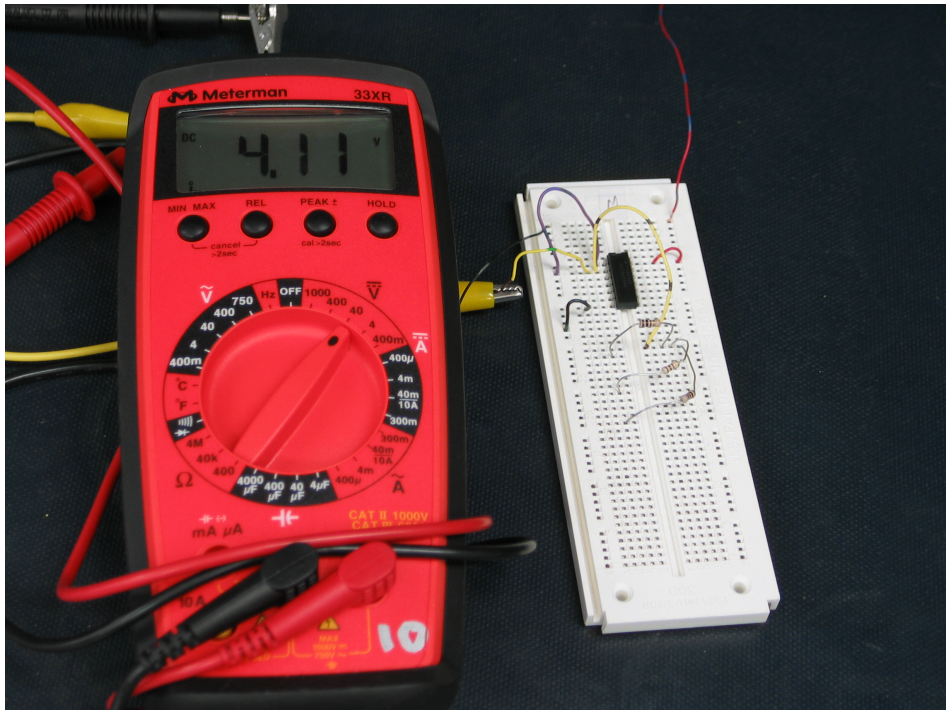
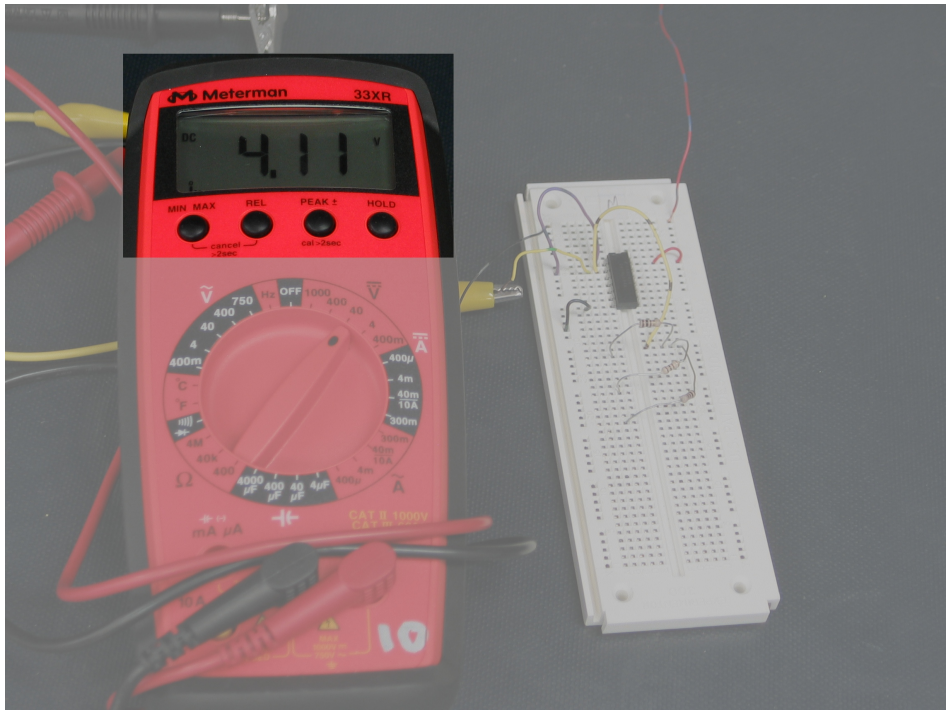


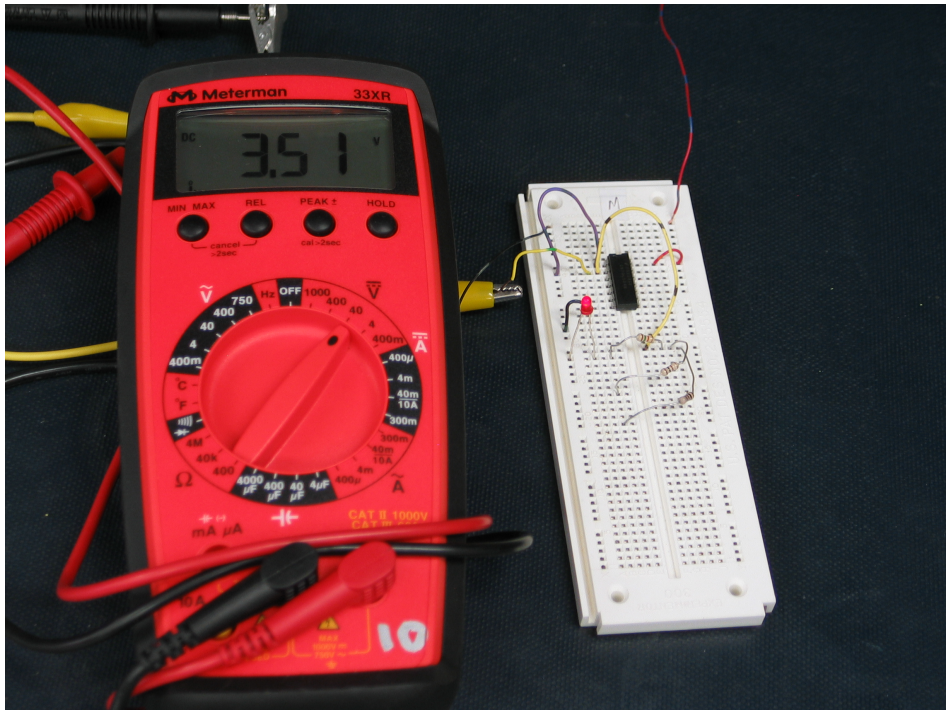
Output current limits; example



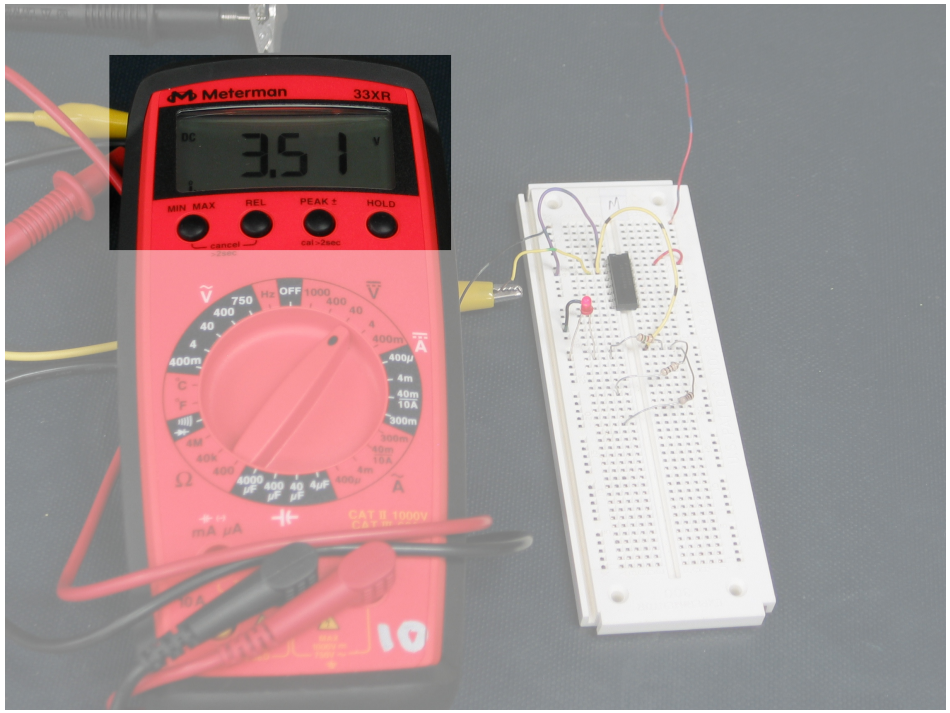
Here's a TTL gate (LS04) producing a HIGH output with no load.



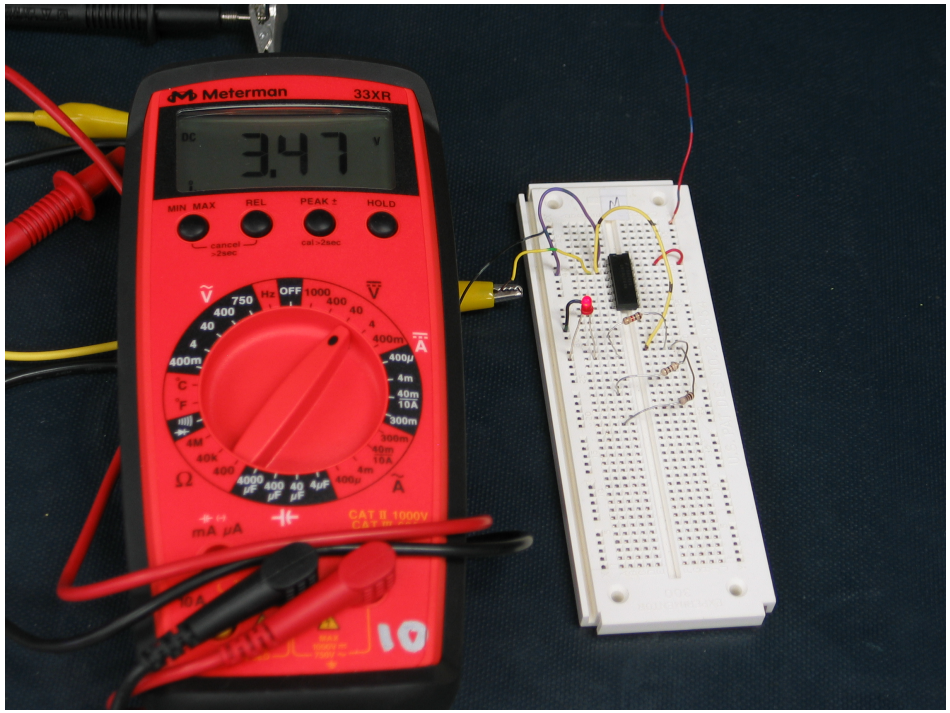
The output voltage with no load is 4.11 Volts.



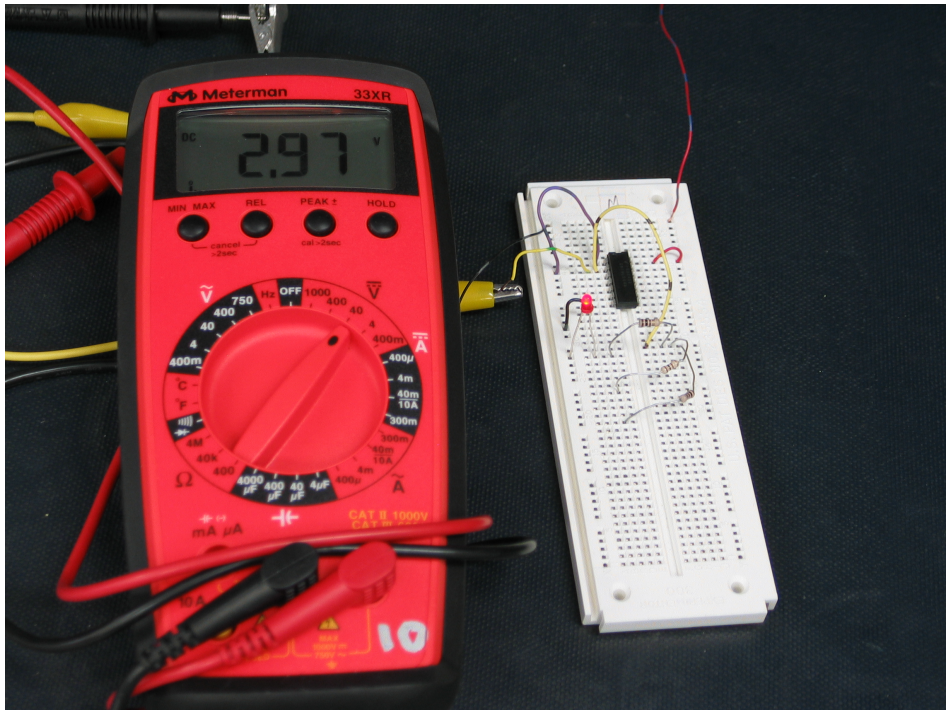
With an LED with a $5.1k\Omega$ resistor, the output voltage has dropped.



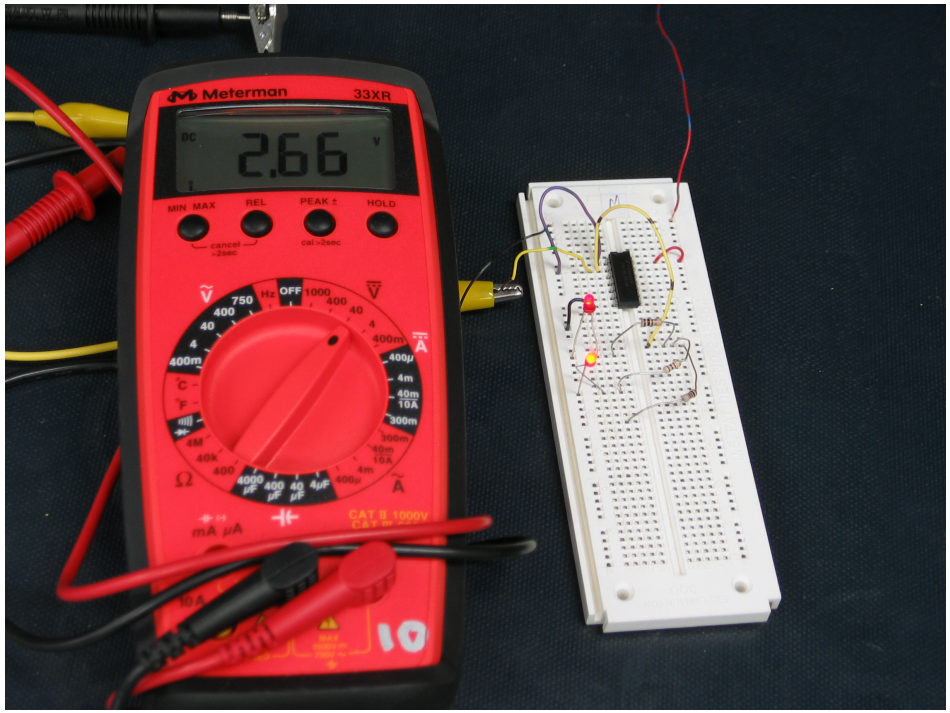
Note that the current being drawn is less than 1 mA.



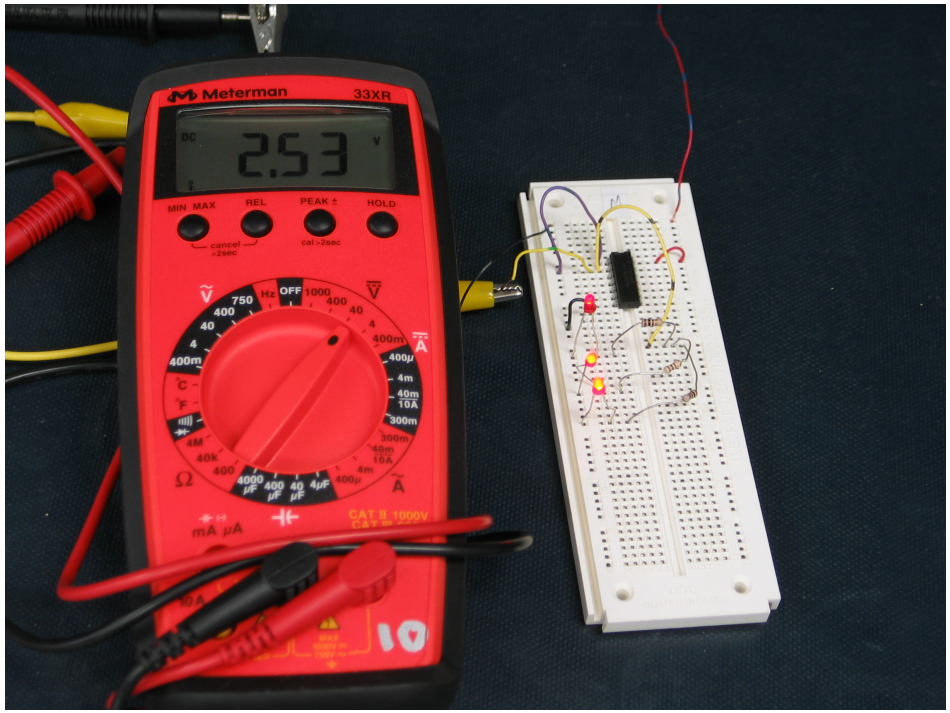
With an LED with a $1k\Omega$ resistor, the output voltage has dropped further.



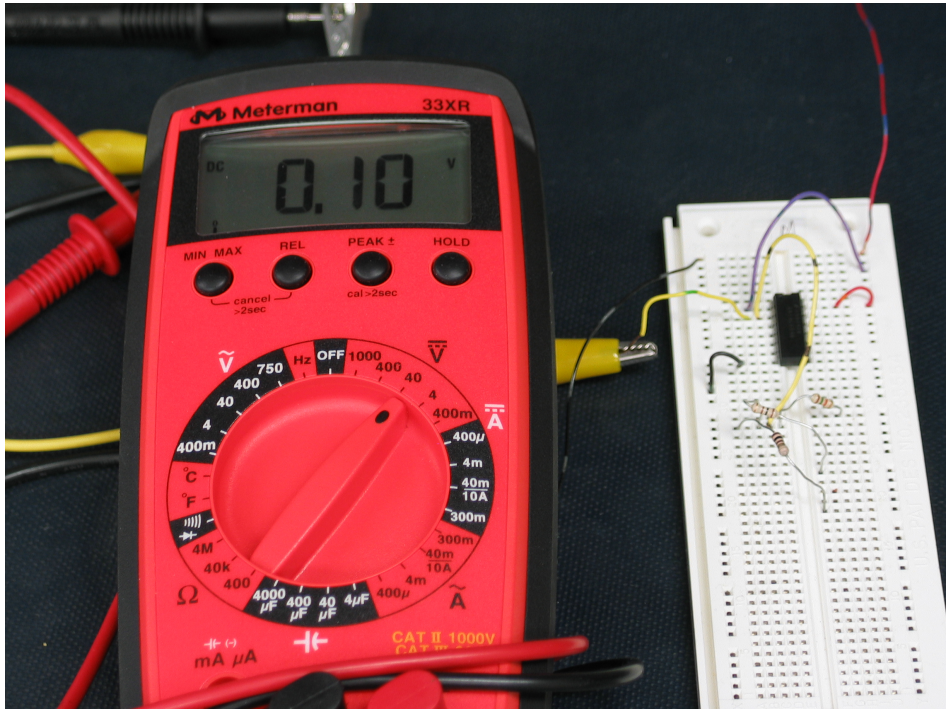
With an LED with a 100Ω resistor, the output voltage has dropped further.



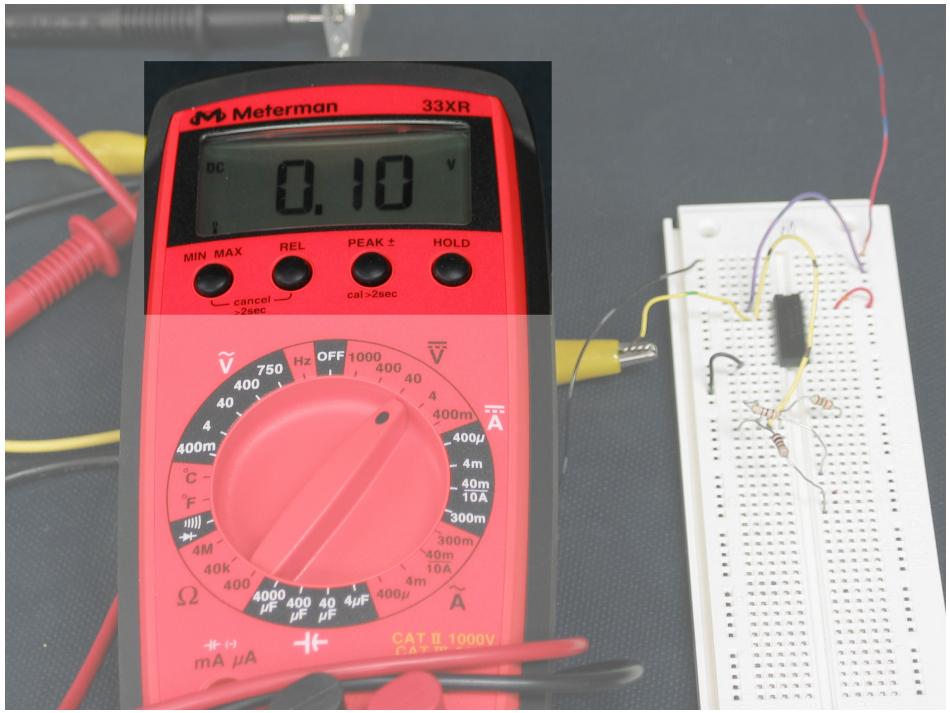
With two LEDs with 100Ω resistors, the output voltage has dropped further.



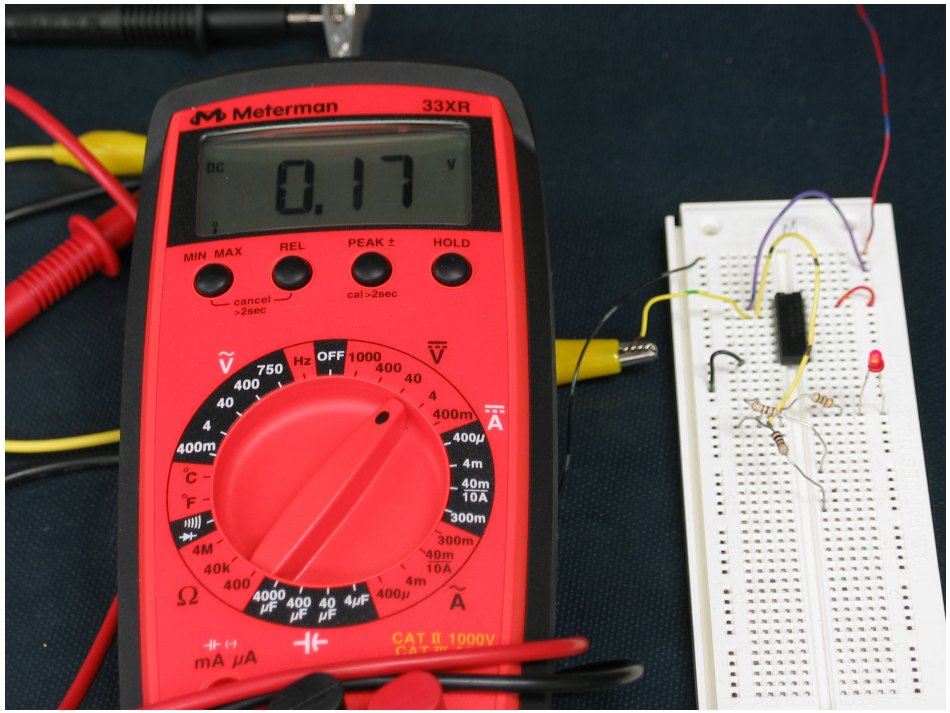
With three LEDs with 100Ω resistors, the output voltage has dropped further.



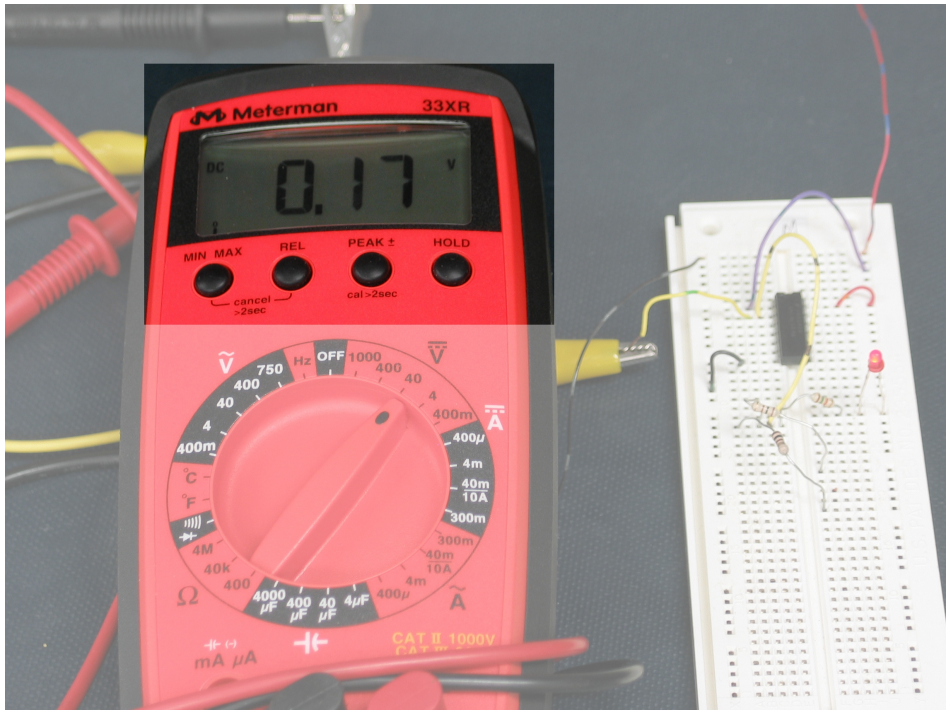
Here's the same TTL gate (LS04) producing a LOW output with no load.



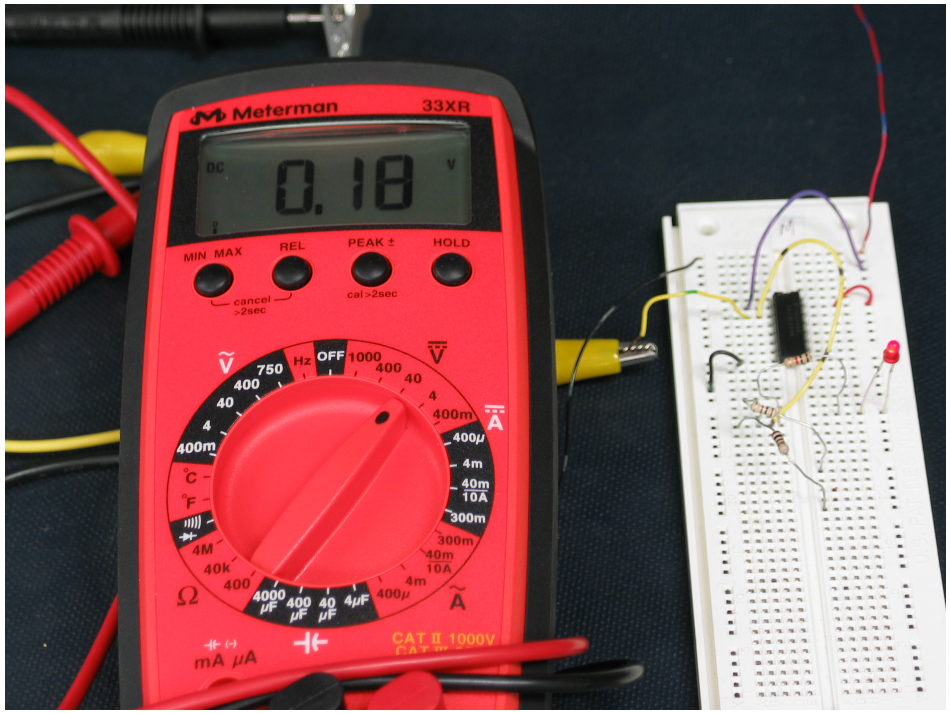
The output voltage with no load is 0.10 Volts.



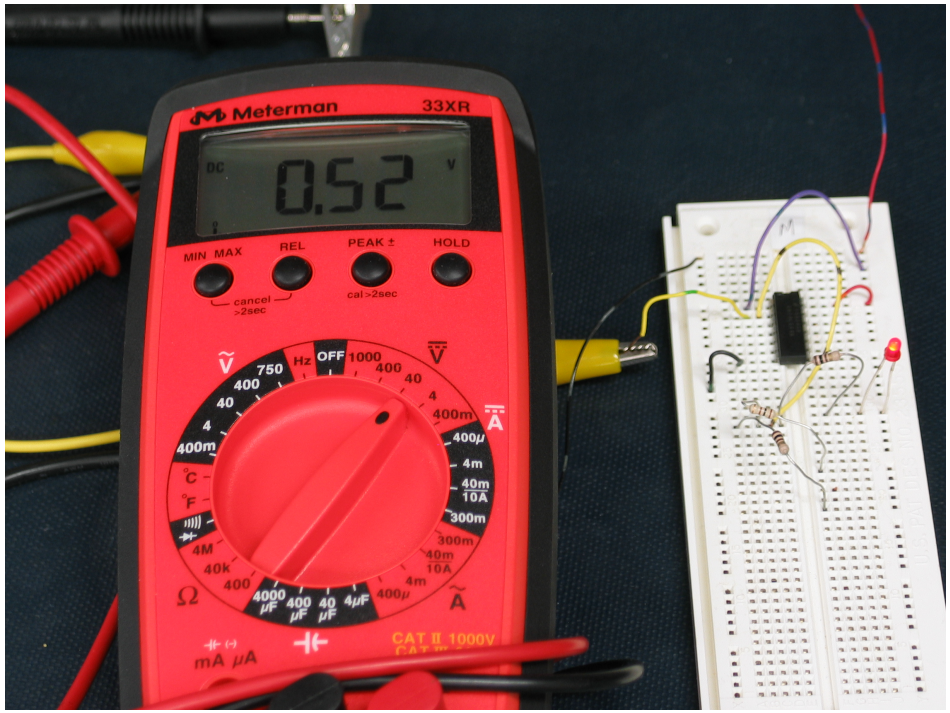
With an LED with a $5.1k\Omega$ *pull-up* resistor, the output voltage has risen.



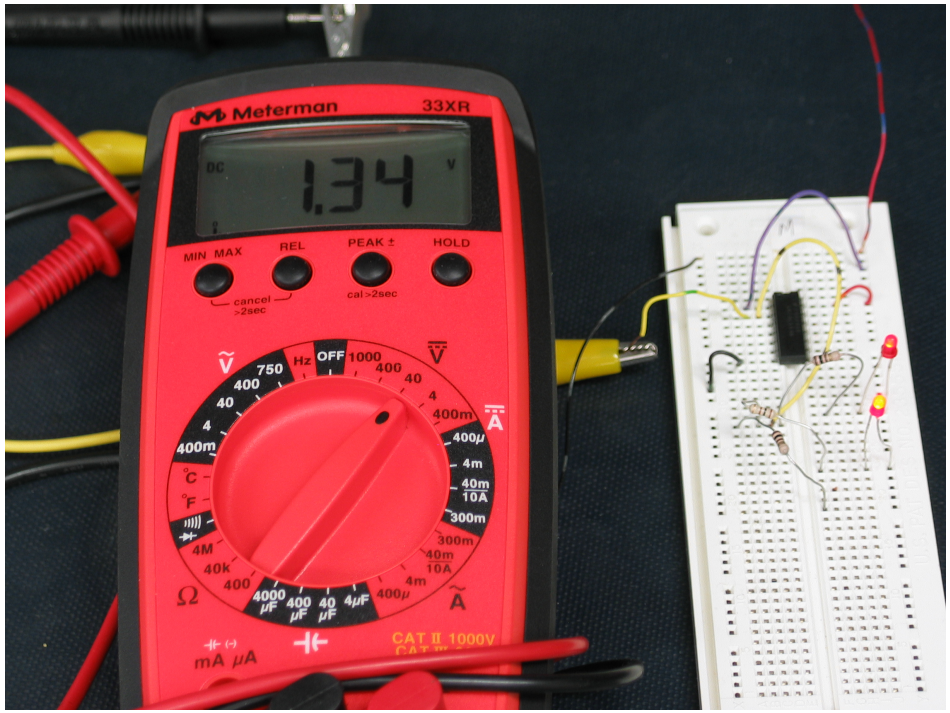
The output voltage with less than 1mA load is 0.17 Volts.



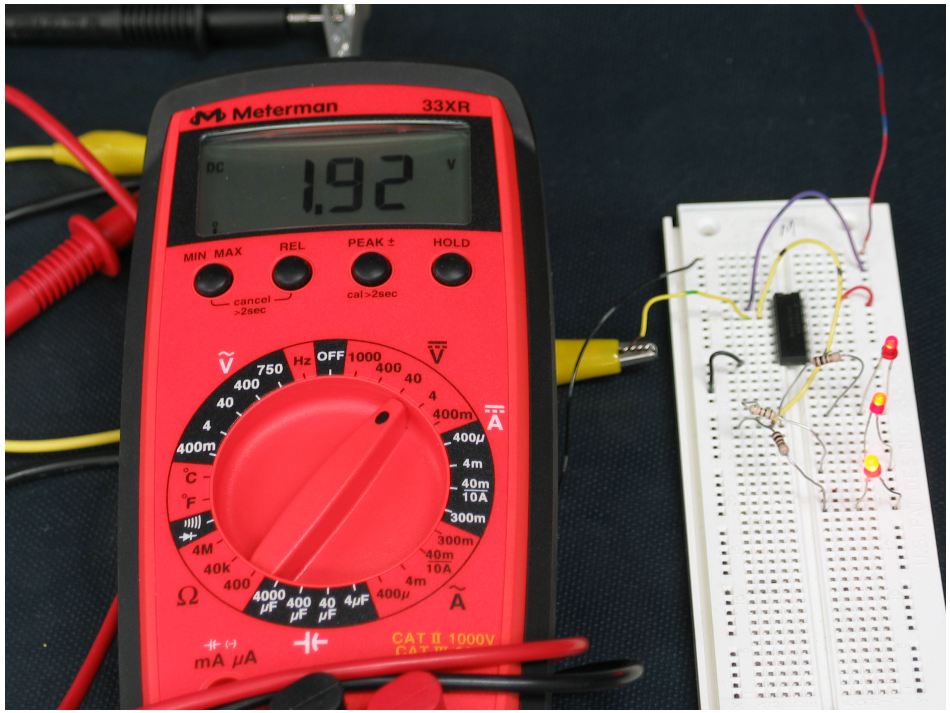
With an LED with a $1k\Omega$ resistor, the output voltage has risen further.



With an LED with a 100Ω resistor, the output voltage has risen further.



With two LEDs with 100Ω resistors, the output voltage has risen further.



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Input current requirements

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When the inputs of a gate are unconnected, they are neither HIGH nor LOW.

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They are said to be **floating**.

Input current limits; example

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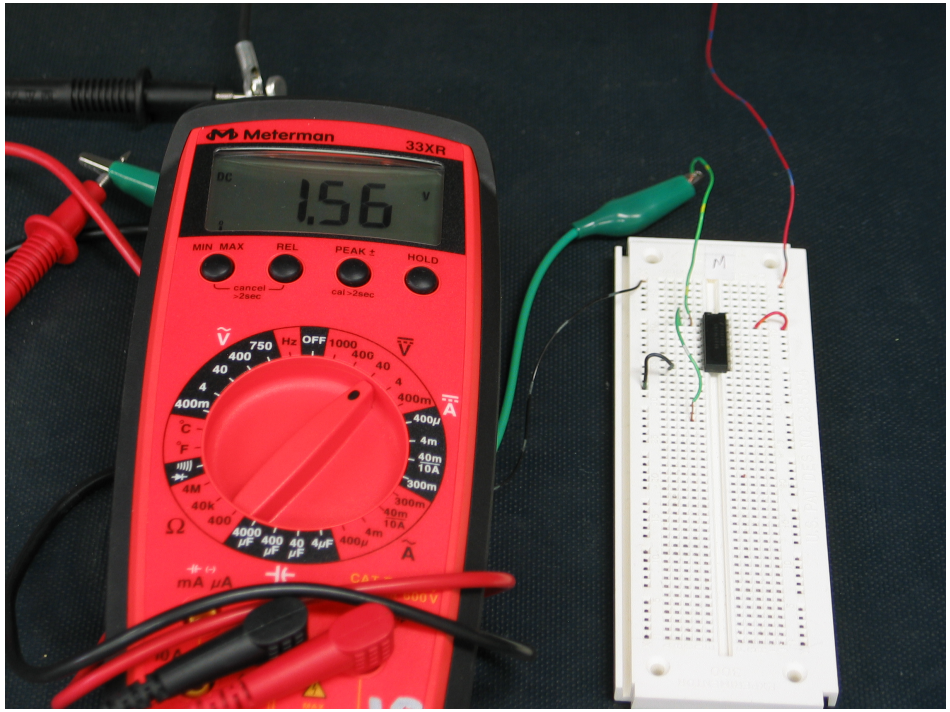

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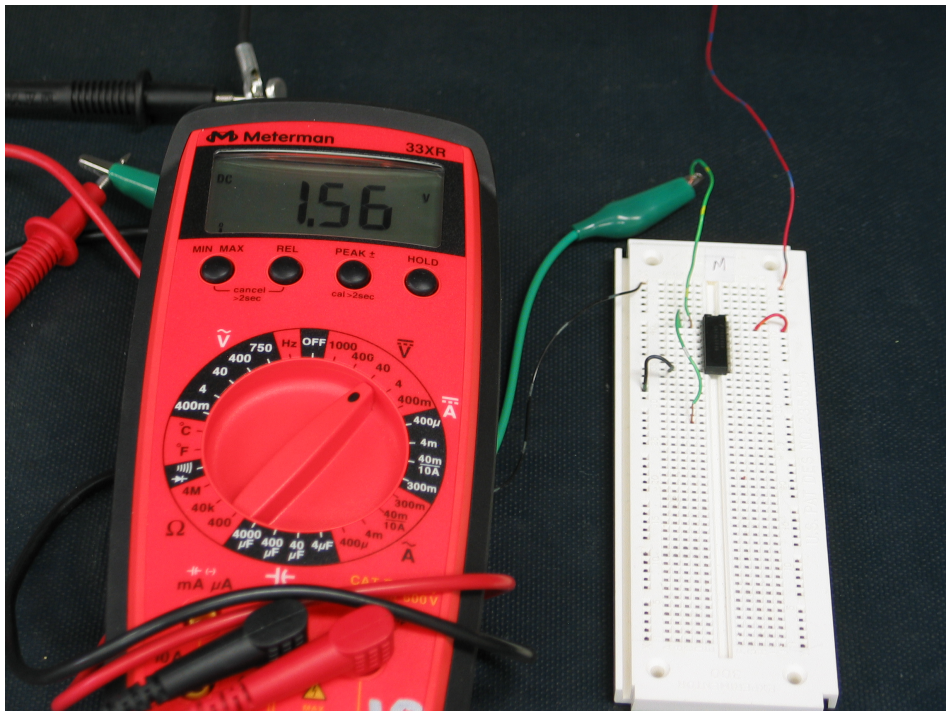
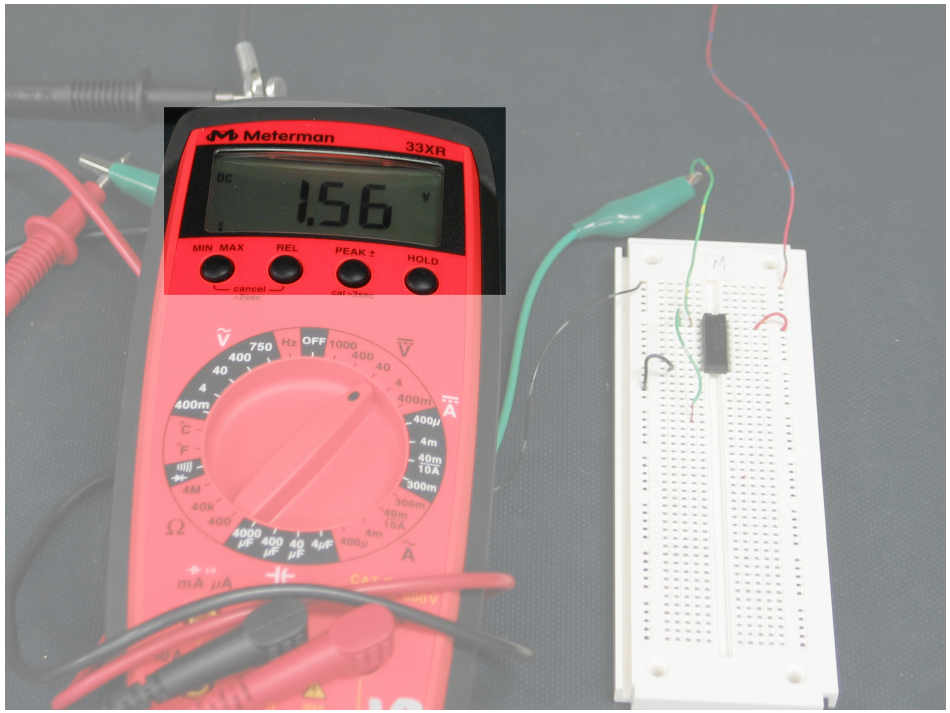
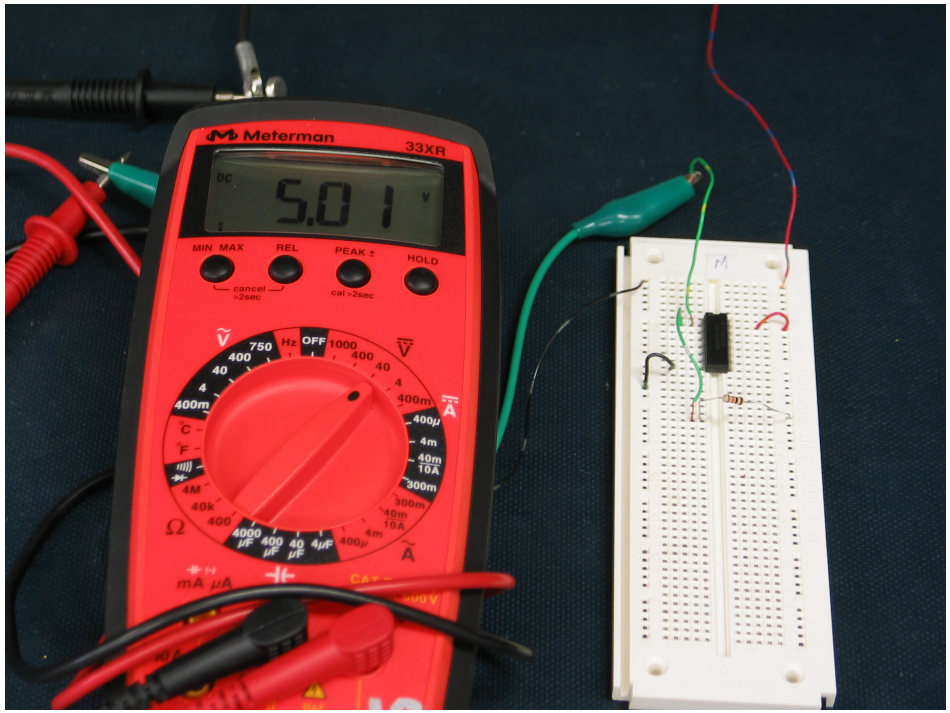


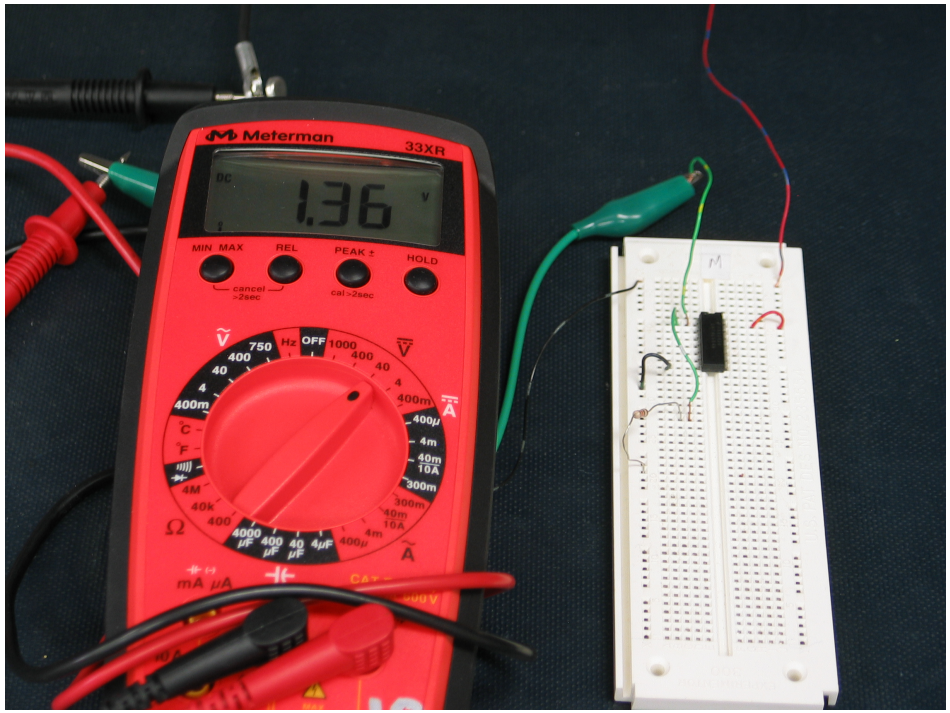
Here's the voltage on the input of a TTL gate (LS04) when left floating.



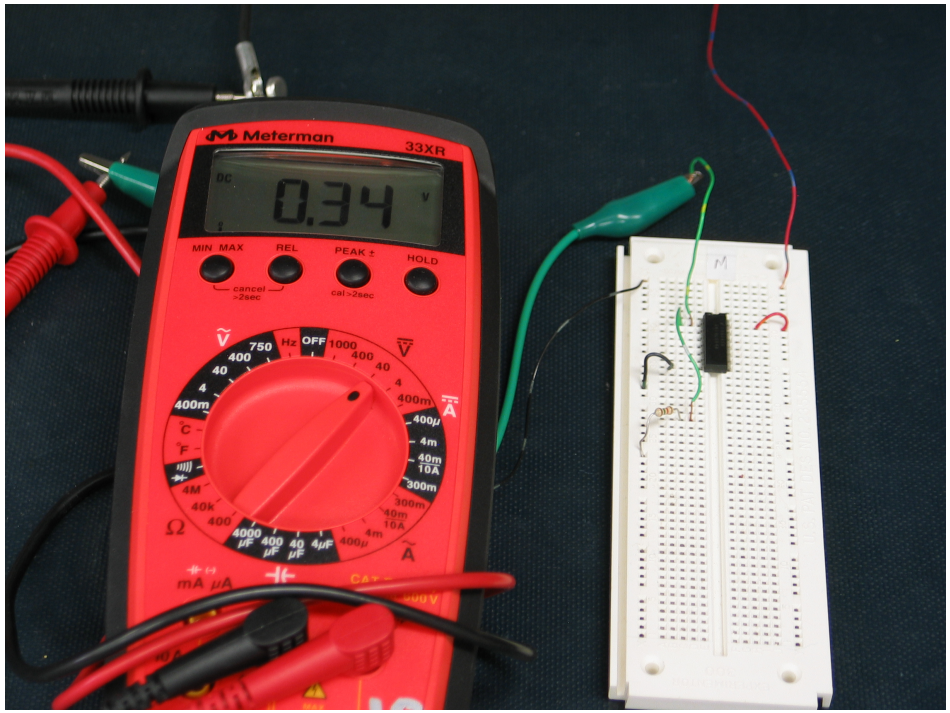
Notice that the input voltage is not valid for either HIGH **or** LOW.



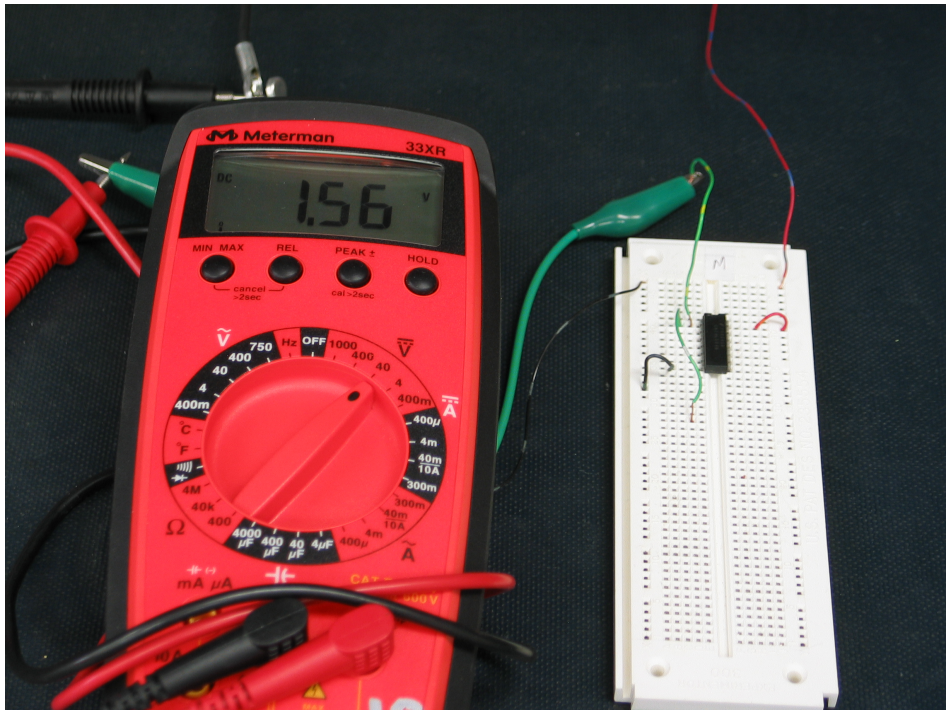
With a $10k\Omega$ resistor to V_{cc}, the input is now a valid HIGH.



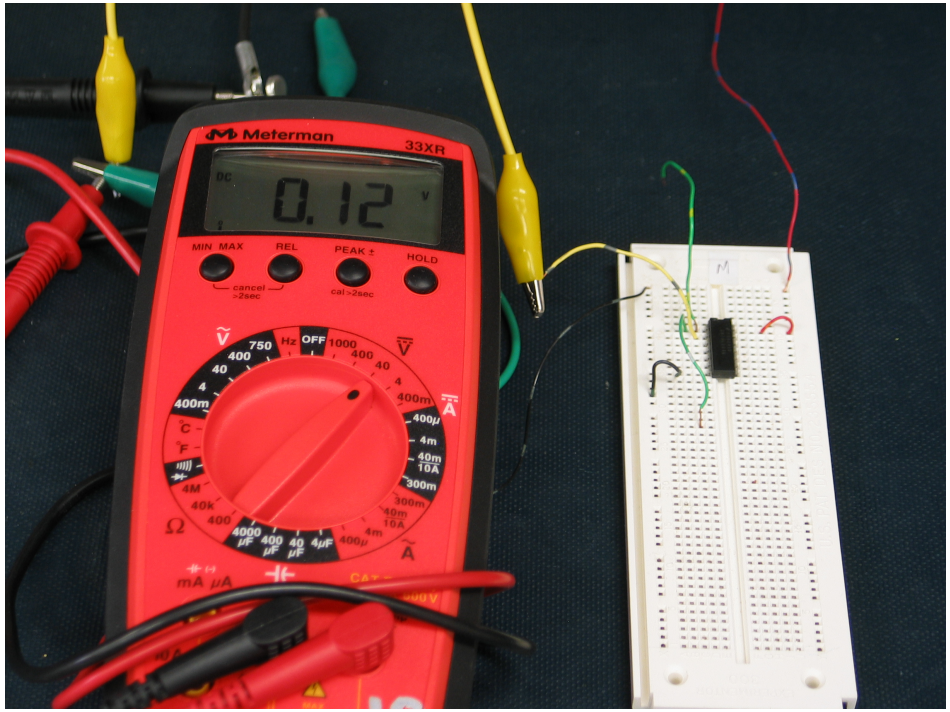
With a $10k\Omega$ resistor to GROUND, though, the input is **not** a valid LOW.



With a $5.1k\Omega$ resistor to GROUND the input **is** a valid LOW.



What's the output when the inputs are floating?



The output (in this case) is a valid LOW, *as though* the input were a valid HIGH.

Output current limits; Connecting gates

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When the output of one gate is used as the input of another gate, the *output* section of the first gate must source (or sink) enough current so that the *input* voltage of the second gate is within the proper range.

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The output of different types of gates is more similar than the inputs functionally, and an equivalent circuit is given in the following figure.

TTL input current limits

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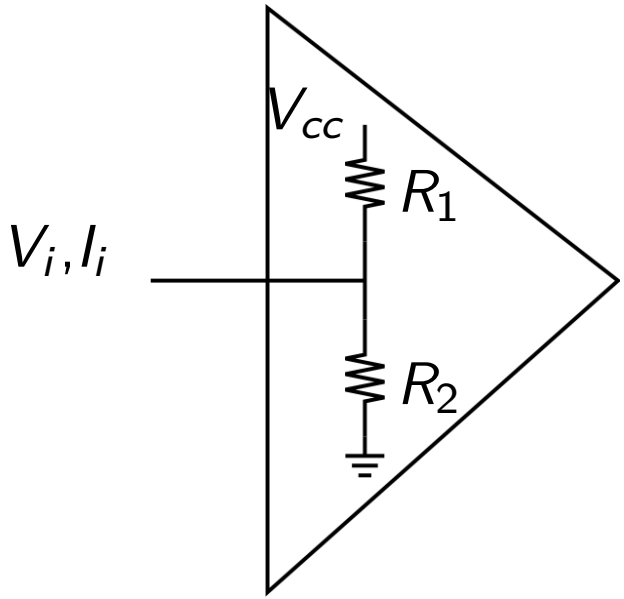

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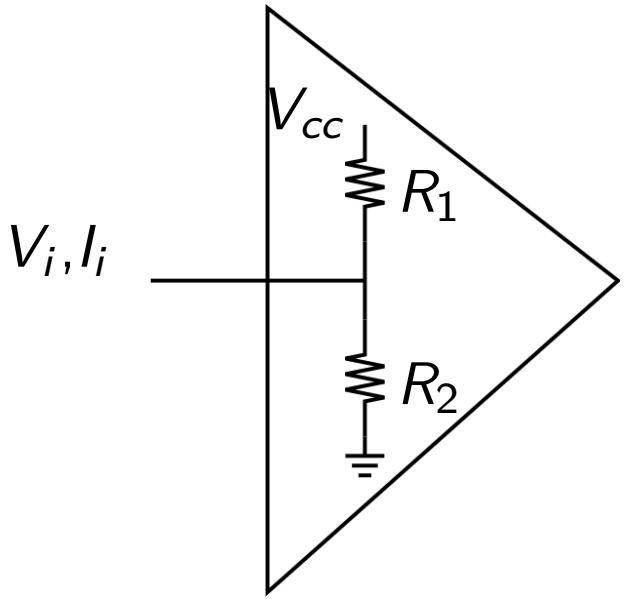

This is an equivalent circuit for a TTL gate *input*.

TTL connections

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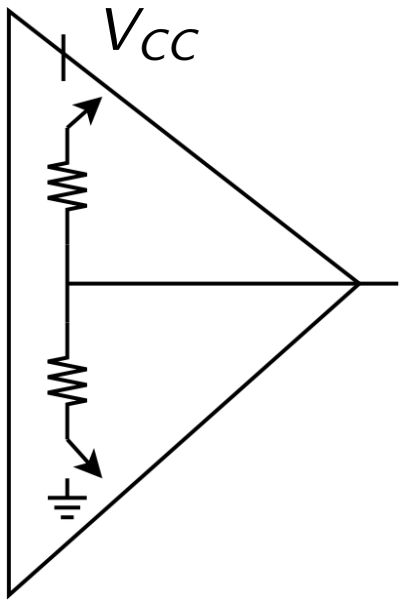

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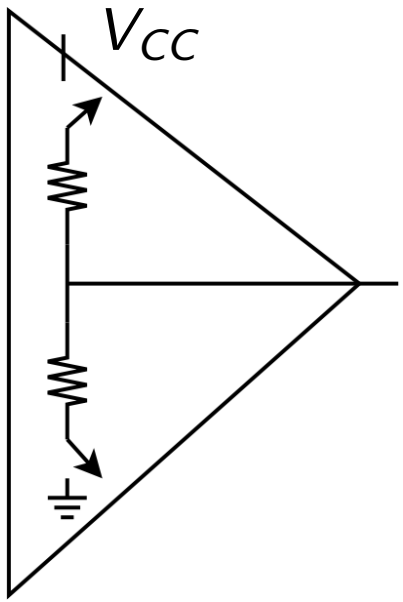

This is an equivalent circuit for a gate *output*.

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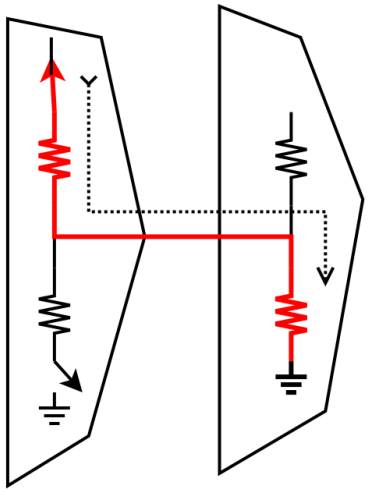

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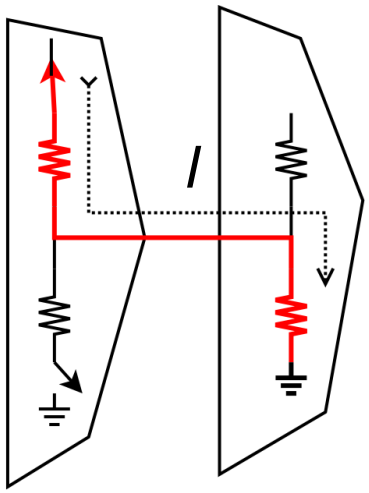

Current flows *out of* gate

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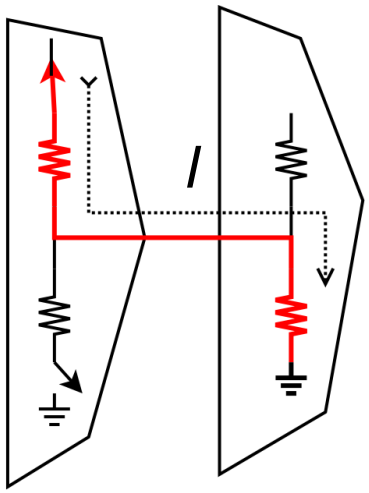

Current flows *out of* gate

Voltage must stay above $V_{IH_{min}}$

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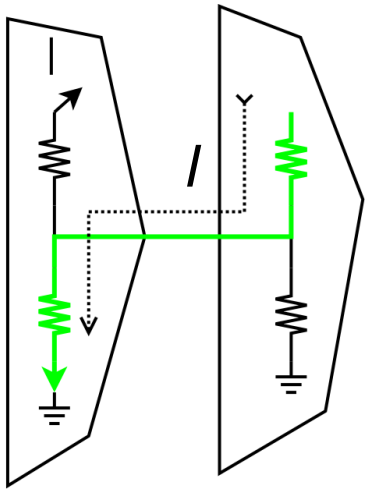
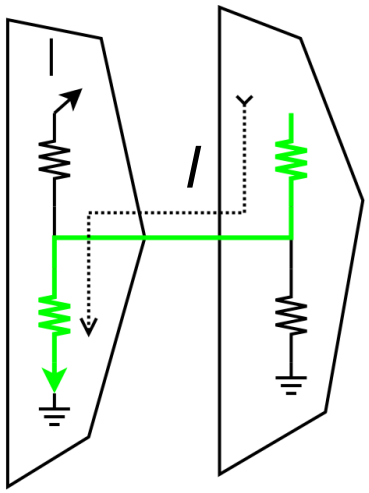


Here's what happens when a TTL LOW output feeds into another TTL input.



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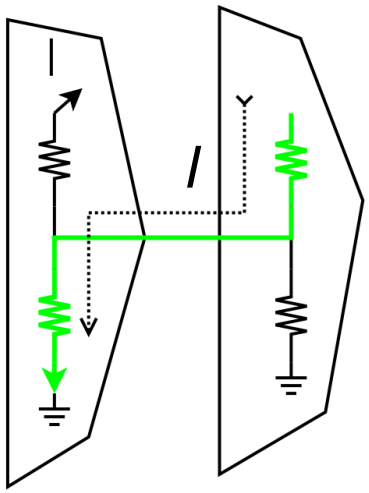

Current flows *into* gate

Voltage must stay below $V_{IL_{max}}$

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Consider the equivalent circuit shown in the following figure.

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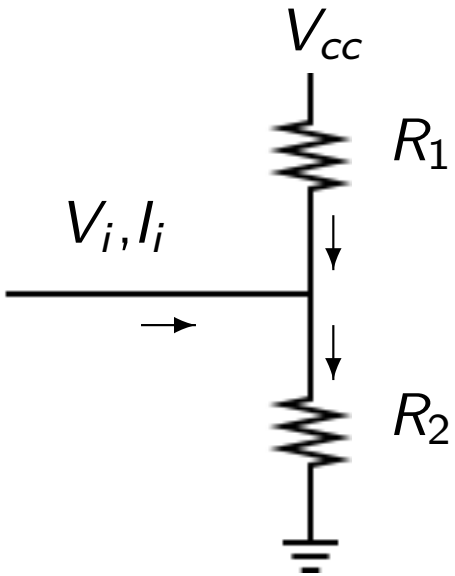

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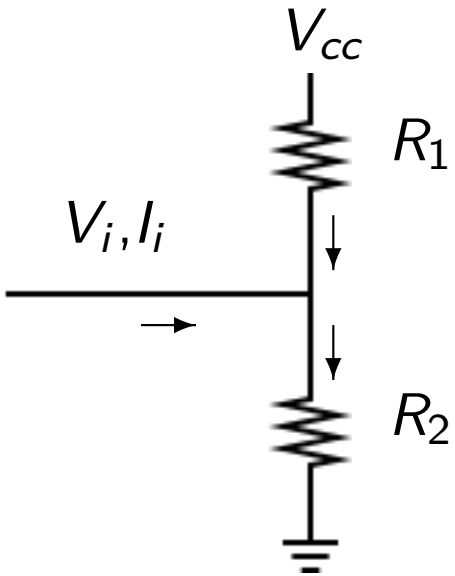

This is an equivalent circuit for a TTL gate *input*.

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$$V_i = \left(\frac{V_{cc} - V_i}{R_1} + I_i \right) R_2$$

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and thus

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(Note that in order to make V_i low, I_i will have to be negative.)

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Thus there are two quantities, I_{CCH} and I_{CCL}.

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The following figure shows the equivalent circuit for a CMOS input.

CMOS input current limits

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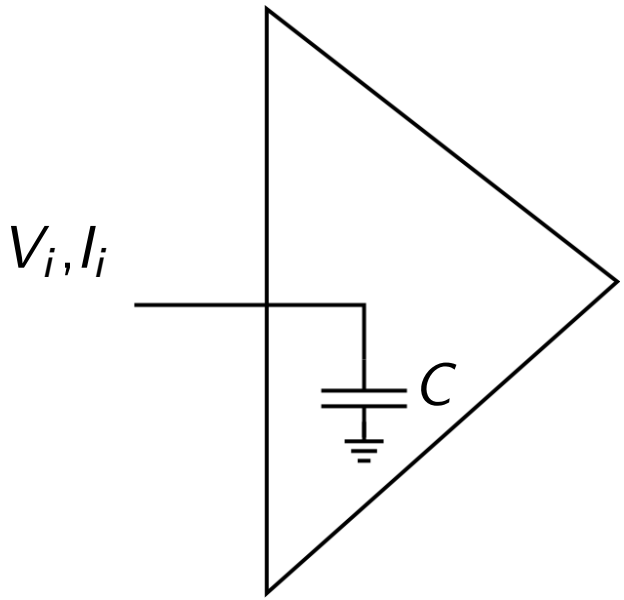

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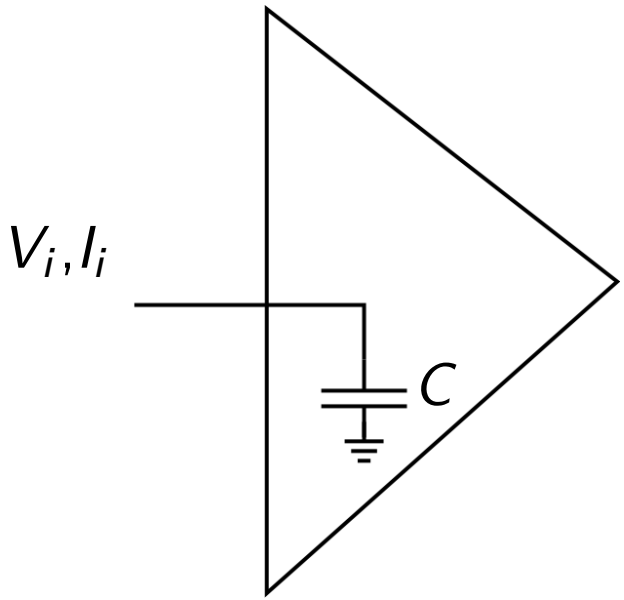

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CMOS connections

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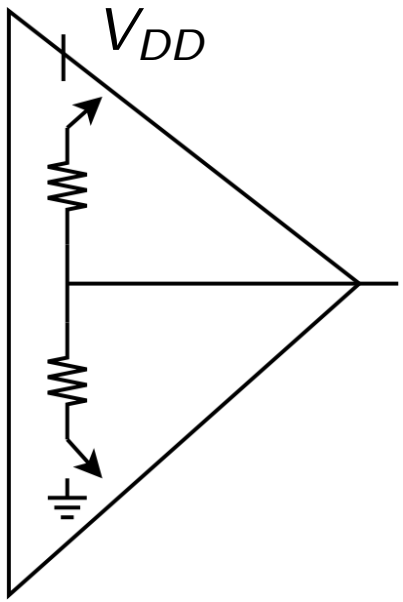

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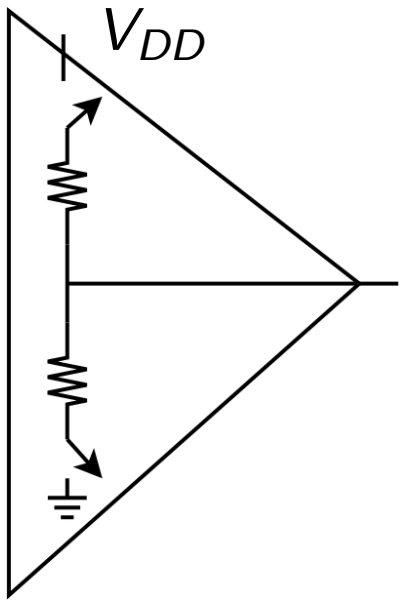

The equivalent circuit for a CMOS *output* is similar to TTL.

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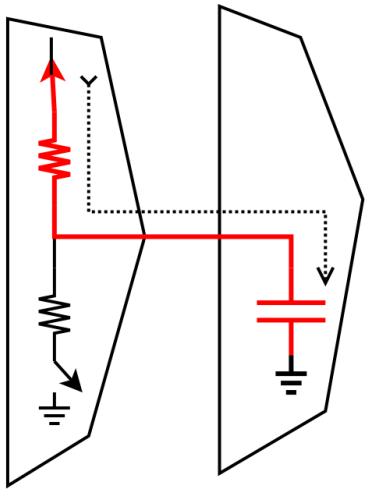

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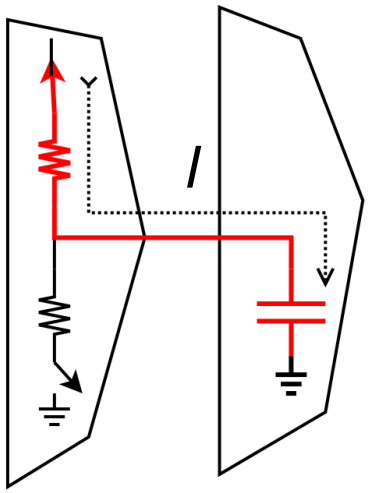
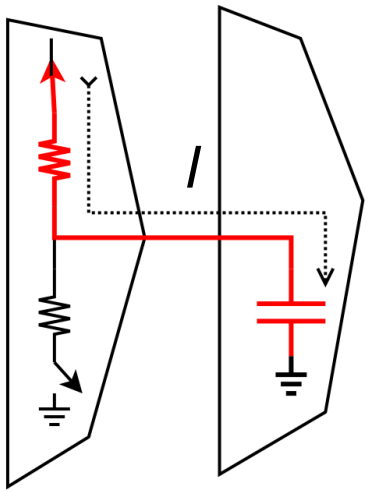


Current flows *out of* gate

Here's what happens when a CMOS HIGH output feeds into another CMOS input.



Current flows *out of* gate

Voltage must rise above $V_{IH_{min}}$

Here's what happens when a CMOS LOW output feeds into another CMOS input.

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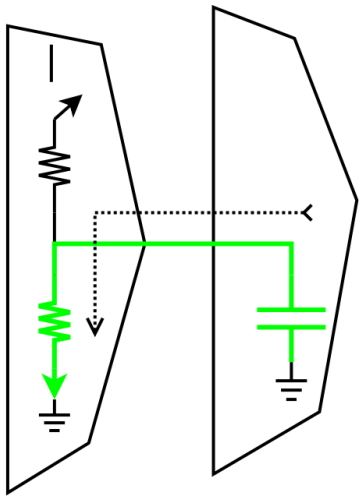
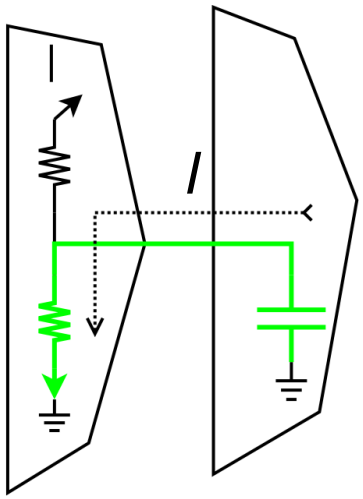
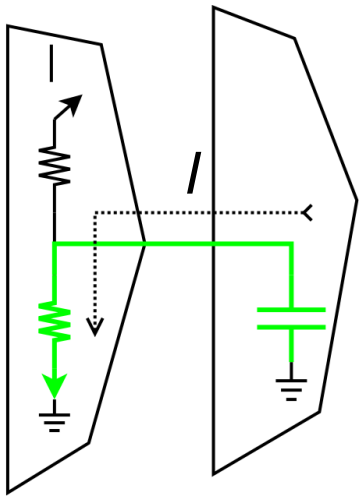


Here's what happens when a CMOS LOW output feeds into another CMOS input.



Current flows *into* gate

Here's what happens when a CMOS LOW output feeds into another CMOS input.



Current flows *into* gate

Voltage must fall below $V_{IL_{max}}$

For CMOS, even though the output equivalent circuit is similar to that of a TTL gate, when one gate is connected to another there is a limit to the *speed* at which the second gate will change due to the time it takes for the input capacitor to charge or discharge.

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Since the gate input is capacitive, then the current drawn from the previous gate will start big and get smaller as the capacitor reaches its intended voltage.

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Thus there is only one quantity, $I_{DD_{max}}$

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where I_{total} is the sum of the currents drawn by each of the gates on the device.

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The supply must be able to provide as much as needed by the whole circuit.

Quiescent current

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As long as power is applied to a chip, it will be drawing a small amount of current.

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While they are functionally equivalent, the first view will give a *minimum* for a quantity while the second will give a *maximum*.

Different manufacturers may take either view, and so it is important to understand this so that you can make sense of whichever you are given.

Four particular quantities are of interest in specifying the tolerance:

1. $I_{IL_{max}}$

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   the *maximum* input current which must be drawn from a gate's input to ground to guarantee the input will be low.

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   the *maximum* current which the gate can source through its output and still keep the output high.

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4. $I_{OL_{max}}$

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   the *maximum* input current which must be supplied to a gate's input to guarantee the input will be high.

3. $I_{OH_{max}}$

   the *maximum* current which the gate can source through its output and still keep the output high.

4. $I_{OL_{max}}$

   the *maximum* current which the gate can sink through its output and still keep the output low.

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If you want them to be in a particular state, tie them that way.

These current limits are referred to as the *fan–in* and *fan–out* characteristics of digital circuits.

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Note that a given gate will occasionally have zero for either $\mathrm{I_{IL_{max}}}$ *or* $\mathrm{I_{IH_{max}}}$.

Interfacing families; CMOS to TTL and TTL to CMOS

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Each gate must stay within its required operating parameters.