CP316 Introduction

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Introduction to the PIC Microcontroller

Introduction to the PIC Microcontroller

μPU vs. μCU vs. DSP

Introduction to the PIC Microcontroller

μPU vs. μCU vs. DSP

$\rightarrow$ Section 1.2.2

Introduction to the PIC Microcontroller

μPU vs. μCU vs. DSP

$\rightarrow$ Section 1.2.2

$\rightarrow$ Section 1.4

Introduction to the PIC Microcontroller

μPU vs. μCU vs. DSP

$\rightarrow$ Section 1.2.2

$\rightarrow$ Section 1.4

QwikFlash Board

Introduction to the PIC Microcontroller

μPU vs. μCU vs. DSP

$\rightarrow$ Section 1.2.2

$\rightarrow$ Section 1.4

QwikFlash Board

MPLABX IDE

Oscillator configurations

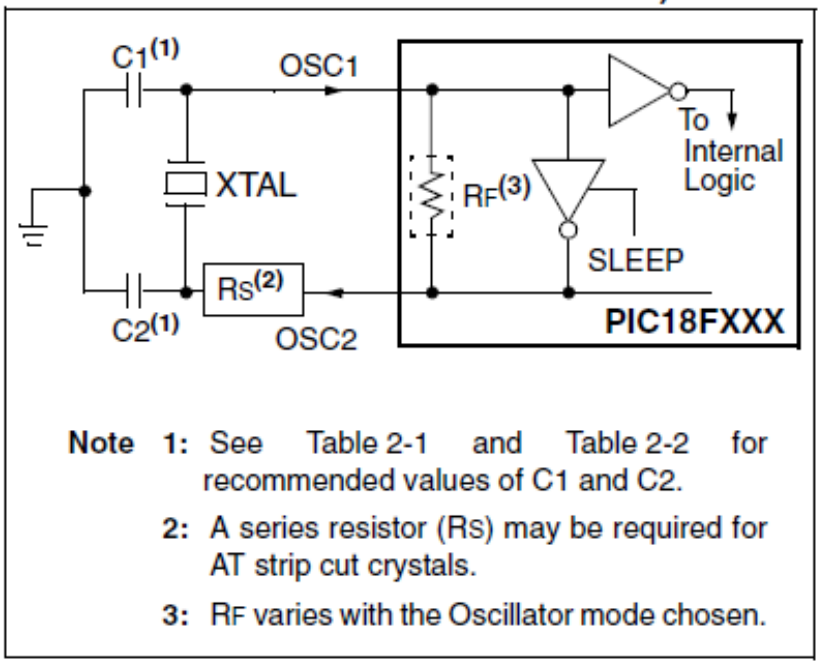
Oscillator configurations

→ Section 2.0

Figure 2-1

Figure 2-1

FIGURE 2-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP CONFIGURATION)



Note 1: See Table 2-1 and Table 2-2 for recommended values of C1 and C2.

2: A series resistor (RS) may be required for AT strip cut crystals.

3: RF varies with the Oscillator mode chosen.

Figure 2-2

Figure 2-2

FIGURE 2-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

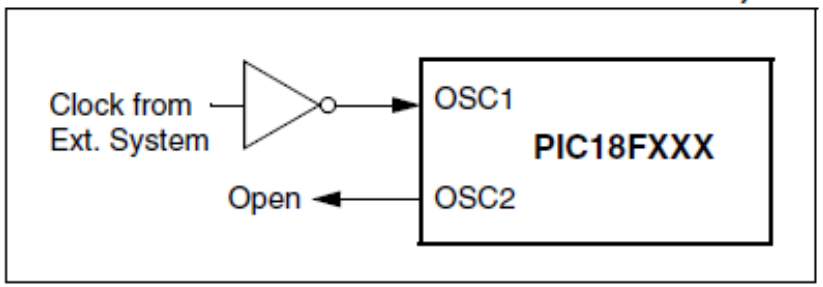
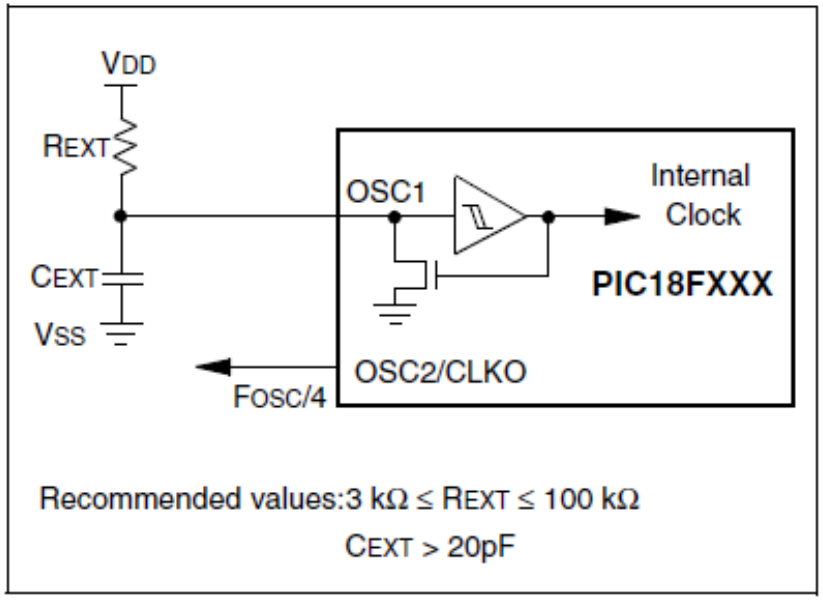


Figure 2-3

Figure 2-3

FIGURE 2-3: RC OSCILLATOR MODE



The RCIO Oscillator mode functions like the RC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6).

Figure 2-4

Figure 2-4

FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION (EC CONFIGURATION)

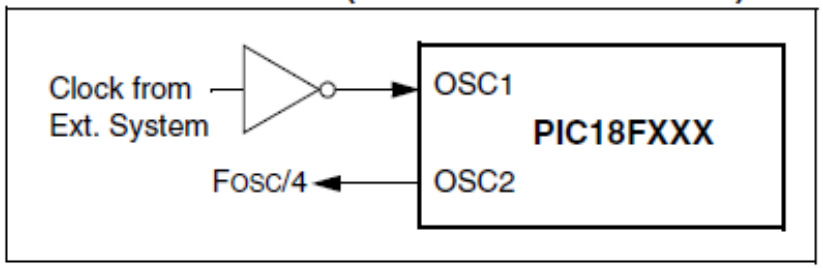


Figure 2-5

Figure 2-5

FIGURE 2-5: EXTERNAL CLOCK INPUT OPERATION (ECIO CONFIGURATION)

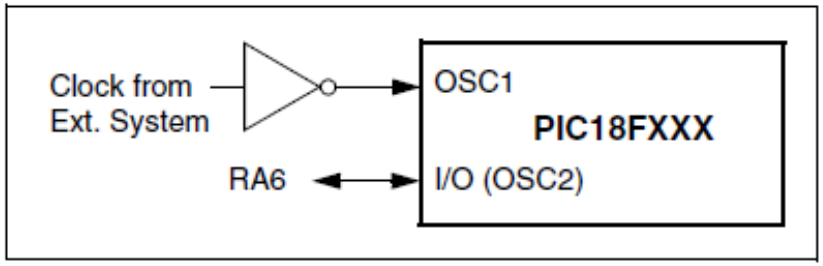


Figure 2-6

Figure 2-6

FIGURE 2-6: PLL BLOCK DIAGRAM

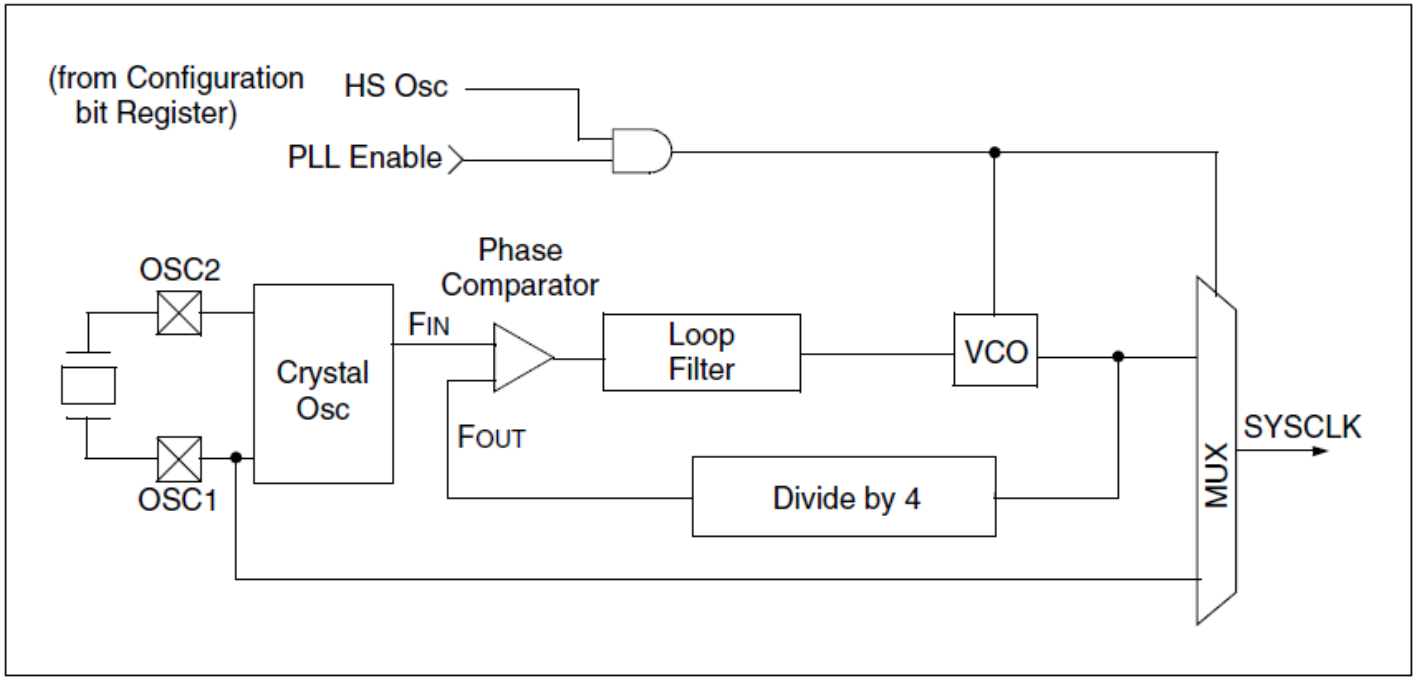


Figure 2-7

Figure 2-7

FIGURE 2-7: DEVICE CLOCK SOURCES

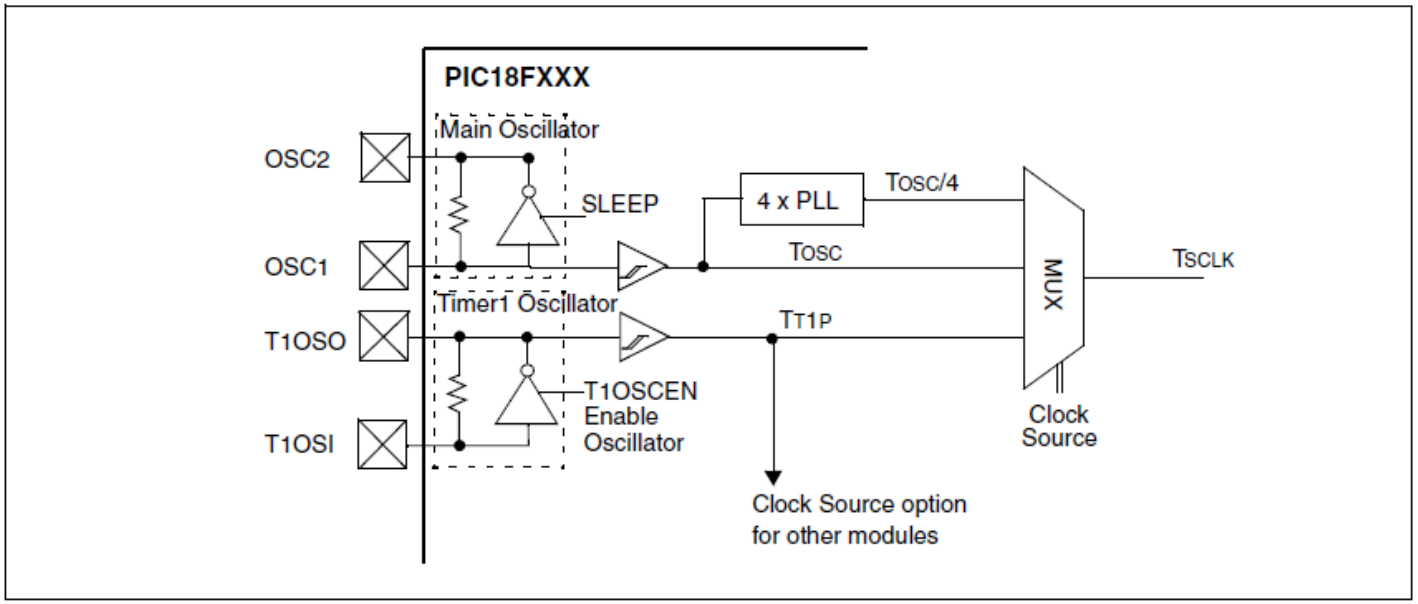
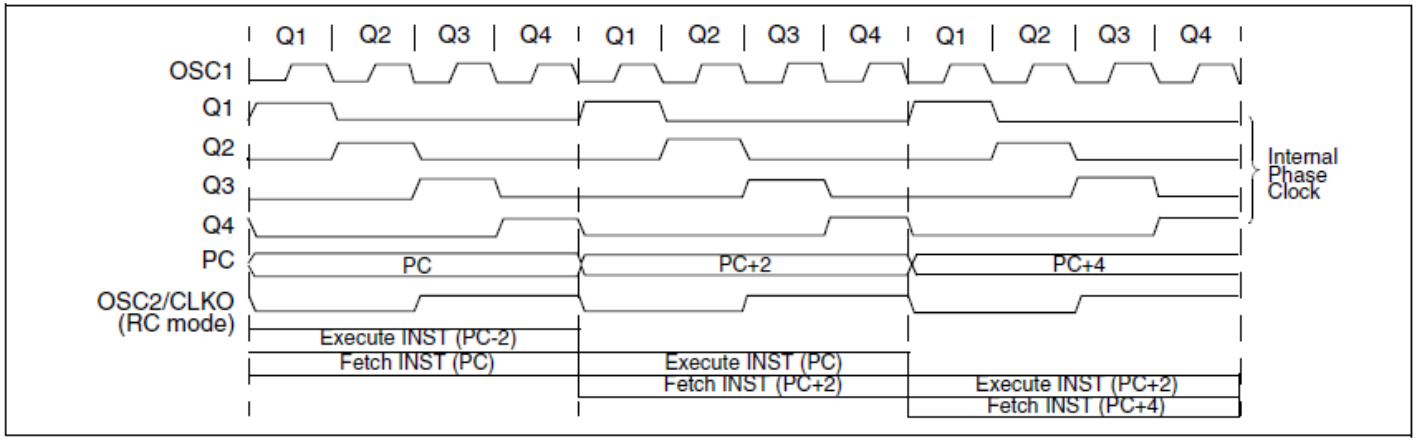


Figure 4-4

Figure 4-4

FIGURE 4-4: CLOCK/INSTRUCTION CYCLE



OSCCON register

OSCCON register

Oscillator configuration register

OSCCON register

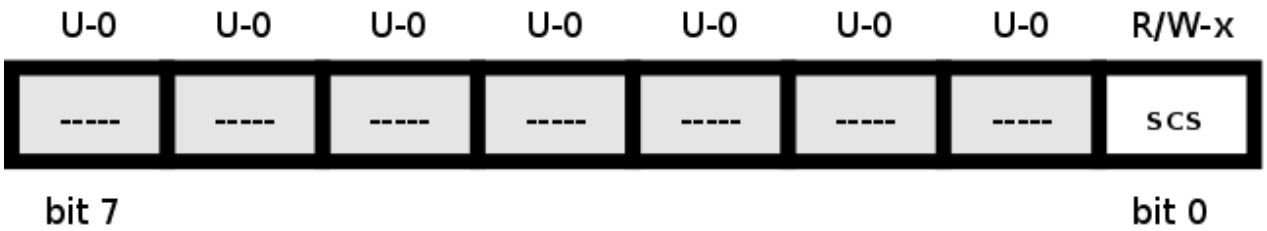
Oscillator configuration register

→ Section 2.6.1

OSCCON register

Oscillator configuration register

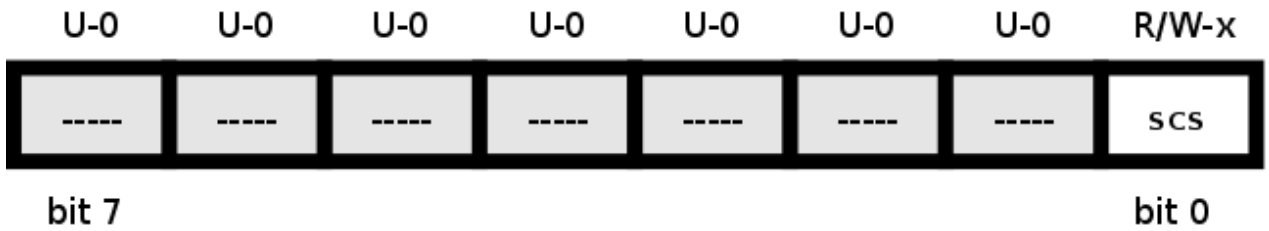
→ Section 2.6.1



OSCCON register

Oscillator configuration register

→ Section 2.6.1



Bits in OSCCON register

Memory organization

Memory organization

Modified Harvard Architechture

Memory organization

Modified Harvard Architechture

→ Section 1.5.1

Memory organization

Modified Harvard Architechture

→ Section 1.5.1

→ Section 14.3

Memory organization

Modified Harvard Architechture

→ Section 1.5.1

→ Section 14.3

→ Section 1.11.1

Memory organization

Modified Harvard Architechture

→ Section 1.5.1

→ Section 14.3

→ Section 1.11.1

→ Section 4.0

Data memory

Data memory

Data memory location $\rightarrow$ File Register

Data memory

Data memory location $\rightarrow$ File Register

GPRs

Data memory

Data memory location $\rightarrow$ File Register

GPRs

SFRs

Data memory

Data memory location → File Register

GPRs

SFRs

→ Section 4.9

Data memory

Data memory location → File Register

GPRs

SFRs

→ Section 4.9

Access bank

Data memory

Data memory location → File Register

GPRs

SFRs

→ Section 4.9

Access bank

→ Section 4.10

Data memory

Data memory location → File Register

GPRs

SFRs

→ Section 4.9

Access bank

→ Section 4.10

BSR

Data memory

Data memory location → File Register

GPRs

SFRs

→ Section 4.9

Access bank

→ Section 4.10

BSR

→ Section 4.11

Data memory

Data memory location → File Register

GPRs

SFRs

→ Section 4.9

Access bank

→ Section 4.10

BSR

→ Section 4.11

No software stack!

Data memory

Data memory location → File Register

GPRs

SFRs

→ Section 4.9

Access bank

→ Section 4.10

BSR

→ Section 4.11

No software stack!

→ Section 1.5.4

Data memory

Data memory location → File Register

GPRs

SFRs

→ Section 4.9

Access bank

→ Section 4.10

BSR

→ Section 4.11

No software stack!

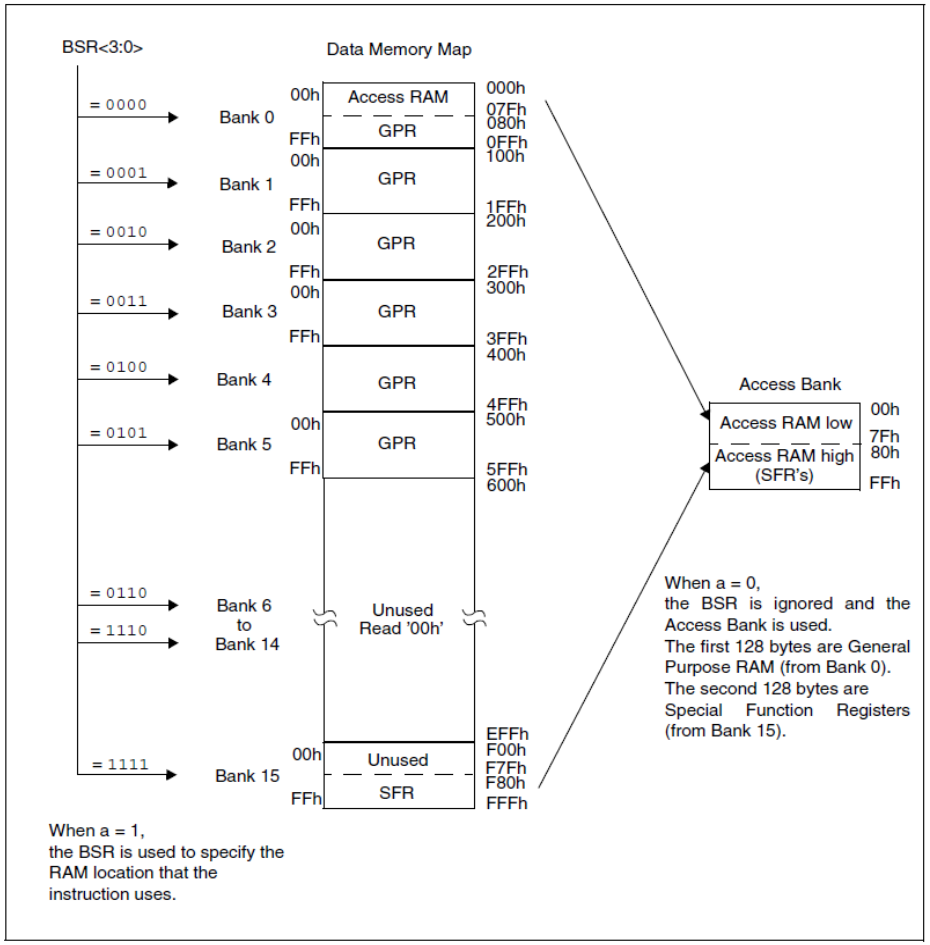
→ Section 1.5.4

→ Section 4.2

File Registers and Access Bank

File Registers and Access Bank

FIGURE 4-7: DATA MEMORY MAP FOR PIC18F252/452



Features

Features

RISC architecture

Features

RISC architecture

→ Section 1.11.1

Features

RISC architecture

→ Section 1.11.1

→ Section 1.4

Features

RISC architecture

→ Section 1.11.1

→ Section 1.4

→ Section 20.0

Features

RISC architecture

→ Section 1.11.1

→ Section 1.4

→ Section 20.0

Simple assembler

Features

RISC architecture

→ Section 1.11.1

→ Section 1.4

→ Section 20.0

Simple assembler

→ Section 1.9

Features

RISC architecture

→ Section 1.11.1

→ Section 1.4

→ Section 20.0

Simple assembler

→ Section 1.9

→ Section 21.2

W Register

W Register

Working register

W Register

Working register

→ Section 1.6

W Register

Working register

→ Section 1.6

also SFR 0xFE8

W Register

Working register

→ Section 1.6

also SFR 0xFE8

→ Section 1.0

STATUS register

STATUS register

Status register

STATUS register

Status register

→ Section 1.6

STATUS register

Status register

→ Section 1.6

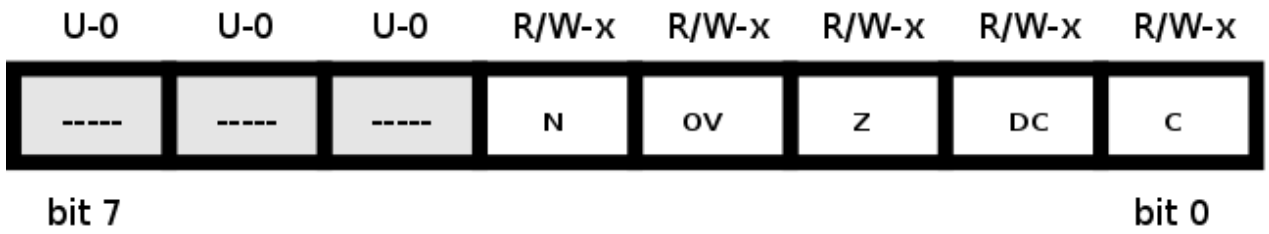
→ Section 4.13

STATUS register

Status register

→ Section 1.6

→ Section 4.13

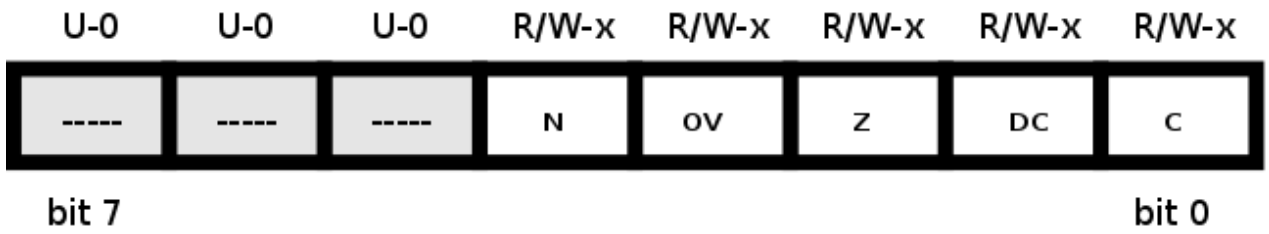


STATUS register

Status register

→ Section 1.6

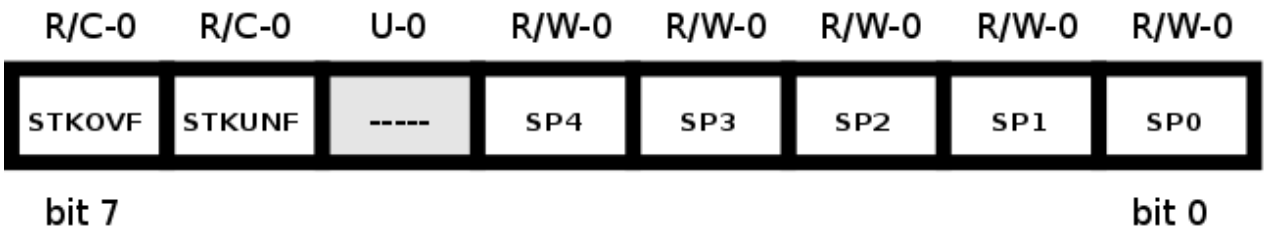
→ Section 4.13



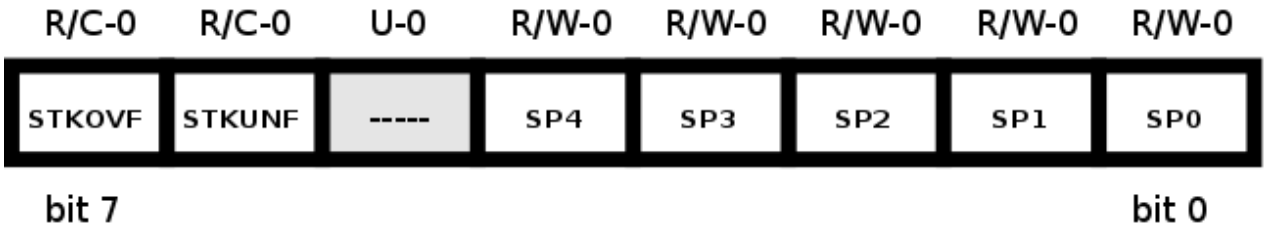
Bits in STATUS register

STKPTR register

STKPTR register



STKPTR register



Bits in STKPTR register