CP316
Interrupts

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Interrupts

Interrupts

overview

Interrupts

overview

→ Section 6.2.5

Interrupts

overview

→ Section 6.2.5

→ Section 8.0

Interrupts

overview

→ Section 6.2.5

→ Section 8.0

vectors

Interrupts

overview

→ Section 6.2.5

→ Section 8.0

vectors

→ Section 6.2.6

Interrupts

overview

→ Section 6.2.5

→ Section 8.0

vectors

→ Section 6.2.6

priority

Interrupts

overview

→ Section 6.2.5

→ Section 8.0

vectors

→ Section 6.2.6

priority

→ Section 6.2.4

Interrupts

overview

→ Section 6.2.5

→ Section 8.0

vectors

→ Section 6.2.6

priority

→ Section 6.2.4

status; clear, pending

Interrupts

overview

→ Section 6.2.5

→ Section 8.0

vectors

→ Section 6.2.6

priority

→ Section 6.2.4

status; clear, pending

→ Sections 6.2.3

Interrupts

overview

→ Section 6.2.5

→ Section 8.0

vectors

→ Section 6.2.6

priority

→ Section 6.2.4

status; clear, pending

→ Sections 6.2.3

bits; enable, priority, flag

Interrupts

overview

→ Section 6.2.5

→ Section 8.0

vectors

→ Section 6.2.6

priority

→ Section 6.2.4

status; clear, pending

→ Sections 6.2.3

bits; enable, priority, flag

→ Sections 6.4.2

Interrupt Inititallization

Interrupt Inititallization

1. setup

Interrupt Inititallization

1. setup
2. clear flags

Interrupt Inititallization

1. setup
2. clear flags
3. enable

Interrupt Service Routines

Interrupt Service Routines

1. confirm source

Interrupt Service Routines

1. confirm source
2. process

Interrupt Service Routines

1. confirm source
2. process
3. clear flags (if required)

Interrupt Service Routines

1. confirm source
2. process
3. clear flags (if required)
4. **retfie**

Interrupt Resources

Interrupt Resources

shadow registers

Interrupt Resources

shadow registers

→ Section 4.7.1

Interrupt Resources

shadow registers

→ Section 4.7.1

fast register stack

Interrupt Resources

shadow registers

→ Section 4.7.1

fast register stack

→ Section 4.7.5

Interrupt Resources

shadow registers

→ Section 4.7.1

fast register stack

→ Section 4.7.5

retfie FAST

Interrupt Resources

shadow registers

→ Section 4.7.1

fast register stack

→ Section 4.7.5

retfie FAST

only use shadow registers for high priority interrupt!

Interrupt Sources

Interrupt Sources

internal, external

Interrupt Sources

internal, external

→ Chapter 8 (Figure 8-1)

Interrupt Sources

internal, external

→ Chapter 8 (Figure 8-1)

portB, timers, serial, ADC, etc.

Interrupt Sources

internal, external

→ Chapter 8 (Figure 8-1)

portB, timers, serial, ADC, etc.

→ Section 6.5.6

Interrupt Sources

internal, external

→ Chapter 8 (Figure 8-1)

portB, timers, serial, ADC, etc.

→ Section 6.5.6

special case: INT0

Interrupt Sources

internal, external

→ Chapter 8 (Figure 8-1)

portB, timers, serial, ADC, etc.

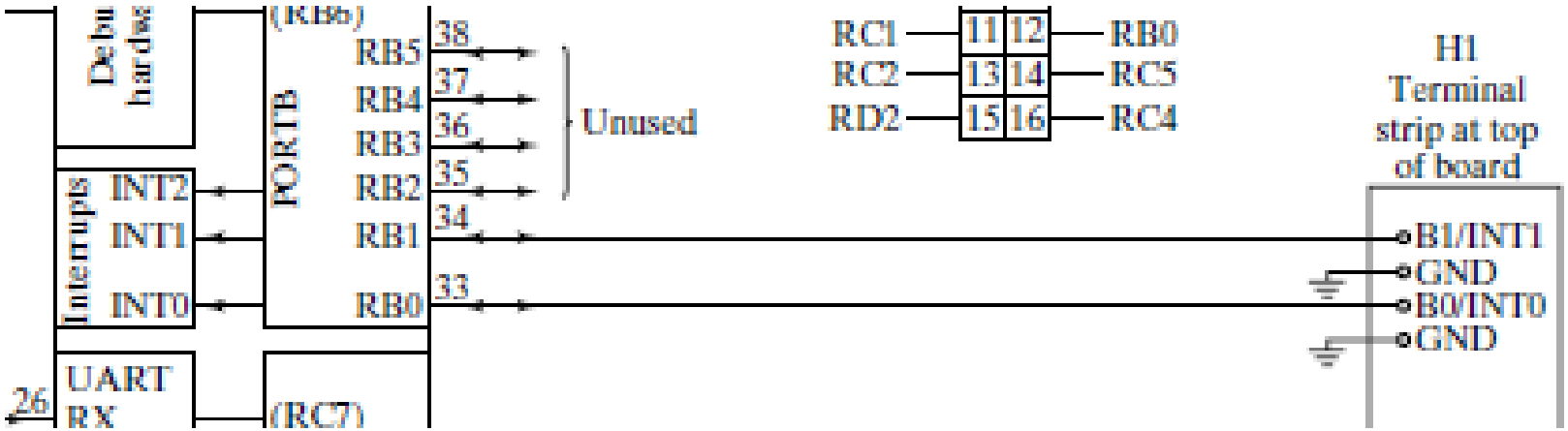
→ Section 6.5.6

special case: INT0

→ Section 8.6

Qwikflash interrupt connections

Qwikflash interrupt connections



Interrupt Registers

Interrupt Registers

RCON

Interrupt Registers

RCON

→ Section 6.4.3

Interrupt Registers

RCON

→ Section 6.4.3

INTCON, **INTCON2**, **INTCON3**

Interrupt Registers

RCON

→ Section 6.4.3

INTCON, **INTCON2**, **INTCON3**

→ Section 6.4.4

Interrupt Registers

RCON

→ Section 6.4.3

INTCON, **INTCON2**, **INTCON3**

→ Section 6.4.4

PIR1, **PIR2**

Interrupt Registers

RCON

→ Section 6.4.3

INTCON, **INTCON2**, **INTCON3**

→ Section 6.4.4

PIR1, **PIR2**

→ Section 6.4.5

Interrupt Registers

RCON

→ Section 6.4.3

INTCON, **INTCON2**, **INTCON3**

→ Section 6.4.4

PIR1, **PIR2**

→ Section 6.4.5

PIE1, **PIE2**

Interrupt Registers

RCON

→ Section 6.4.3

INTCON, **INTCON2**, **INTCON3**

→ Section 6.4.4

PIR1, **PIR2**

→ Section 6.4.5

PIE1, **PIE2**

→ Section 6.4.6

Interrupt Registers

RCON

→ Section 6.4.3

INTCON, **INTCON2**, **INTCON3**

→ Section 6.4.4

PIR1, **PIR2**

→ Section 6.4.5

PIE1, **PIE2**

→ Section 6.4.6

IPR1, **IPR2**

Interrupt Registers

RCON

→ Section 6.4.3

INTCON, **INTCON2**, **INTCON3**

→ Section 6.4.4

PIR1, **PIR2**

→ Section 6.4.5

PIE1, **PIE2**

→ Section 6.4.6

IPR1, **IPR2**

→ Section 6.4.7

Interrupt Registers

RCON

→ Section 6.4.3

INTCON, **INTCON2**, **INTCON3**

→ Section 6.4.4

PIR1, **PIR2**

→ Section 6.4.5

PIE1, **PIE2**

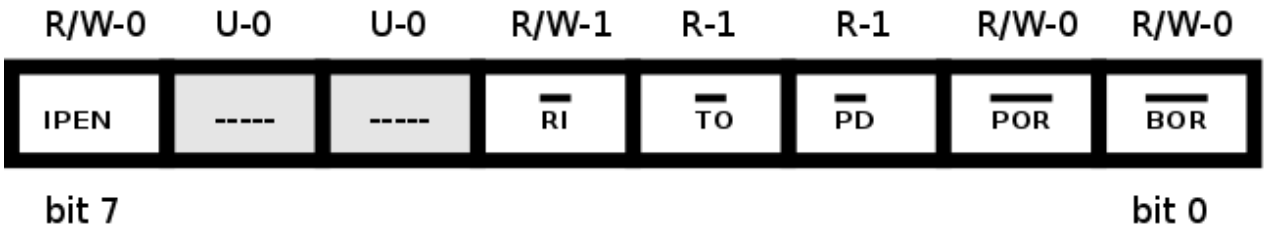
→ Section 6.4.6

IPR1, **IPR2**

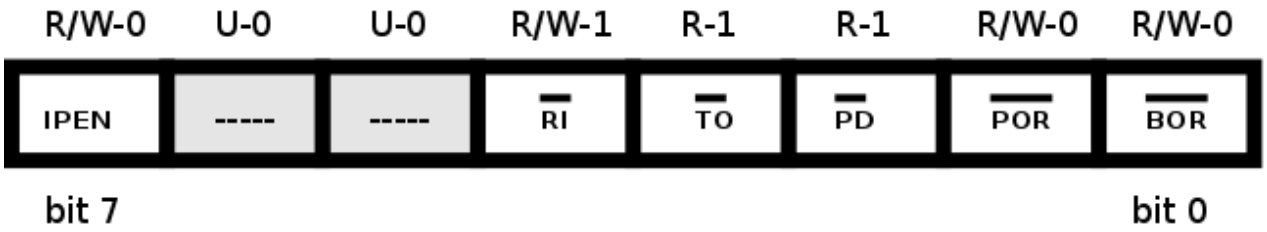
→ Section 6.4.7

RCON

RCON

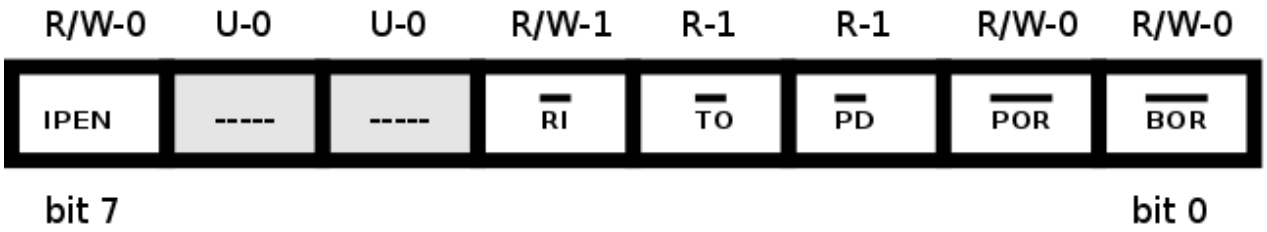


RCON



Bits in RCON register

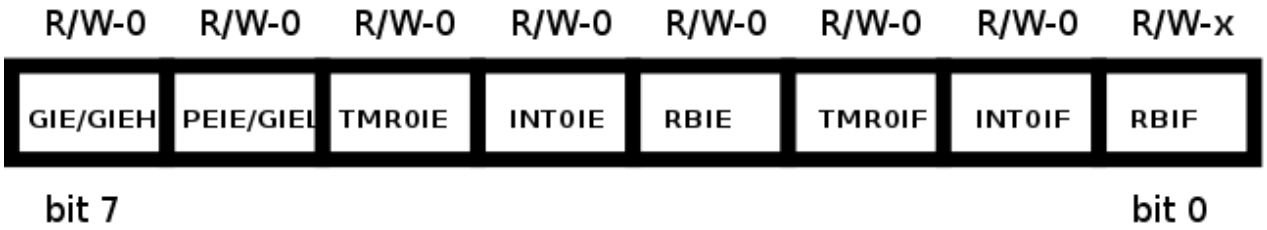
RCON



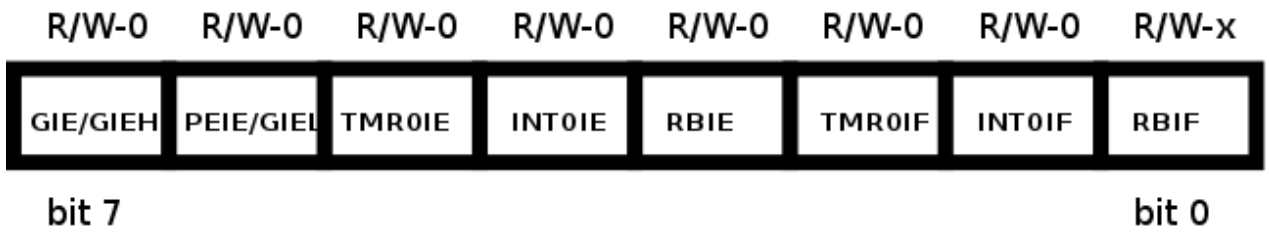
Bits in RCON register -Set IPEN for priority

INTCON

INTCON

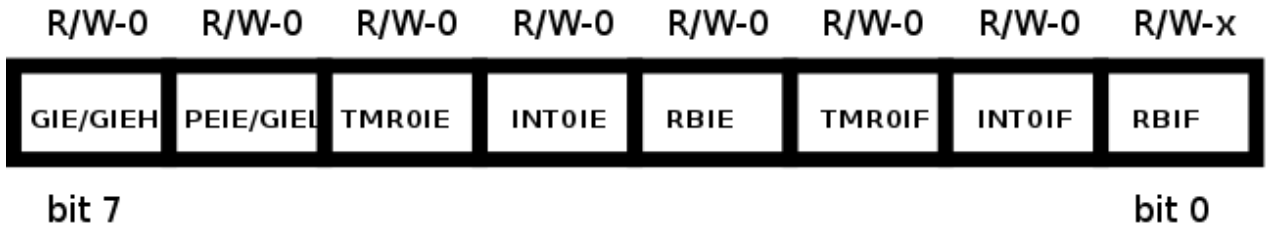

R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-x
GIE/GIEH
PEIE/GIEL
TMR0IE
INT0IE
RBIE
TMR0IF
INT0IF
RBIF
bit 7
bit 0

INTCON



Bits in INTCON register

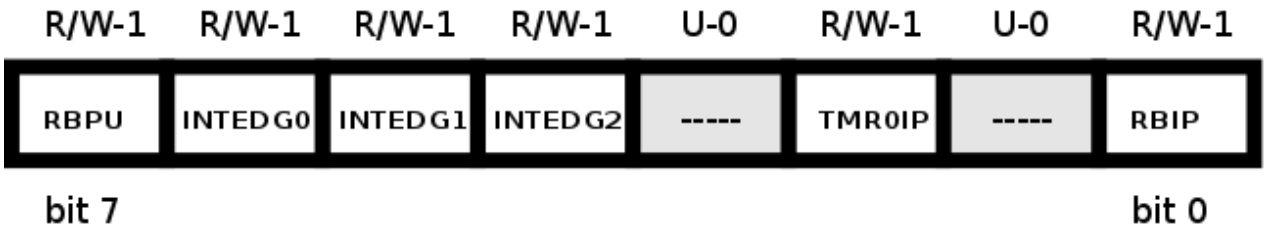
INTCON



Bits in INTCON register -Set GIEH to enable high priority, GIEL to enable low priority (if GIEH set)

INTCON2

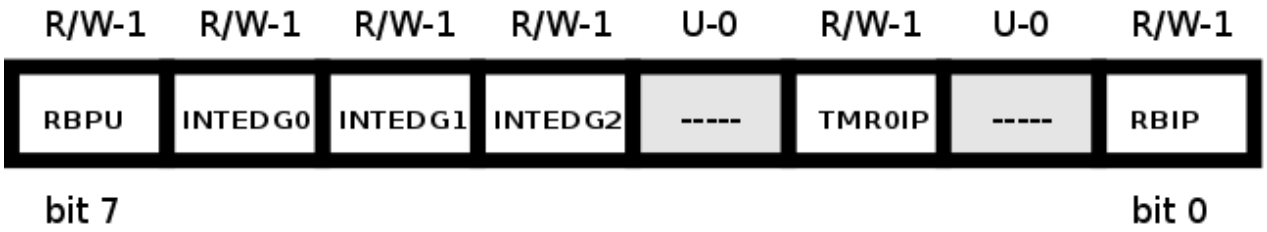
INTCON2


R/W-1
R/W-1
R/W-1
R/W-1
U-0
R/W-1
U-0
R/W-1
RBPU
INTEDG0
INTEDG1
INTEDG2

TMR0IP

RBIP
bit 7
bit 0

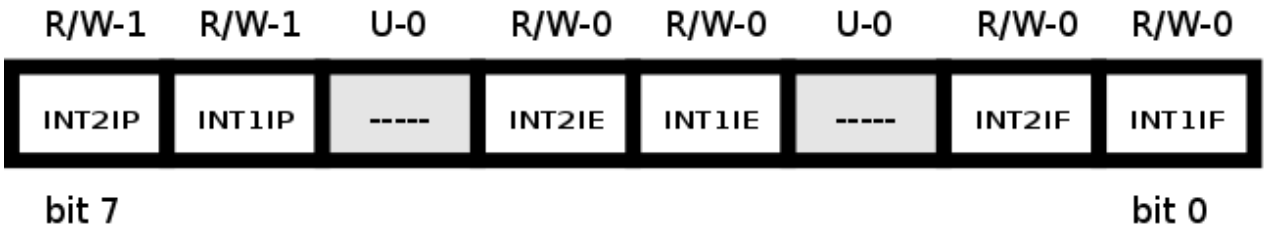
INTCON2



Bits in INTCON2 register

INTCON3

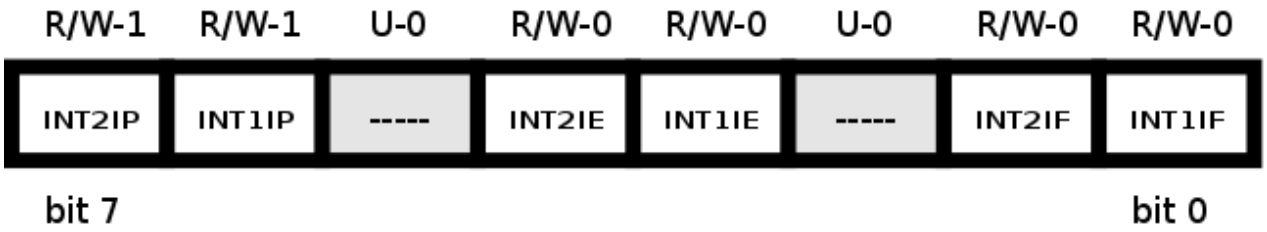
INTCON3


R/W-1
R/W-1
U-0
R/W-0
R/W-0
U-0
R/W-0
R/W-0
INT2IP
INT1IP

INT2IE
INT1IE

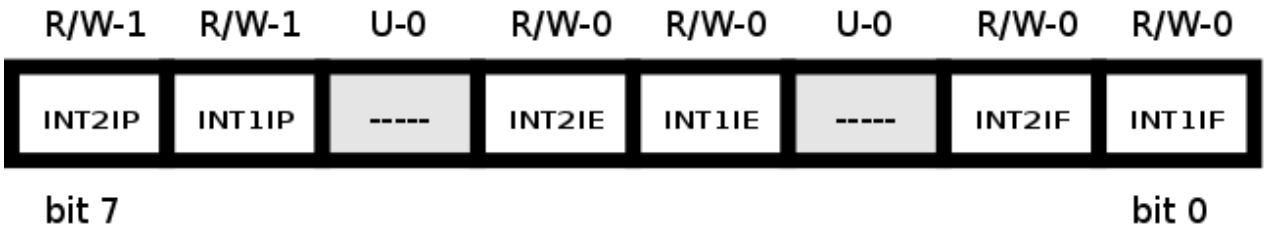
INT2IF
INT1IF
bit 7
bit 0

INTCON3



Bits in INTCON3 register

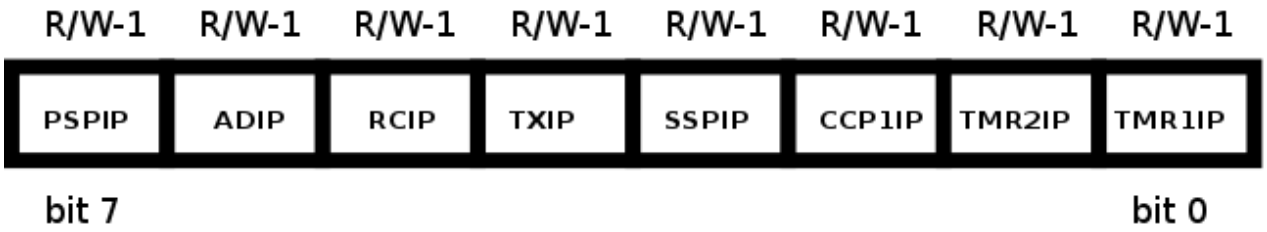
INTCON3



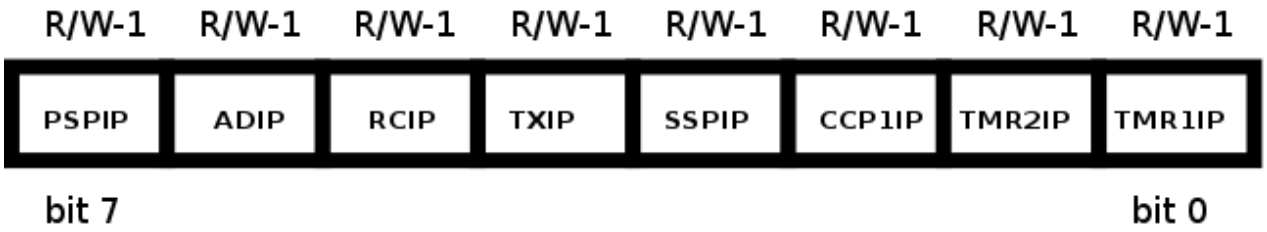
Bits in INTCON3 register -Note INT0 is not mentioned

IPR1

IPR1


R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
PSPIP
ADIP
RCIP
TXIP
SSPIP
CCP1IP
TMR2IP
TMR1IP
bit 7
bit 0

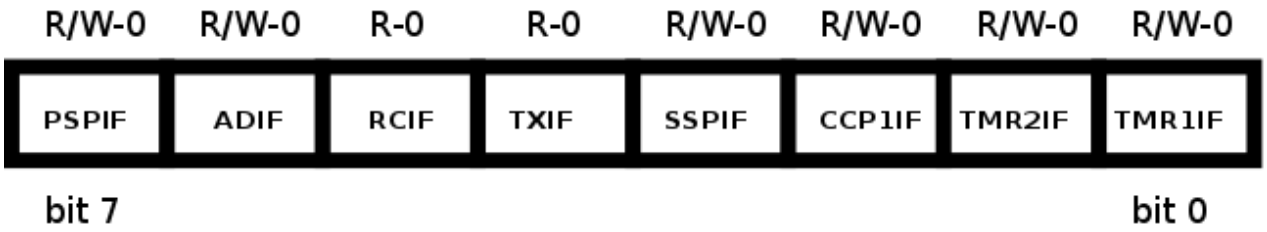
IPR1



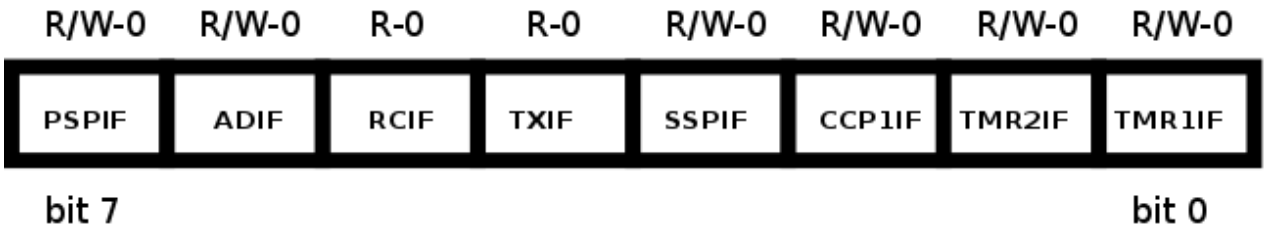
Bits in IPR1 register

PIR1

PIR1


R/W-0
R/W-0
R-0
R-0
R/W-0
R/W-0
R/W-0
R/W-0
PSPIF
ADIF
RCIF
TXIF
SSPIF
CCP1IF
TMR2IF
TMR1IF
bit 7
bit 0

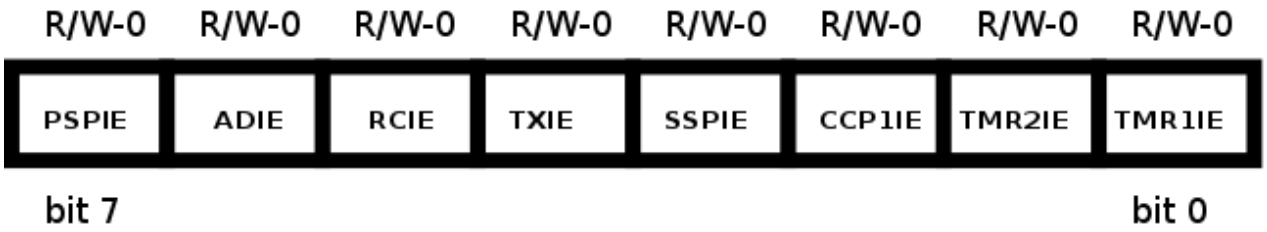
PIR1



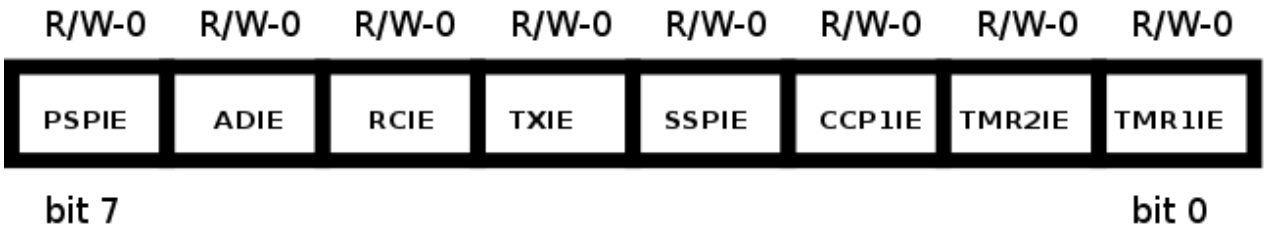
Bits in PIR1 register

PIE1

PIE1


R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
PSPIE
ADIE
RCIE
TXIE
SSPIE
CCP1IE
TMR2IE
TMR1IE
bit 7
bit 0

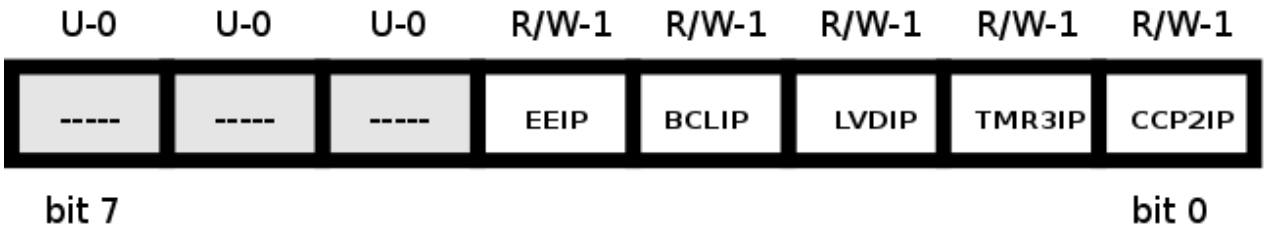
PIE1



Bits in PIE1 register

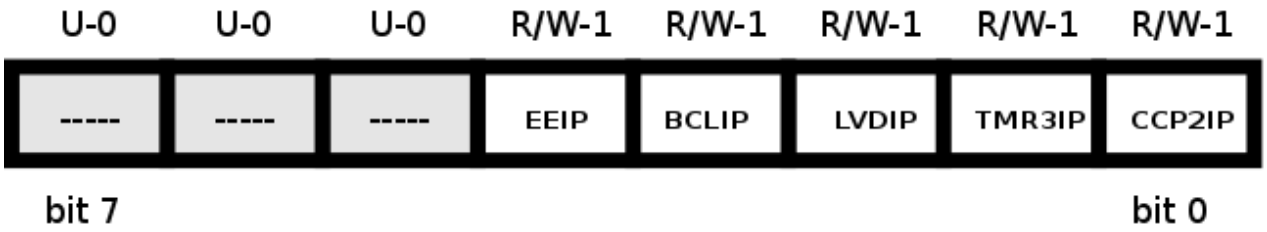
IPR2

IPR2


U-0
U-0
U-0
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1

EEIP
BCLIP
LVDIP
TMR3IP
CCP2IP
bit 7
bit 0

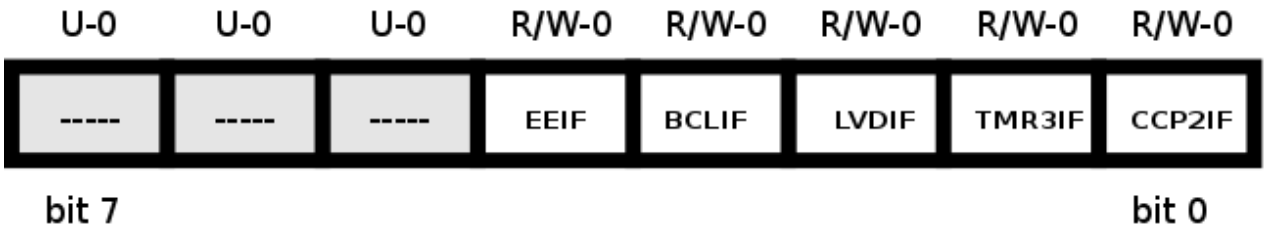
IPR2



Bits in IPR2 register

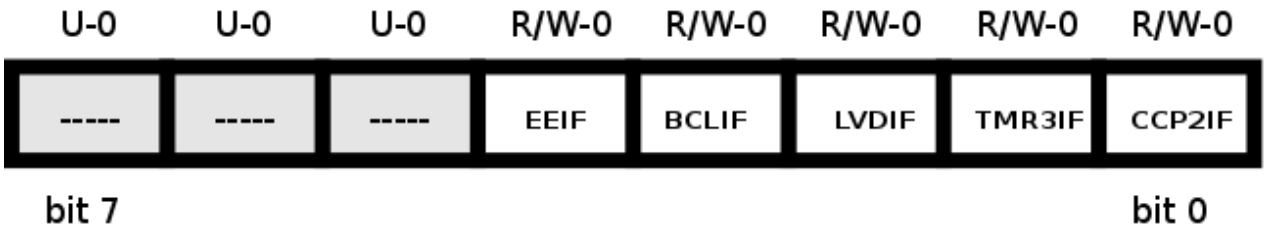
PIR2

PIR2


U-0
U-0
U-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0

EEIF
BCLIF
LVDIF
TMR3IF
CCP2IF
bit 7
bit 0

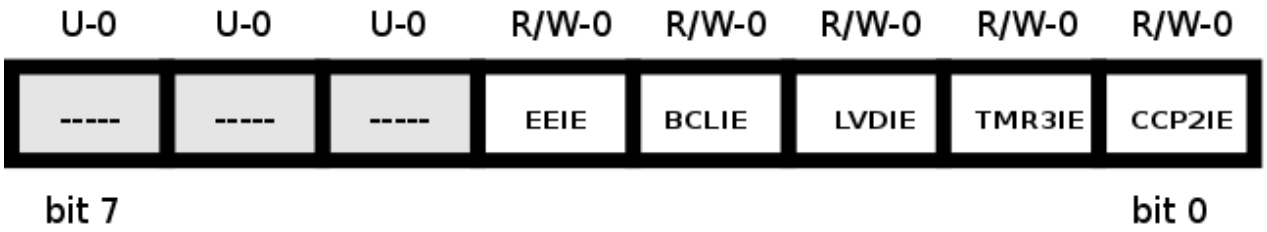
PIR2



Bits in PIR2 register

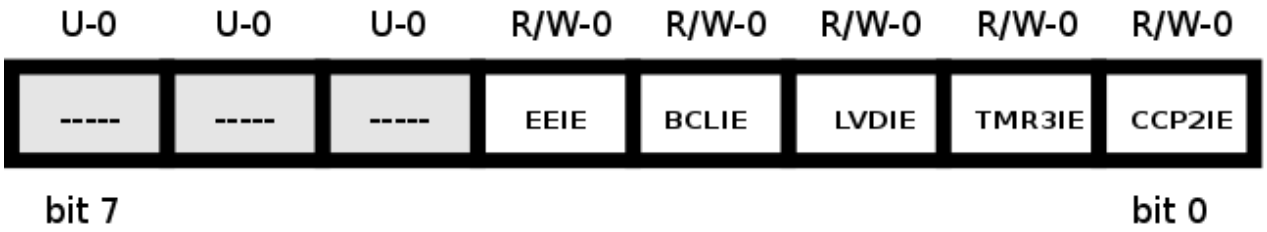
PIE2

PIE2


U-0
U-0
U-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0

EEIE
BCLIE
LVDIE
TMR3IE
CCP2IE
bit 7
bit 0

PIE2



Bits in PIE2 register