CP316
Serial Communication-I2C

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Serial Communication -I^2C

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- Inter-Integrated Circuit Interface

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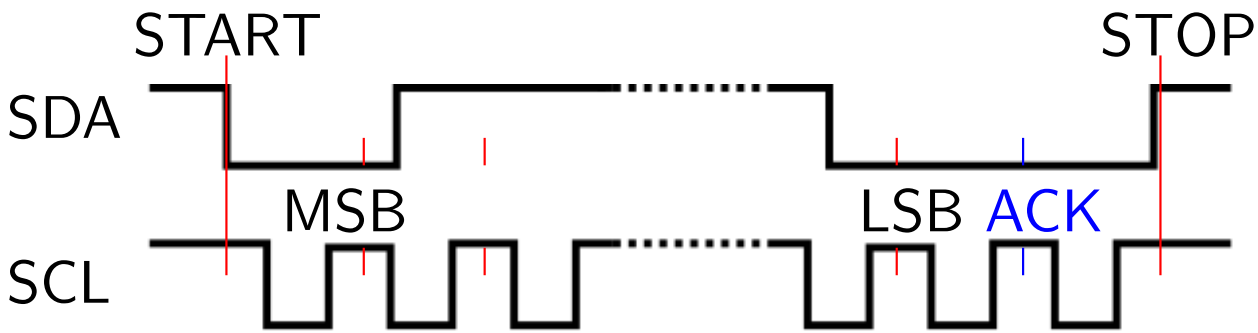
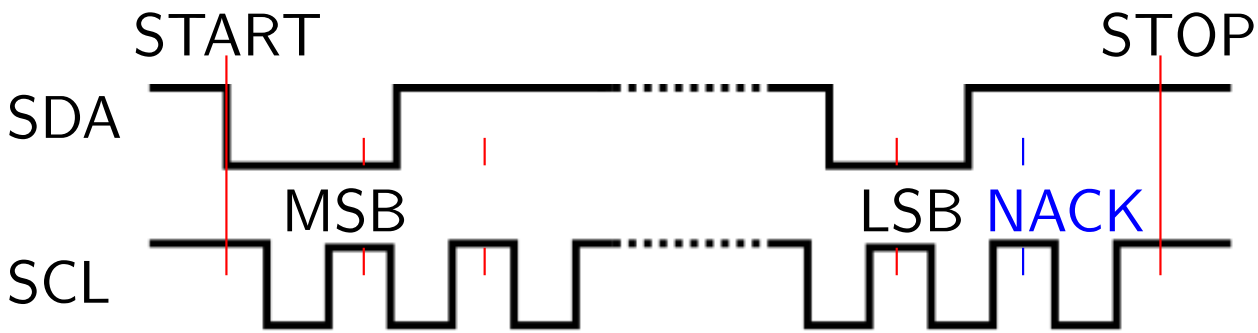
- Synchronous, so master controls clock rate



- I^2C ; bits are read when SCL is HIGH
- ACK is sent by receiver if OK

  sender must release SDA after LSB



- I^2C ; bits are read when SCL is HIGH
- NACK is sent by master-receiver if OK

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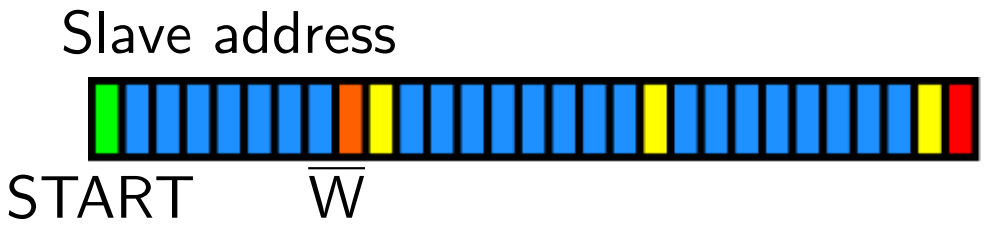
- I^2C write to slave register



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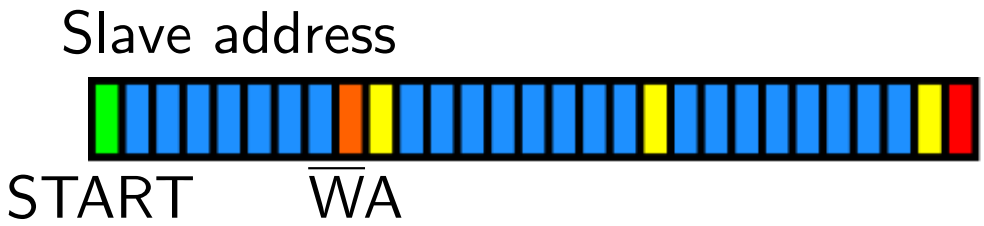

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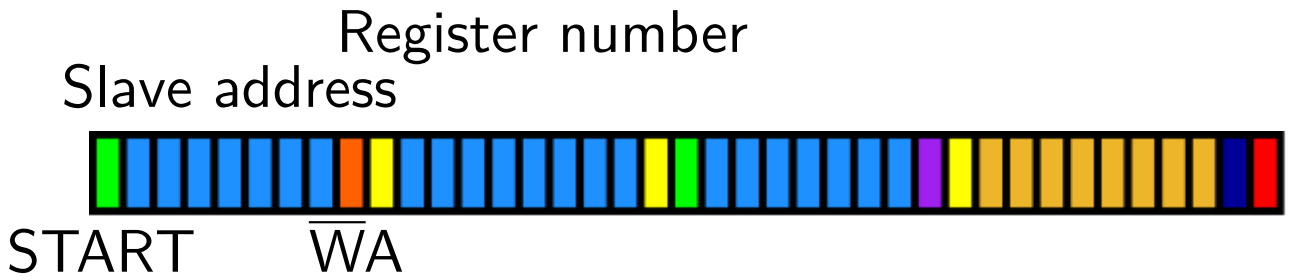

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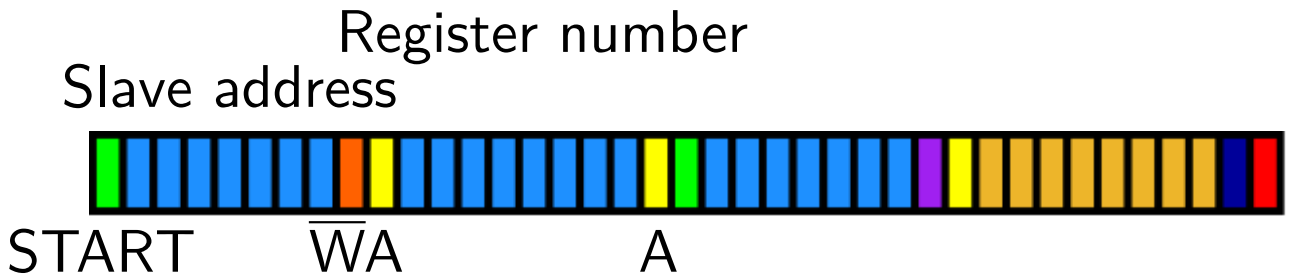

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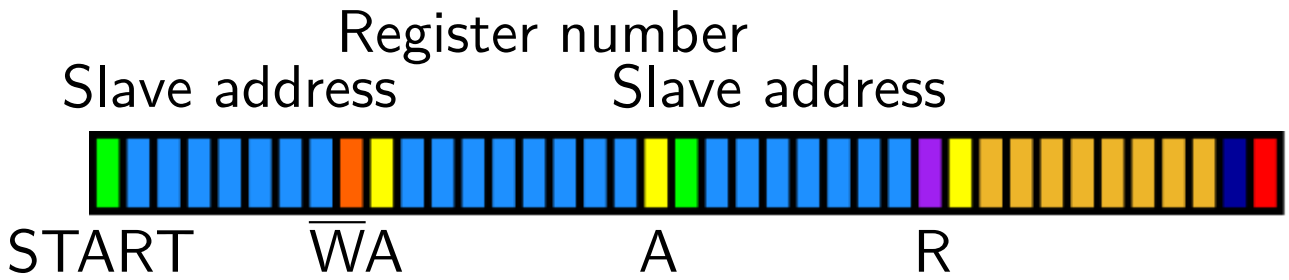

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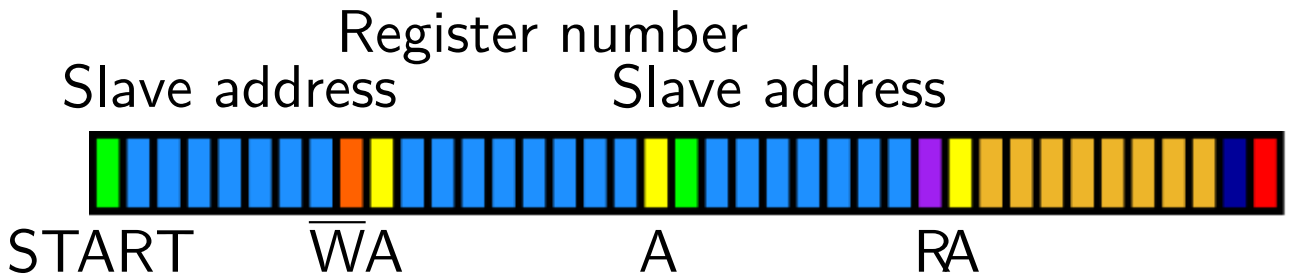

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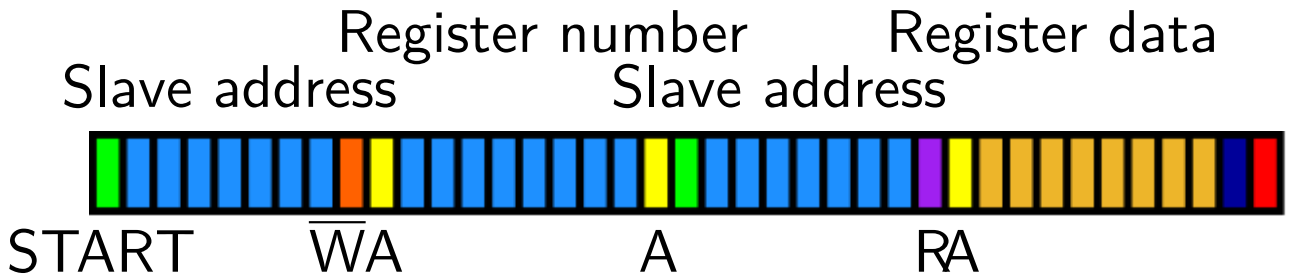

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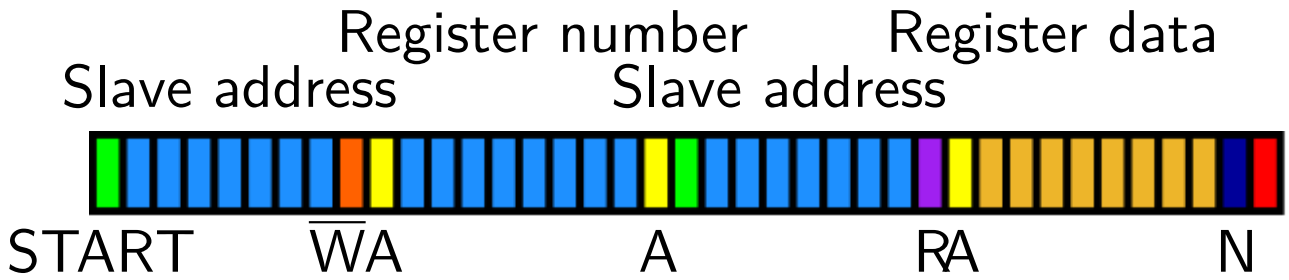
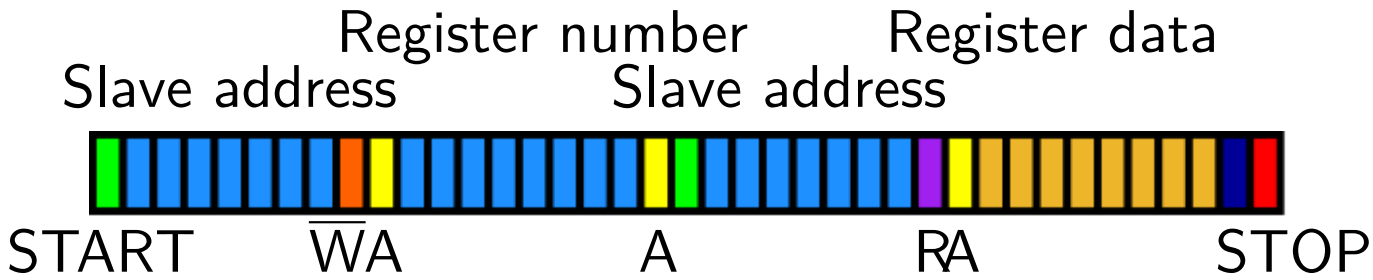


- I^2C read from slave register



- I^2C read from slave register

Introduction

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QwikFlash modules

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QwikFlash modules

ramifications???

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interrupts; transmit and receive

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$\rightarrow$ Sections 6.4.5 to 6.4.7

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QwikFlash modules

ramifications???

interrupts; transmit and receive

→ Sections 6.4.5 to 6.4.7

→ Section 8.2

Master Synchronous Serial Port (MSSP) module

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2 modes; **SPI** and $\mathrm{I}^2\mathrm{C}$

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2 modes; **SPI** and I^2C

$\rightarrow$ Section 15.0 -15.2

I^2C

I^2C

2 wires, master-multiple slave

I^2C

2 wires, master-multiple slave

overview

I^2C

2 wires, master-multiple slave

overview

$\rightarrow$ Section 11.2

I^2C

2 wires, master-multiple slave

overview

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I^2C module

I^2C

2 wires, master-multiple slave

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I^2C module

$\rightarrow$ Sections 11.3 to 11.6

I^2C

2 wires, master-multiple slave

overview

→ Section 11.2

I^2C module

→ Sections 11.3 to 11.6

→ Section 15.4

I^2C summary

I^2C summary

2 wires (+ ground), one-to-many

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2 wires (+ ground), one-to-many

SCL (from master)

I^2C summary

2 wires (+ ground), one-to-many

SCL (from master)

SDA (serial data)

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2 wires (+ ground), one-to-many

SCL (from master)

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data transmission rate set by SCL

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address for each device, preset (but possibly programmable)

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2 wires (+ ground), one-to-many

SCL (from master)

SDA (serial data)

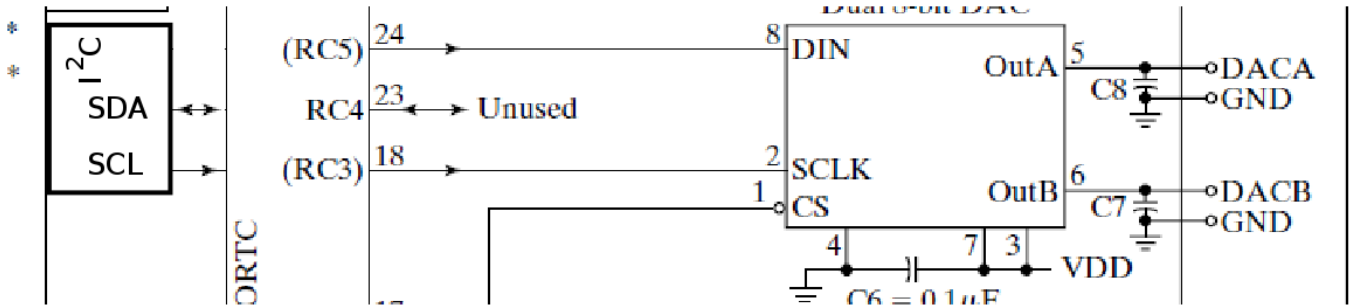
data transmission rate set by SCL

address for each device, preset (but possibly programmable)

packets are complex; address of recipient, read or write, data (variable number of bytes)

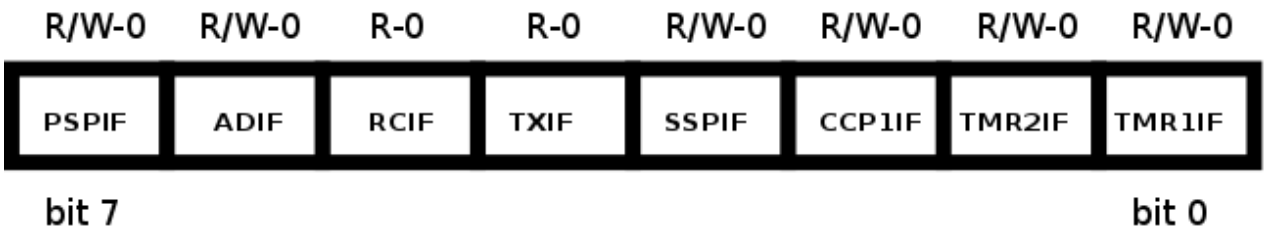
Qwikflash I^2C connections

Qwikflash I^2C connections

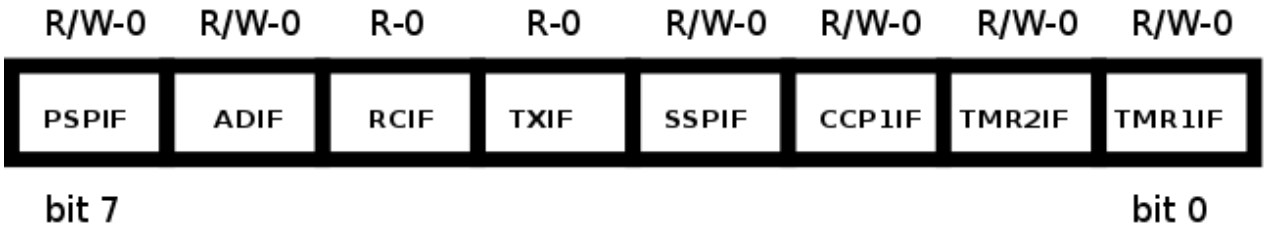


PIR1

PIR1

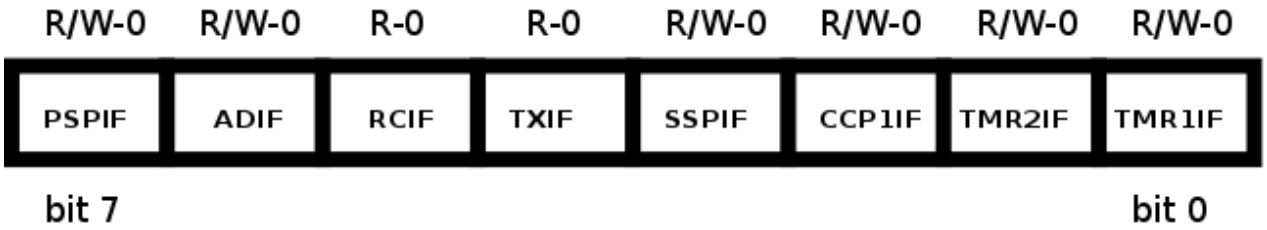

R/W-0
R/W-0
R-0
R-0
R/W-0
R/W-0
R/W-0
R/W-0
PSPIF
ADIF
RCIF
TXIF
SSPIF
CCP1IF
TMR2IF
TMR1IF
bit 7
bit 0

PIR1



Bits in PIR1 register

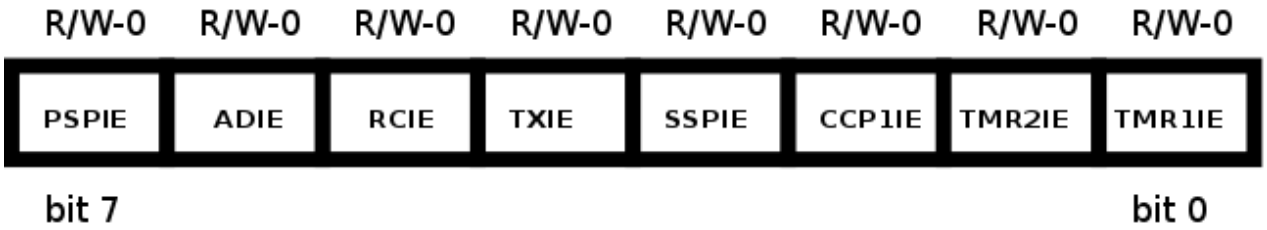
PIR1



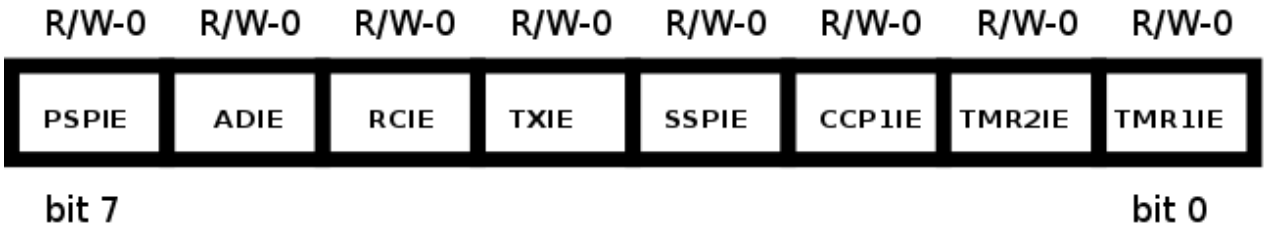
Bits in PIR1 register - Note SSPIF

PIE1

PIE1

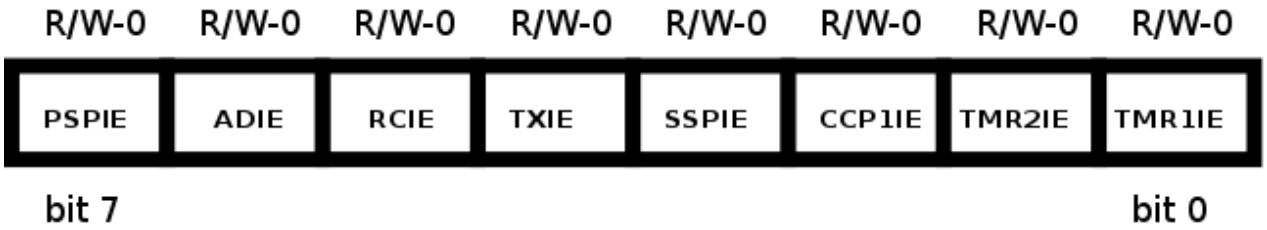

R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
PSPIE
ADIE
RCIE
TXIE
SSPIE
CCP1IE
TMR2IE
TMR1IE
bit 7
bit 0

PIE1



Bits in PIE1 register

PIE1



Bits in PIE1 register - Note SSPIE

IPR1

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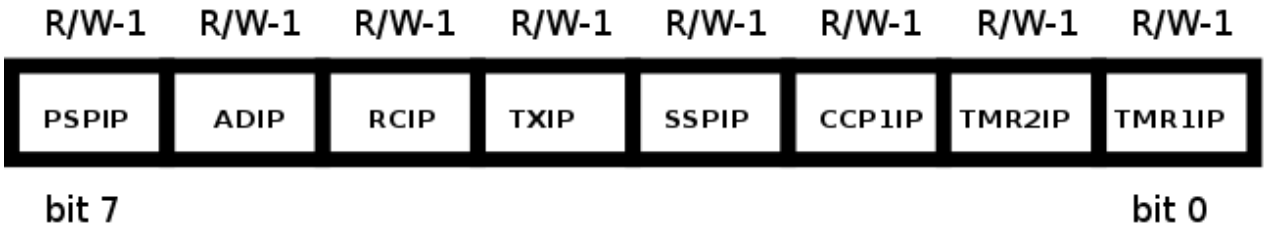
R/W-1
R/W-1
R/W-1
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R/W-1
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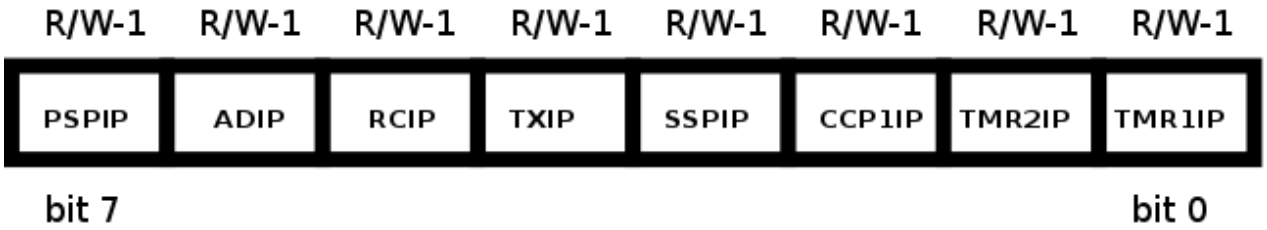
PSPIP
ADIP
RCIP
TXIP
SSPIP
CCP1IP
TMR2IP
TMR1IP
bit 7
bit 0

IPR1



Bits in IPR1 register

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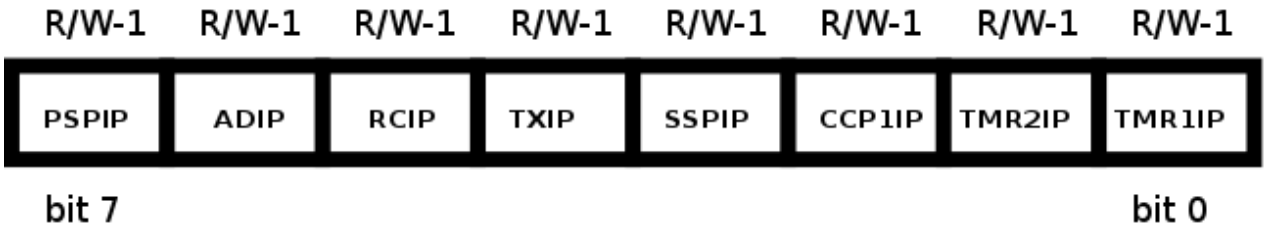

Bits in IPR1 register - Note SSPIP

Bit-bashing

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overview

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reasons

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reasons

NIB

Code

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PORT configuration

Code

PORT configuration

$\rightarrow$ macro or subroutine?

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$\rightarrow$ macro or subroutine?

Initiallization

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Write to device

Code

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