

CP316

Serial Communication-UART

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Serial Communication -UART

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- Universal Asynchronous Receiver Transmitter

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- Universal Asynchronous Receiver Transmitter
- Simplest form of serial communication
- Between 2 devices
- Uses 2 signals (and Ground), Rx and Tx
- Asynchronous, so both must agree on baud rate

Communication parameters

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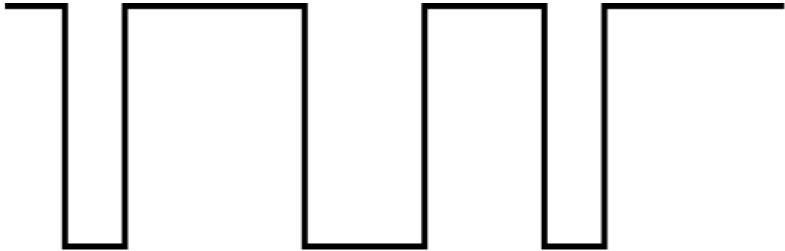
Communication parameters

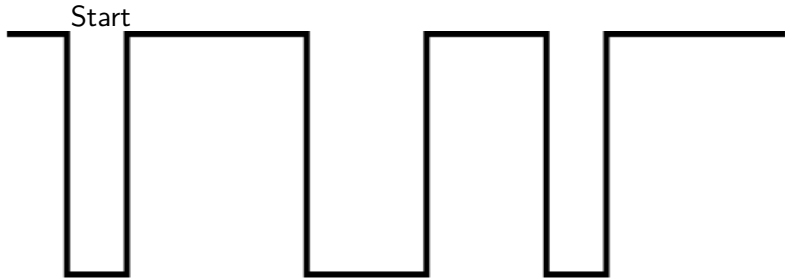
- 1 Start bit at “0” level
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- 1 or 2 Stop bits at “1” level

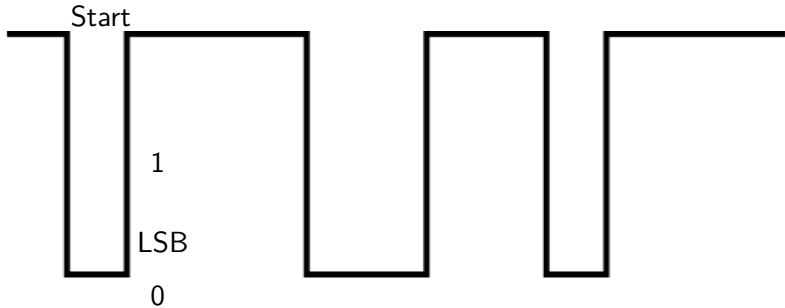
Communication parameters

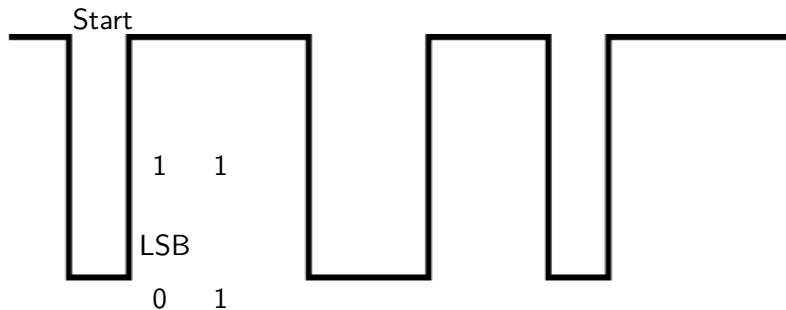
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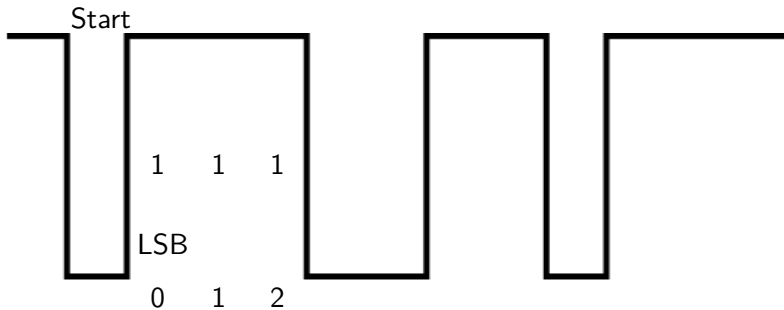
Since start and stop bits are opposite, new characters can always be detected.

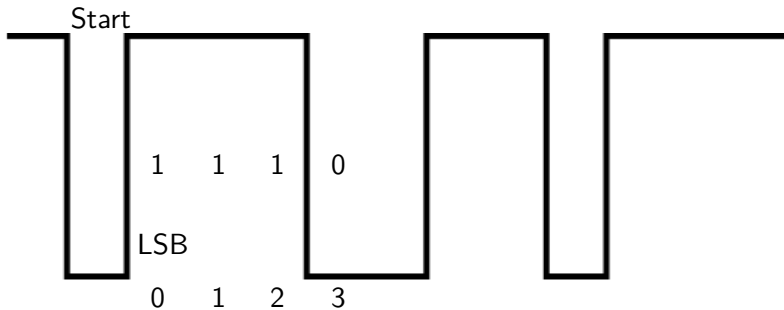


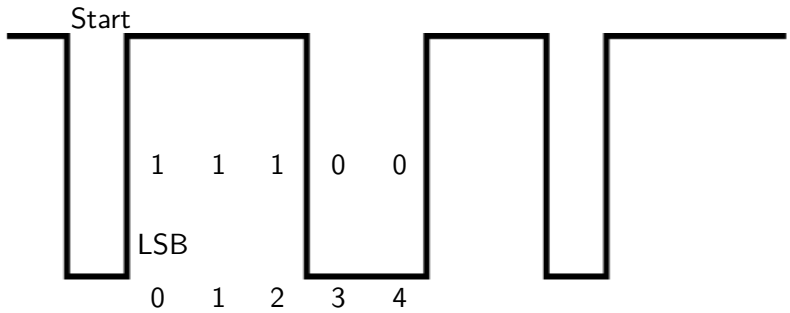


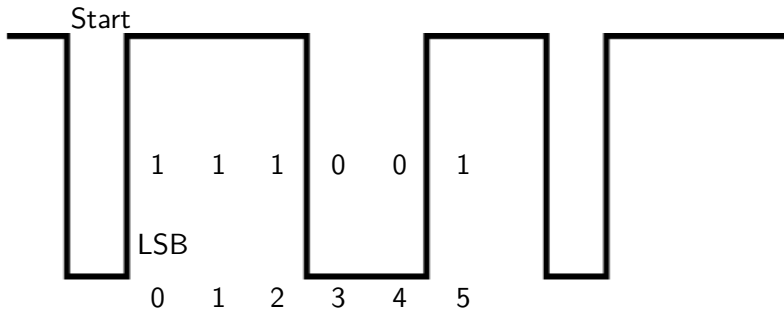


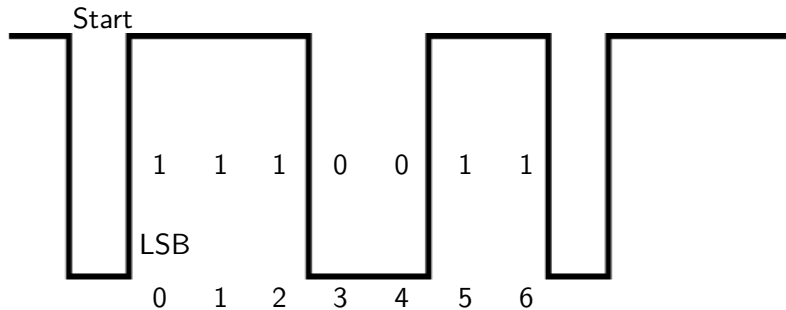


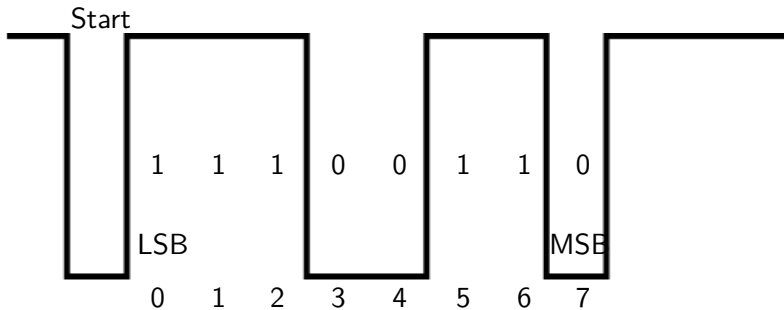


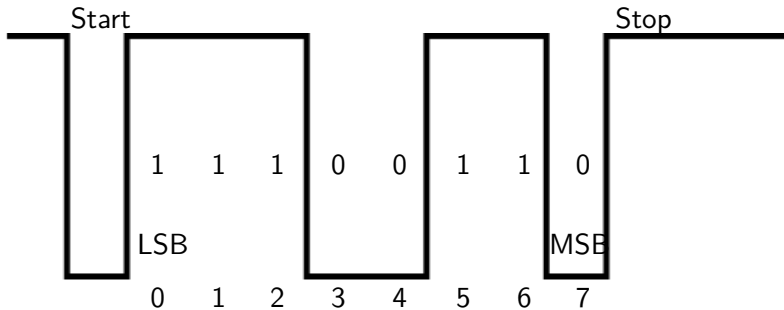


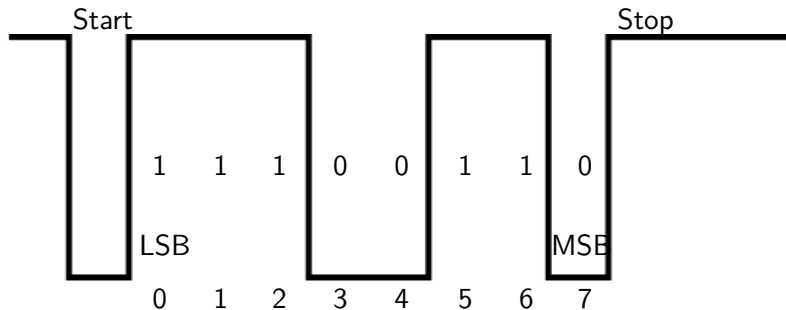




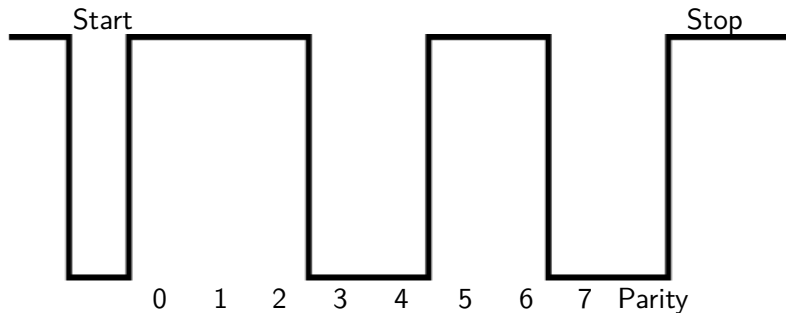


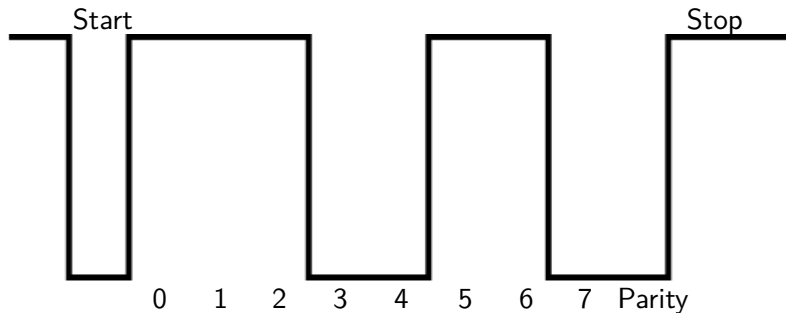




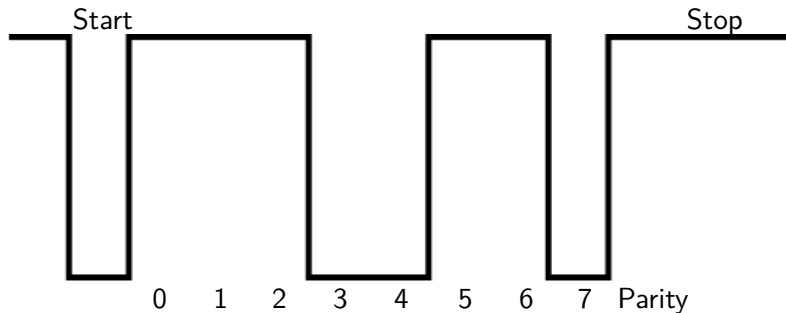


UART no parity - 01100111





UART even parity



UART odd parity

Baud rate calculation

Baud rate calculation

- Baud rate is the number of bits possible in a second

Baud rate calculation

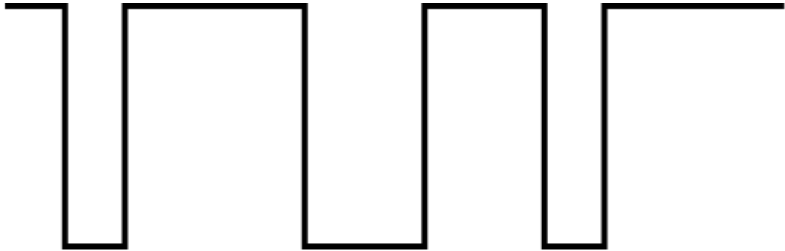
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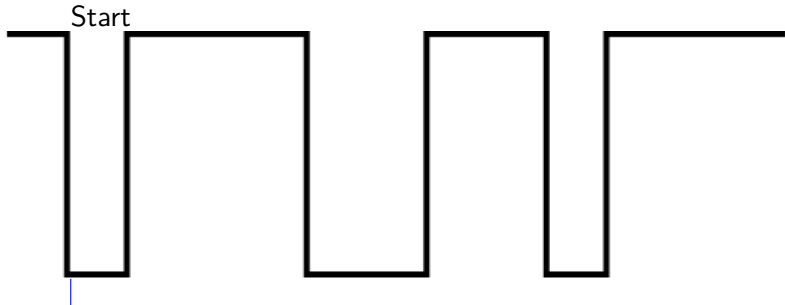
Baud rate calculation

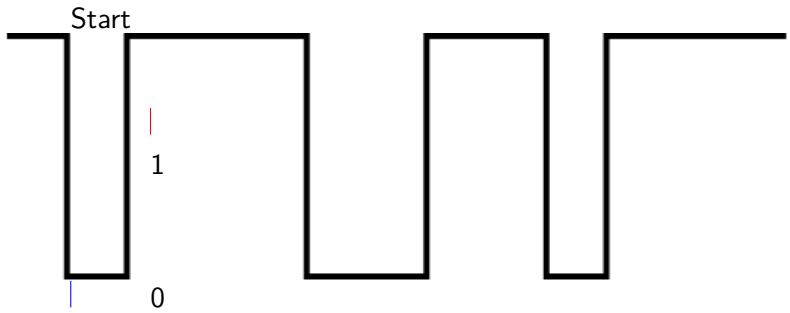
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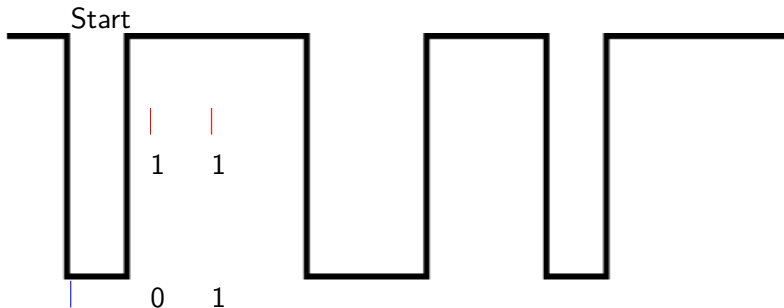
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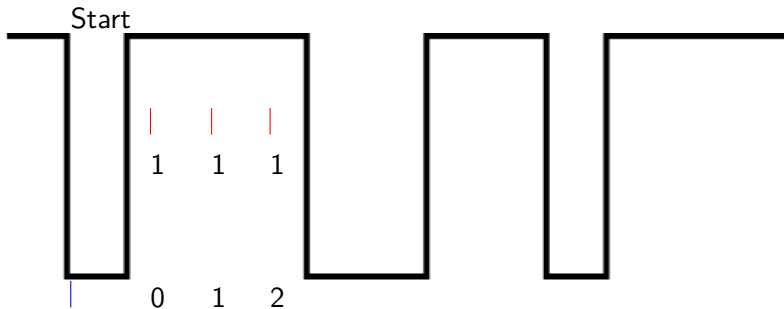
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- After start bit is detected, wait time for $1\frac{1}{2}$ bit to test for first data bit and then after every 1 bit interval
- Resetting at the start bit allows some clock variation

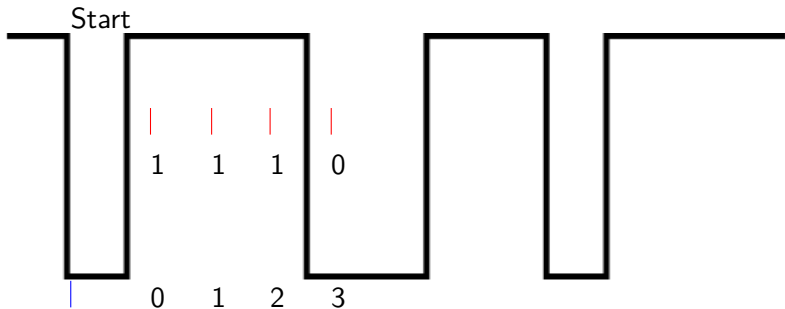


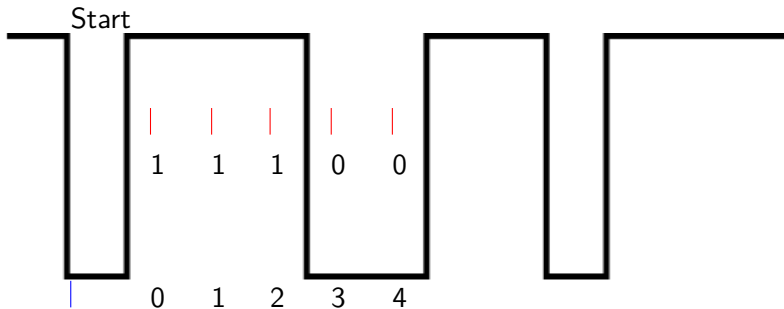


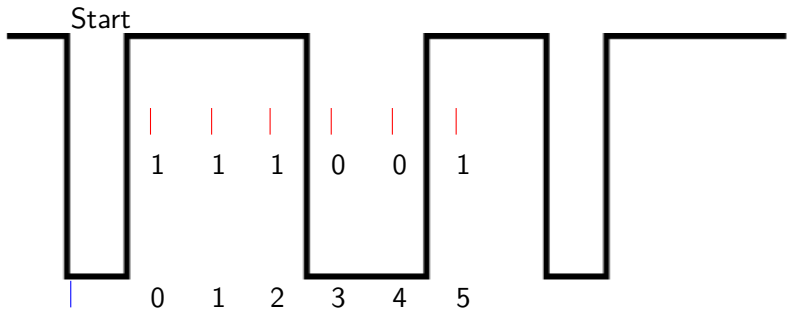


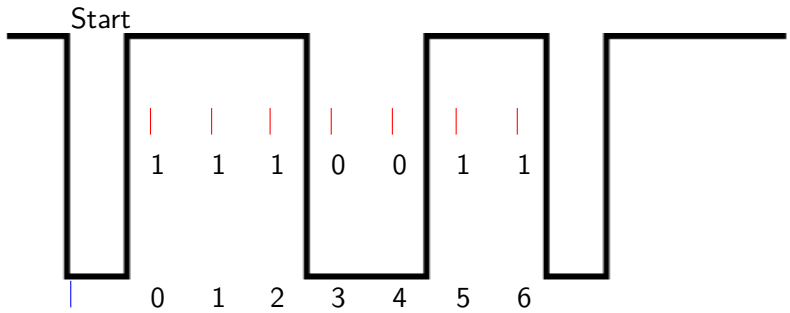


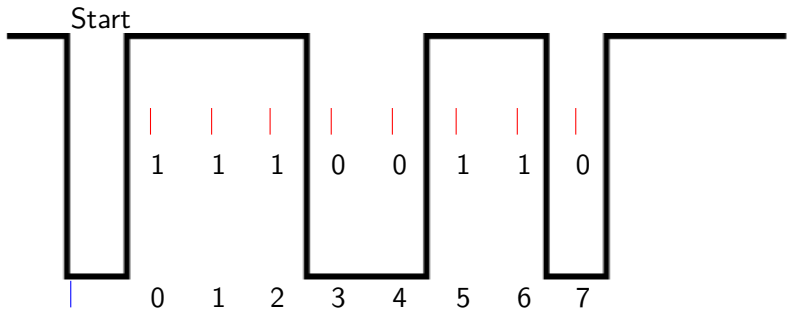


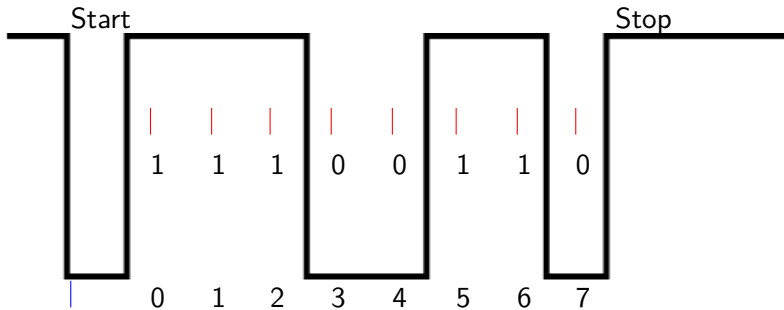


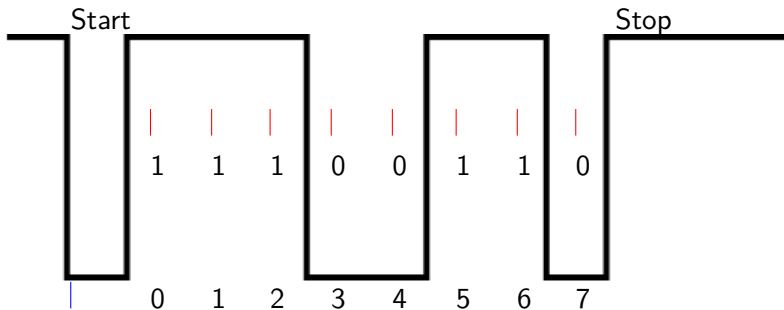












Bit timing

RS232 communication

RS232 communication

- Voltages are inverted

RS232 communication

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- $\pm 3 \rightarrow \pm 12$

RS232 communication

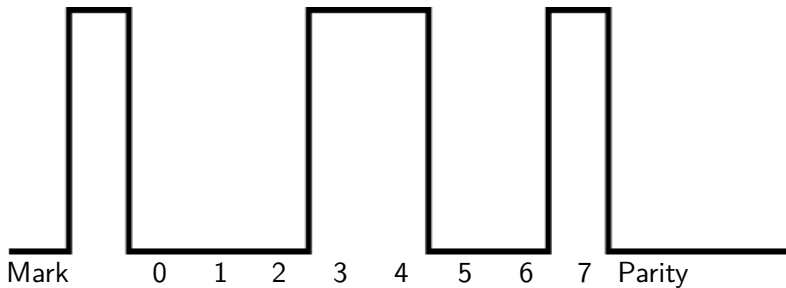
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- Zero is not a valid voltage

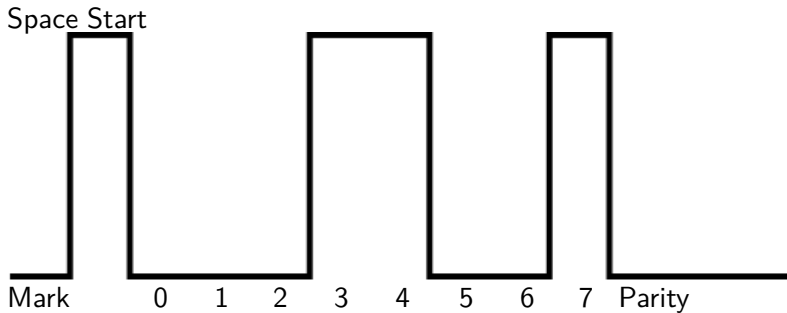
RS232 communication

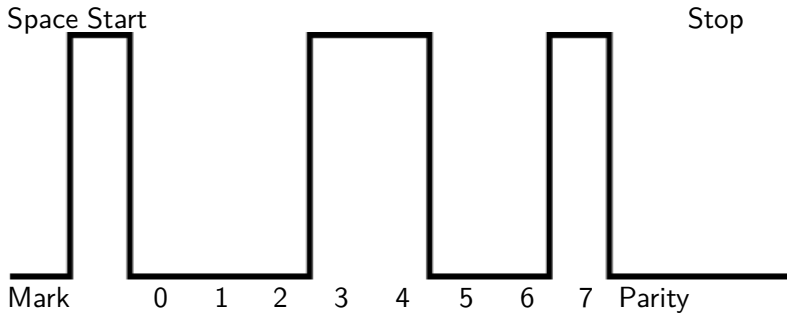
- Voltages are inverted
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- Zero is not a valid voltage
- Mark level (inactive/1) is a negative voltage

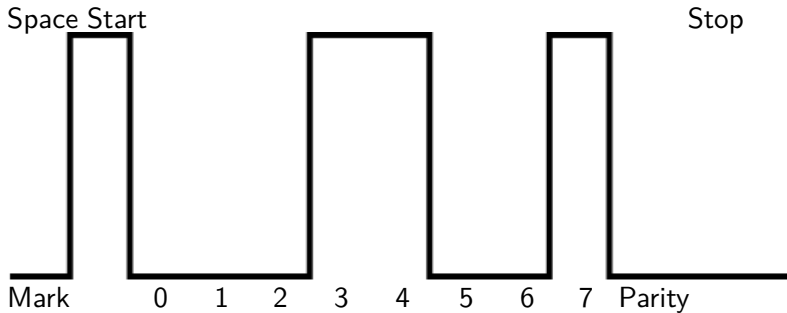
RS232 communication

- Voltages are inverted
- $\pm 3 \rightarrow \pm 12$
- Zero is not a valid voltage
- Mark level (inactive/1) is a negative voltage
- Space level (active/0) is a positive voltage









RS232 levels

Introduction

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QwikFlash modules

Introduction

QwikFlash modules
ramifications???

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QwikFlash modules
ramifications???

interrupts; transmit and receive

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QwikFlash modules
ramifications???

interrupts; transmit and receive
→ Sections 6.4.5 to 6.4.7

Introduction

QwikFlash modules
ramifications???

interrupts; transmit and receive
→ Sections 6.4.5 to 6.4.7
→ **Section 8.2**

USART

USART

2 wires, one-to-one

USART

2 wires, one-to-one
EIA232 (RS232)

USART

2 wires, one-to-one

EIA232 (RS232)

→ Section 9.3

USART

2 wires, one-to-one

EIA232 (RS232)

→ Section 9.3

USART registers

USART

2 wires, one-to-one

EIA232 (RS232)

→ Section 9.3

USART registers

→ Section 9.4.1

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2 wires, one-to-one

EIA232 (RS232)

→ Section 9.3

USART registers

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USART asynchronous mode

USART

2 wires, one-to-one

EIA232 (RS232)

→ Section 9.3

USART registers

→ Section 9.4.1

USART asynchronous mode

→ Section 9.4.2

USART

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EIA232 (RS232)

→ Section 9.3

USART registers

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USART asynchronous mode

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USART asynchronous mode to EIA232

USART

2 wires, one-to-one

EIA232 (RS232)

→ Section 9.3

USART registers

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USART asynchronous mode

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USART asynchronous mode to EIA232

→ Section 9.4.5

USART

2 wires, one-to-one

EIA232 (RS232)

→ Section 9.3

USART registers

→ Section 9.4.1

USART asynchronous mode

→ Section 9.4.2

USART asynchronous mode to EIA232

→ Section 9.4.5

→ **Section 16.0**

EIA232 summary

EIA232 summary

2 wires (+ ground), one-to-one

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2 wires (+ ground), one-to-one
TX

EIA232 summary

2 wires (+ ground), one-to-one

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RX

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2 wires (+ ground), one-to-one

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Fixed baud rate, common to both devices

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At least one *start* bit

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EIA232 summary

2 wires (+ ground), one-to-one

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At least one *stop* bit

voltage levels not TTL; inverted (normally)

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(except “TTL serial” devices)

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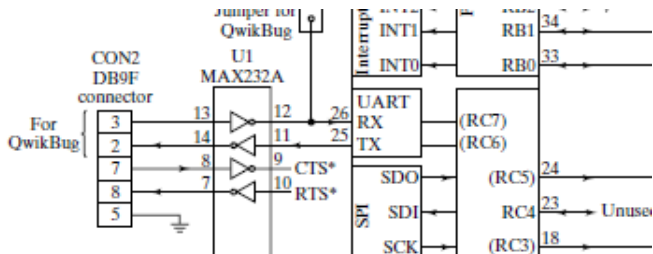
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packets are single characters

Qwikflash UART connections

Qwikflash UART connections



Bit-bashing

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overview

Bit-bashing

overview

reasons

Bit-bashing

overview

reasons

NIB

Code

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PORT configuration

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→ macro or subroutine?

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Initiallization

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