CP316 Timers and Counters

Terry Sturtevant

Wilfrid Laurier University

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Timers and Counters

Timers and Counters

• timers vs. counters

timers vs. counters

A timer counts clock pulses; a counter counts external events

timers vs. counters

A timer counts clock pulses; a counter counts external events size (i.e. number of bits)

timers vs. counters
 A timer counts clock pulses; a counter counts external events
 size (i.e. number of bits)
 output pins

timers vs. counters
 A timer counts clock pulses; a counter counts external events
 size (i.e. number of bits)
 output pins
 prescaler

timers vs. counters

A timer counts clock pulses; a counter counts external events

size (i.e. number of bits)

output pins

prescaler

start/stop

timers vs. counters

A timer counts clock pulses; a counter counts external events

size (i.e. number of bits)

output pins

prescaler

start/stop

interrupt flag

Details
Timer0
Timer1
Timer2

Definitions

Definitions

BOTTOM

Definitions

BOTTOM

value from which the timer starts

Definitions

- BOTTOM
 value from which the timer starts
- MAX

Definitions

- BOTTOM
 - value from which the timer starts
- MAX

maximum value the timer can reach

Definitions

- BOTTOM
 value from which the timer starts
- MAX
 maximum value the timer can reach
- TOP

Definitions

- BOTTOM
 value from which the timer starts
- MAX
 maximum value the timer can reach
- TOP
 highest value in the timer count sequence

Definitions

- BOTTOM
 value from which the timer starts
- MAX
 maximum value the timer can reach
- TOP

highest value in the timer count sequence depending on *mode*, can be less than or equal to MAX

Tn

Tn

Timer *n* input

- Tn
 - Timer *n* input
- OCnx

Pins

Tn

Timer *n* input

OCnx

Output compare pin x for timer n

Tn

Timer *n* input

OCnx

Output compare pin x for timer n

ICPn

Tn

Timer *n* input

OCnx

Output compare pin x for timer n

ICPn

Input capture pin for timer n

Flags

Flags

TOVn

Flags

TOVn

Timer overflow *n*

Flags

- TOVn
 - Timer overflow n
- OCFnx

Flags

TOVn

Timer overflow n

OCFnx

Output compare match x for timer n

Flags

TOVn

Timer overflow *n*

OCFnx

Output compare match x for timer n

ICFn

Flags

TOVn

Timer overflow *n*

OCFnx

Output compare match x for timer n

ICFn

Input capture for timer n

Timer modes

Timer modes

Normal

Timer modes

Normal

rolls over at TOP

Timer modes

- Normal
 - rolls over at TOP
- CTC (Clear Timer on Compare Match)

Timer modes

- Normal
 - rolls over at TOP
- CTC (Clear Timer on Compare Match)
 returns to zero when OCRnx (or ICRn) reached

- Normal rolls over at TOP
- CTC (Clear Timer on Compare Match)
 returns to zero when OCRnx (or ICRn) reached
- Fast PWM

- Normal
 TOP
 - rolls over at TOP
- CTC (Clear Timer on Compare Match) returns to zero when OCRnx (or ICRn) reached
- Fast PWM
 rolls over at TOP

- Normal
 - rolls over at TOP
- CTC (Clear Timer on Compare Match)
 returns to zero when OCRnx (or ICRn) reached
- Fast PWM
 - rolls over at TOP
 - output OCnx set when compare matches TCNTx and OCRnx

- Normal
 - rolls over at TOP
- CTC (Clear Timer on Compare Match)
 returns to zero when OCRnx (or ICRn) reached
- Fast PWM
 - rolls over at TOP
 - output OCnx set when compare matches TCNTx and OCRnx

Timer modes (continued)

Phase correct PWM

Timer modes (continued)

 Phase correct PWM counts BOTTOM to TOP then TOP to BOTTOM

Timer modes (continued)

Phase correct PWM
 counts BOTTOM to TOP then TOP to BOTTOM
 output OCnx cleared on upcount, set on downcount when
 compare matches TCNTx and OCRnx

- Phase correct PWM
 counts BOTTOM to TOP then TOP to BOTTOM
 output OCnx cleared on upcount, set on downcount when
 compare matches TCNTx and OCRnx
- Phase and frequency correct PWM

- Phase correct PWM
 counts BOTTOM to TOP then TOP to BOTTOM
 output OCnx cleared on upcount, set on downcount when
 compare matches TCNTx and OCRnx
- Phase and frequency correct PWM counts BOTTOM to TOP then TOP to BOTTOM

- Phase correct PWM
 counts BOTTOM to TOP then TOP to BOTTOM
 output OCnx cleared on upcount, set on downcount when
 compare matches TCNTx and OCRnx
- Phase and frequency correct PWM
 counts BOTTOM to TOP then TOP to BOTTOM
 output set when ????????? compare matches TCNTx and OCRnx ???

- Phase correct PWM
 counts BOTTOM to TOP then TOP to BOTTOM
 output OCnx cleared on upcount, set on downcount when
 compare matches TCNTx and OCRnx
- Phase and frequency correct PWM
 counts BOTTOM to TOP then TOP to BOTTOM
 output set when ????????? compare matches TCNTx and OCRnx ???

Timer0

counter?

Timer0

counter?

size?

Timer0

counter?

size?

prescaler?

Timer0

counter?

size?

prescaler?

Arduino connections

BOTTOM

Timer0 details

BOTTOM

0×00

Timer0 details

- BOTTOM
 - 0×00
- MAX

- BOTTOM
 - 0x00
- MAX
 - 0xFF

BOTTOM

0x00

MAX

0xFF

maximum value the timer can reach

BOTTOM

0x00

MAX

0xFF

maximum value the timer can reach

TOP

BOTTOM

 0×00

MAX

0xFF

maximum value the timer can reach

TOP

MAX or value in OCR0A, depending on mode

Figure 15-1. 8-bit Timer/Counter Block Diagram

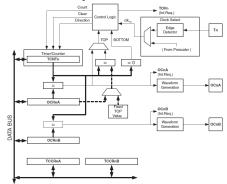
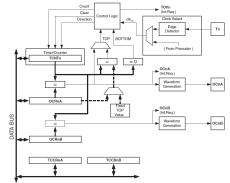


Figure 15-1. 8-bit Timer/Counter Block Diagram

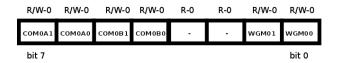


TCCR0A register

TCCR0A register

R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0
COM0A1	сомодо	сомові	сомово		•	WGM01	WGM00
bit 7							bit 0

TCCR0A register



Bits in TCCR0A register

TCCR0A register



Bits in TCCR0A register

COM Output compare bits

WGM Waveform generation mode bits

Timers and Counters

Details
Timer0
Timer1
Timer2
16 bit register access

TCCR0B register

TCCR0B register

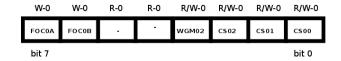


TCCR0B register



Bits in TCCR0B register

TCCR0B register



Bits in TCCR0B register

FOC Force output compare bits

WGM Waveform generation mode bits

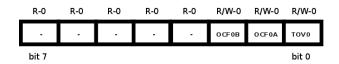
CS Clock select bits

TIFR0 register

TIFR0 register

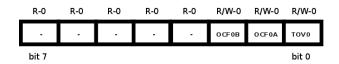
R-0	R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0
-		-		-	OCF0B	O CF 0A	TOV0
bit 7							bit 0

TIFR0 register



Bits in TIFR0 register

TIFR0 register



Bits in TIFR0 register

OCF Output compare flag bits

TOV Timer overflow flag bits

Timer1

counter?

Timer1

counter?

size?

Timer1

counter?

size?

prescaler?

Timer1

counter?

size?

prescaler?

Arduino connections

Timer1 details

Timer1 details

BOTTOM

Timer1 details

BOTTOM

0x0000

Timer1 details

- **BOTTOM** 0×0000
- MAX

Timer1 details

- BOTTOM
 - 0x0000
- MAX
 - 0xFFFF



Timer1 details

BOTTOM

0x0000

MAX

0xFFFF

maximum value the timer can reach

Timer1 details

BOTTOM

0x0000

MAX

0xFFFF

maximum value the timer can reach

TOP

Timer1 details

BOTTOM

0x0000

MAX

0×FFFF

maximum value the timer can reach

TOP

0x00FF, 0x01FF, or 0x03FF, or to the value stored in the OCR1A or ICR1, depending on mode

Figure 16-1. 16-bit Timer/Counter Block Diagram⁽¹⁾

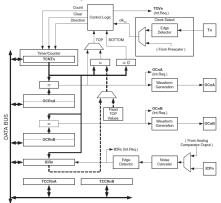
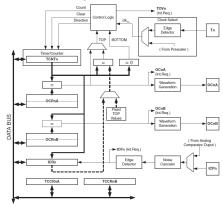


Figure 16-1. 16-bit Timer/Counter Block Diagram(1)



TCCR1A register

TCCR1A register

R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0
COM1A1	COM1A0	соміві	сом1во		•	WGM11	WGM10
bit 7							bit 0



TCCR1A register



Bits in TCCR1A register



TCCR1A register



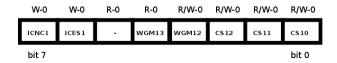
Bits in TCCR1A register

COM Output compare bits

WGM Waveform generation mode bits

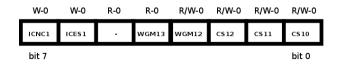
TCCR1B register

TCCR1B register



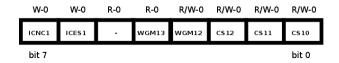


TCCR1B register



Bits in TCCR1B register

TCCR1B register



Bits in TCCR1B register

ICNC Input capture noise canceler bit

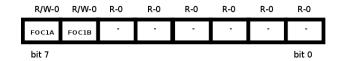
ICES Input capture edge select bit

WGM Waveform generation mode bits

CS Clock select bits

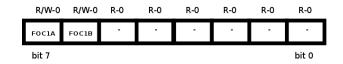
TCCR1C register

TCCR1C register





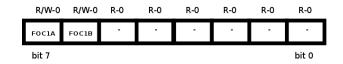
TCCR1C register



Bits in TCCR1C register



TCCR1C register

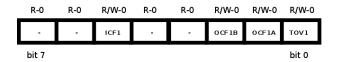


Bits in TCCR1C register

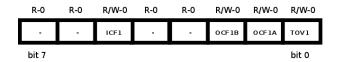
FOC Force output compare bits

TIFR1 register

TIFR1 register



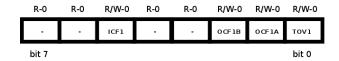
TIFR1 register



Bits in TIFR1 register



TIFR1 register



Bits in TIFR1 register

ICF Input capture flag bit

OCF Output compare flag bits

TOV Timer overflow flag bits

Timer2

counter?

Timer2

counter?

size?

Timer2

counter?

size?

prescaler?

counter?

size?

prescaler?

Arduino connections

Timer2 details

BOTTOM

Timer2 details

BOTTOM

0×00

Timer2 details

- BOTTOM
 - 0×00
- MAX

Timer2 details

- BOTTOM
 - 0×00
- MAX
 - 0xFF

BOTTOM

0x00

MAX

0xFF

maximum value the timer can reach

BOTTOM

0x00

MAX

0xFF

maximum value the timer can reach

TOP

BOTTOM

 0×00

MAX

0xFF

maximum value the timer can reach

TOP

MAX or the value stored in the OCR2A, depending on mode

Figure 18-1. 8-bit Timer/Counter Block Diagram

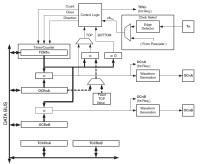
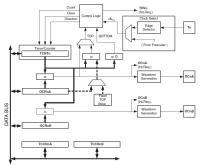


Figure 18-1. 8-bit Timer/Counter Block Diagram



TCCR2A register

TCCR2A register

R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0
COM2A1	COM2A0	сом2В1	сом2во	•	-	WGM21	WGM20
bit 7							bit 0

TCCR2A register



Bits in TCCR2A register

TCCR2A register



Bits in TCCR2A register

COM Output compare bits

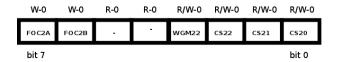
WGM Waveform generation mode bits

Timers and Counters

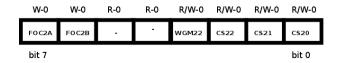
Details
Timer0
Timer1
Timer2
16 bit register acce

TCCR2B register

TCCR2B register

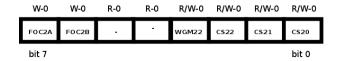


TCCR2B register



Bits in TCCR2B register

TCCR2B register



Bits in TCCR2B register

FOC Force output compare bits

WGM Waveform generation mode bits

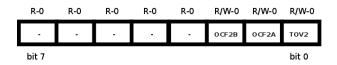
CS Clock select bits

TIFR2 register

TIFR2 register

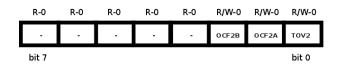
R-0)	R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0
		-	•		•	OCF2B	OCF2A	TOV2
bit	7							bit 0

TIFR2 register



Bits in TIFR2 register

TIFR2 register



Bits in TIFR2 register

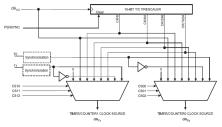
OCF Output compare flag bits

TOV Timer overflow flag bits

Timer 0-1 prescaler

Timer 0-1 prescaler

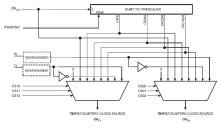
Figure 17-2. Prescaler for Timer/Counter0 and Timer/Counter1(1)



Note: 1. The synchronization logic on the input pins (T1/T0) is shown in Figure 17-1.

Timer 0-1 prescaler

Figure 17-2. Prescaler for Timer/Counter0 and Timer/Counter1(1)



Note: 1. The synchronization logic on the input pins (T1/T0) is shown in Figure 17-1.

Timer 0-1 prescaler

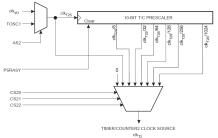


Timer 2 prescaler

Timer 2 prescaler

18.10 Timer/Counter Prescaler

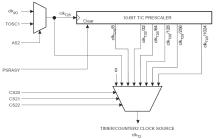
Figure 18-12. Prescaler for Timer/Counter2



Timer 2 prescaler

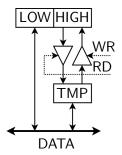
18.10 Timer/Counter Prescaler

Figure 18-12. Prescaler for Timer/Counter2



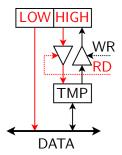
Timer 2 prescaler





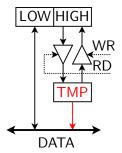
16 bit register access





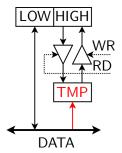
Reading LOW byte latches HIGH byte





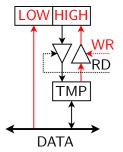
Reading HIGH byte gets value from latch





Writing HIGH byte places value in latch





Writing LOW byte transfers value from latch

