CP316
Serial Communication-SPI

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Serial Communication -SPI

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- Serial Peripheral Interface

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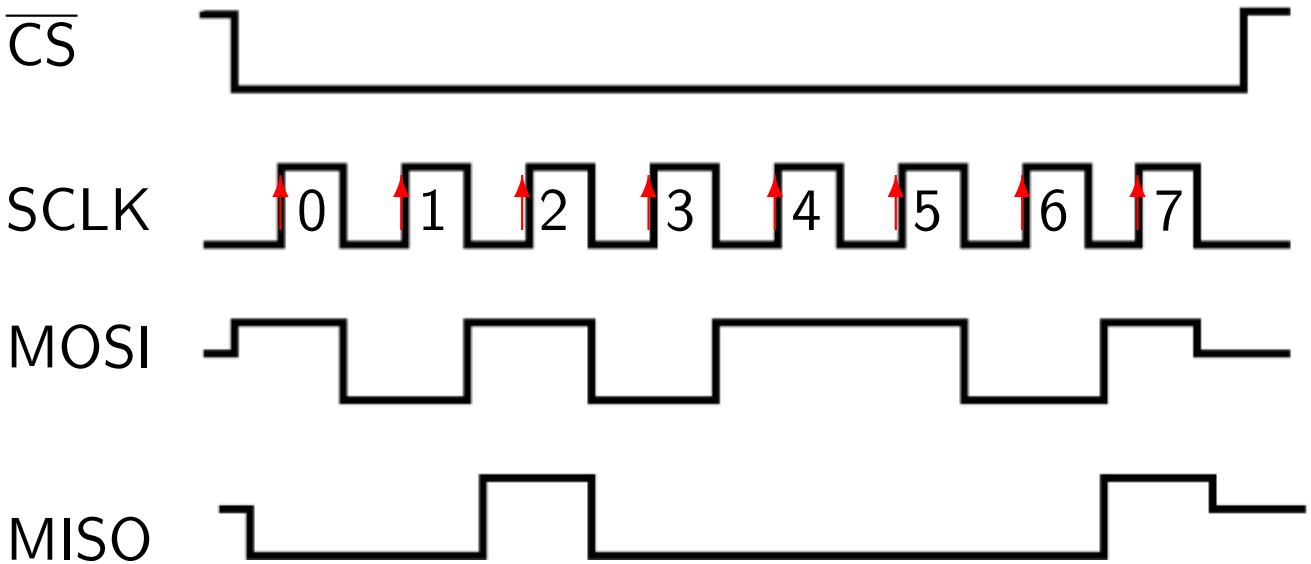
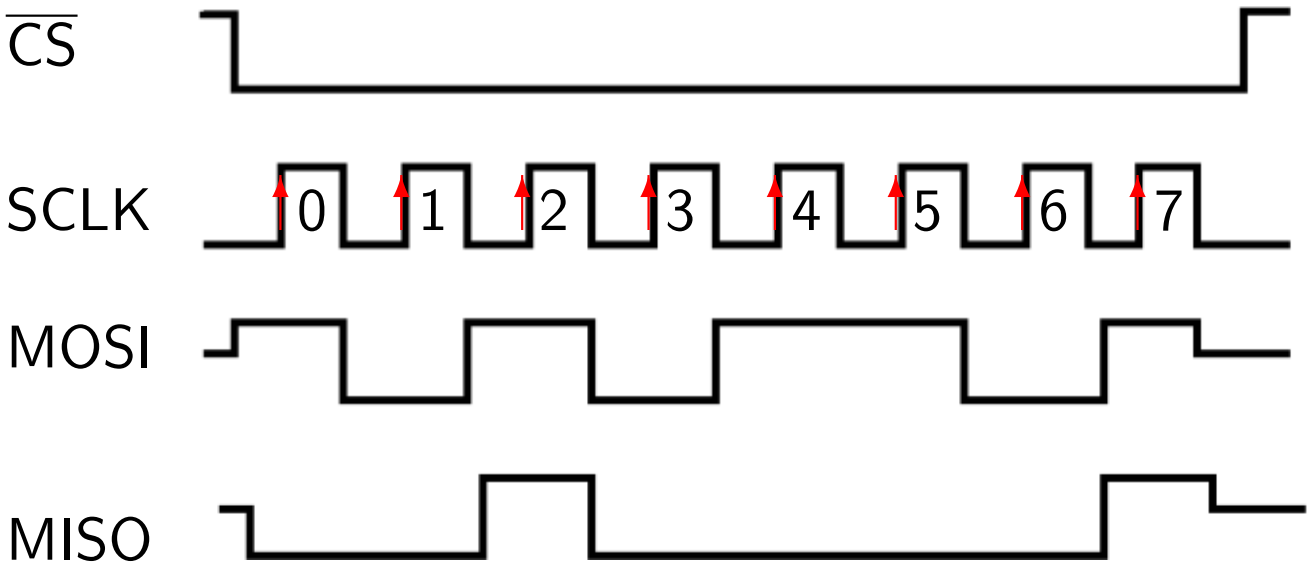
- Synchronous, so master controls clock rate


$\overline{CS}$
SCLK
0
1
2
3
4
5
6
7
MOSI
MISO



SPI transfers can happen in both directions simultaneously.

Introduction

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QwikFlash modules

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QwikFlash modules

ramifications???

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interrupts; transmit and receive

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$\rightarrow$ Sections 6.4.5 to 6.4.7

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interrupts; transmit and receive

→ Sections 6.4.5 to 6.4.7

→ Section 8.2

QwikFlash SPI connections

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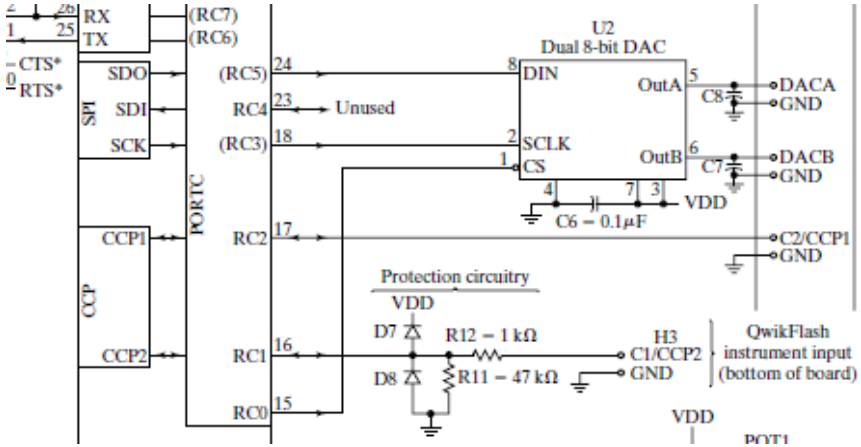

Master Synchronous Serial Port (MSSP) module

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2 modes; **SPI** and I^2C

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→ Section 15.0 -15.2

SPI

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3 wires +chip select, master-slave

SPI

3 wires +chip select, master-slave

overview

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overview

→ Section 10.2

SPI

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overview

→ Section 10.2

SPI registers

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overview

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SPI registers

→ Section 10.3.1

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3 wires +chip select, master-slave

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→ Section 10.2

SPI registers

→ Section 10.3.1

operation

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operation

→ Sections 10.3.2 to 10.3.5

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operation

→ Sections 10.3.2 to 10.3.5

→ Section 15.3

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SPI registers

→ Section 10.3.1

operation

→ Sections 10.3.2 to 10.3.5

→ Section 15.3

QwikFlash MAX522 DAC

SPI summary

SPI summary

3 wires (+ ground), one-to-many

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3 wires (+ ground), one-to-many

SCLK (from master)

SPI summary

3 wires (+ ground), one-to-many

SCLK (from master)

SDO (serial data out)

SPI summary

3 wires (+ ground), one-to-many

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data transmission rate set by SCLK

SPI summary

3 wires (+ ground), one-to-many

SCLK (from master)

SDO (serial data out)

SDI (serial data in)

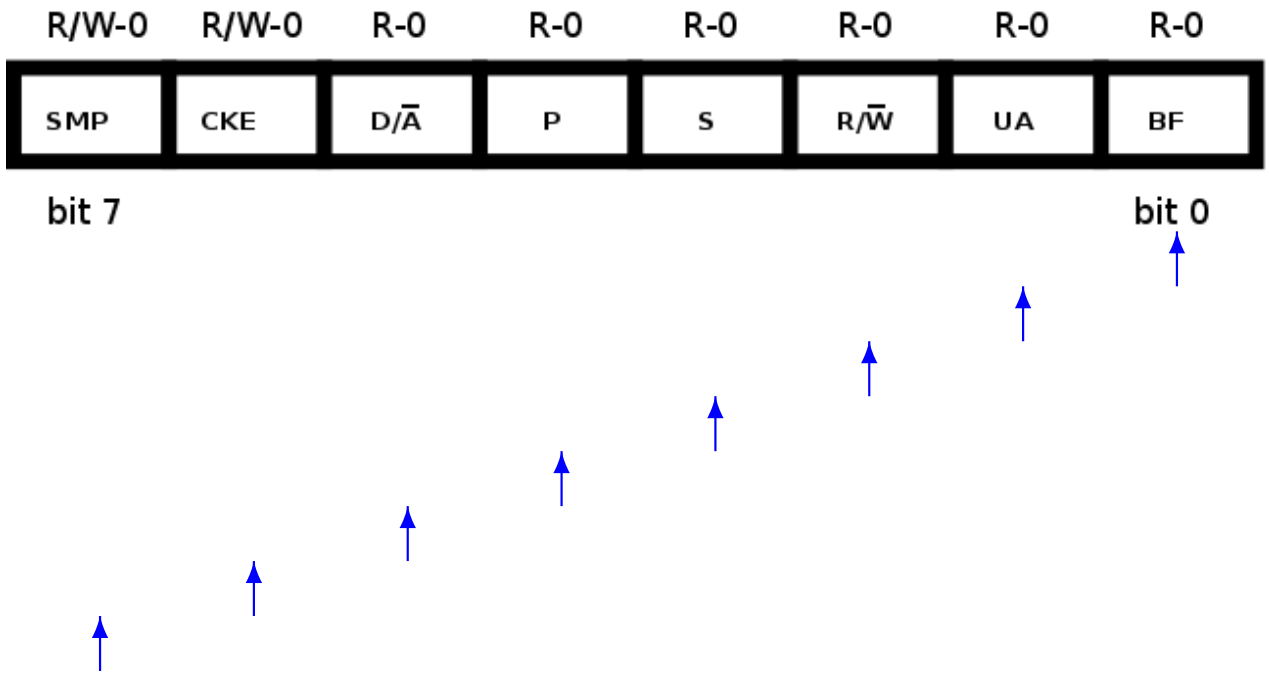
$\overline{CS}$ for each device, generated by master

data transmission rate set by SCLK

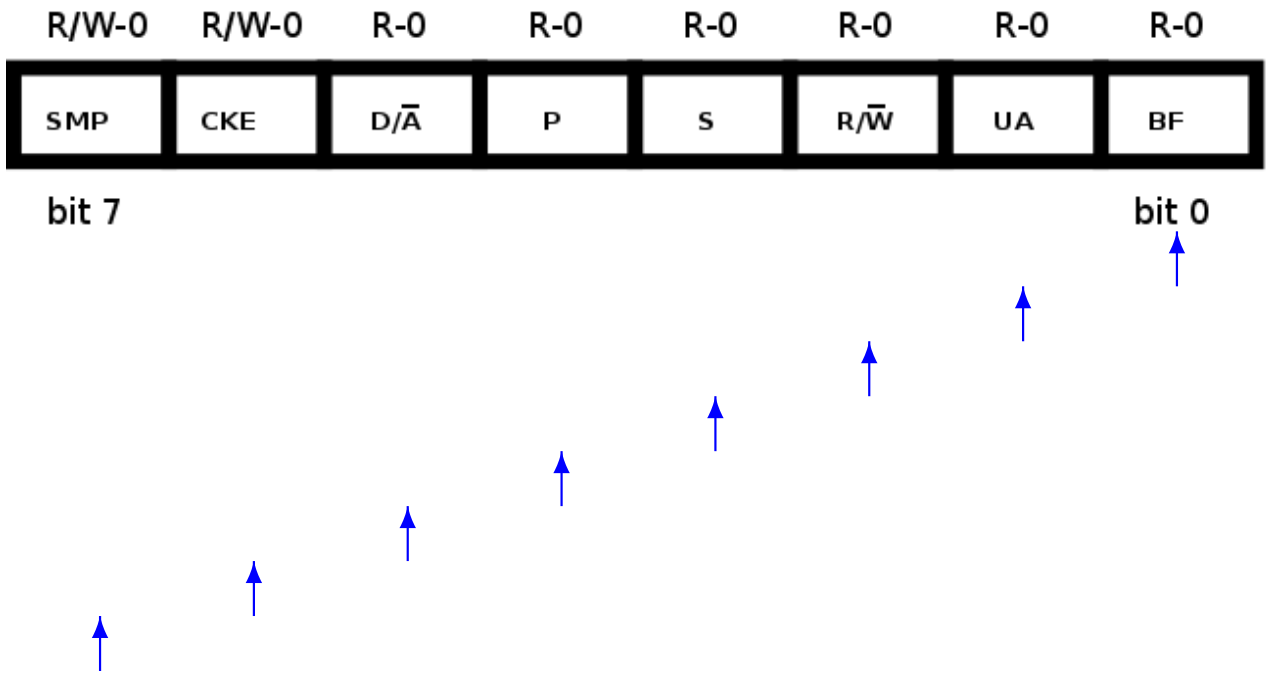
packets are single characters

SSPSTAT

SSPSTAT



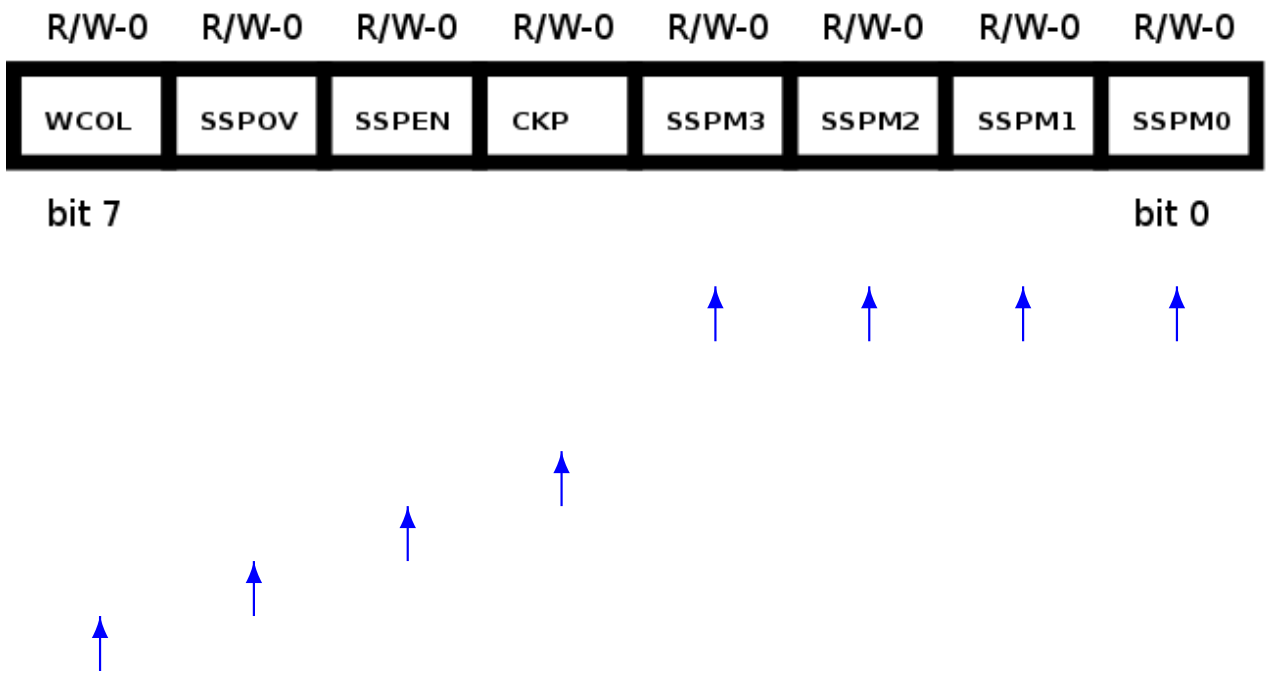
SSPSTAT



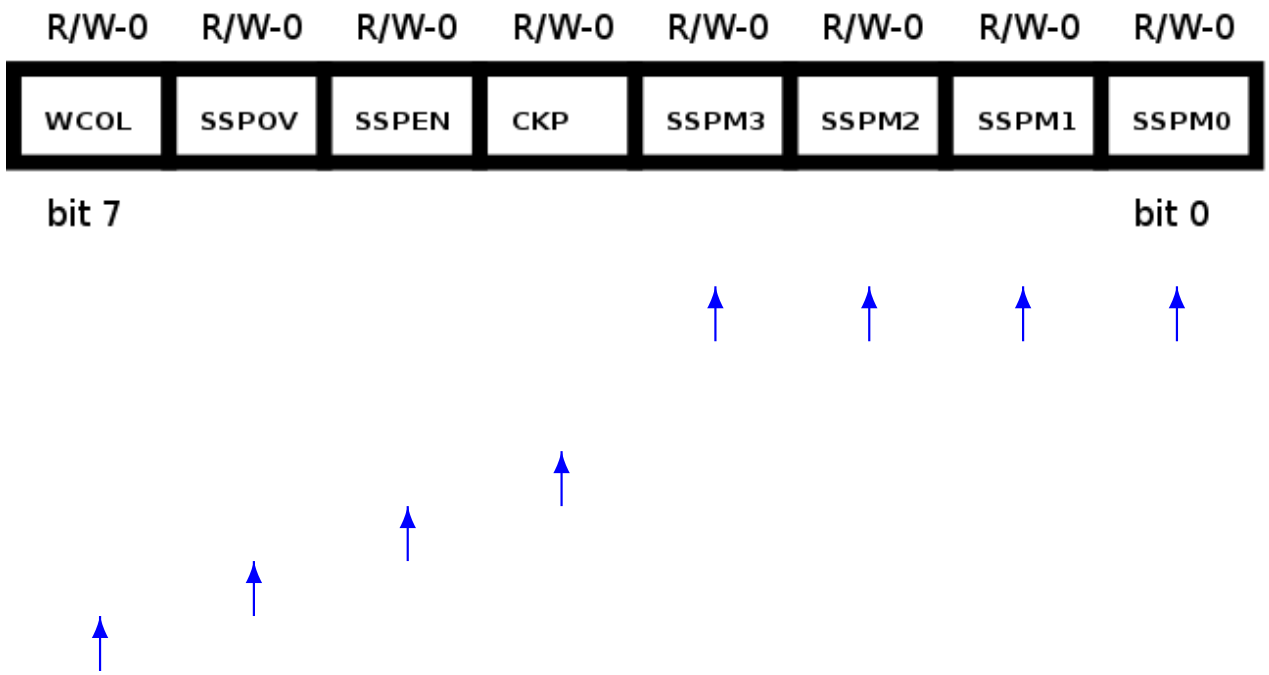
Bits in SSPSTAT register

SSPCON1

SSPCON1


R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
WCOL
SSPOV
SSPEN
CKP
SSPM3
SSPM2
SSPM1
SSPM0
bit 7
bit 0

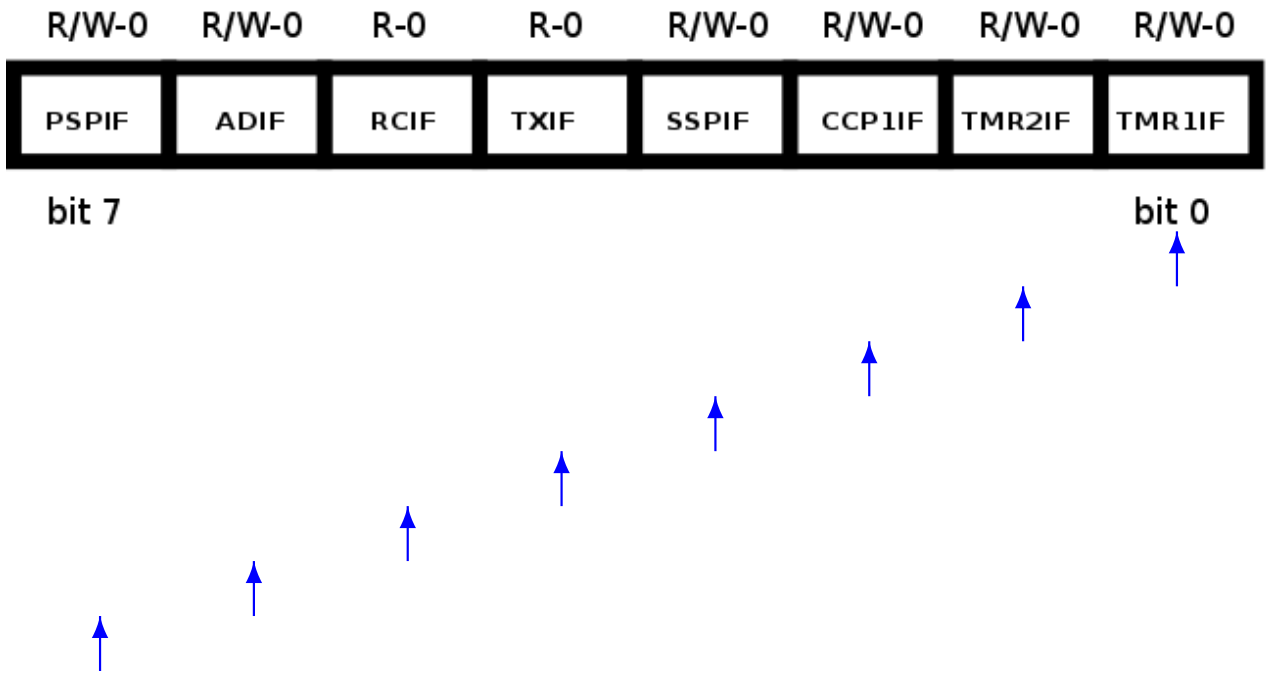
SSPCON1



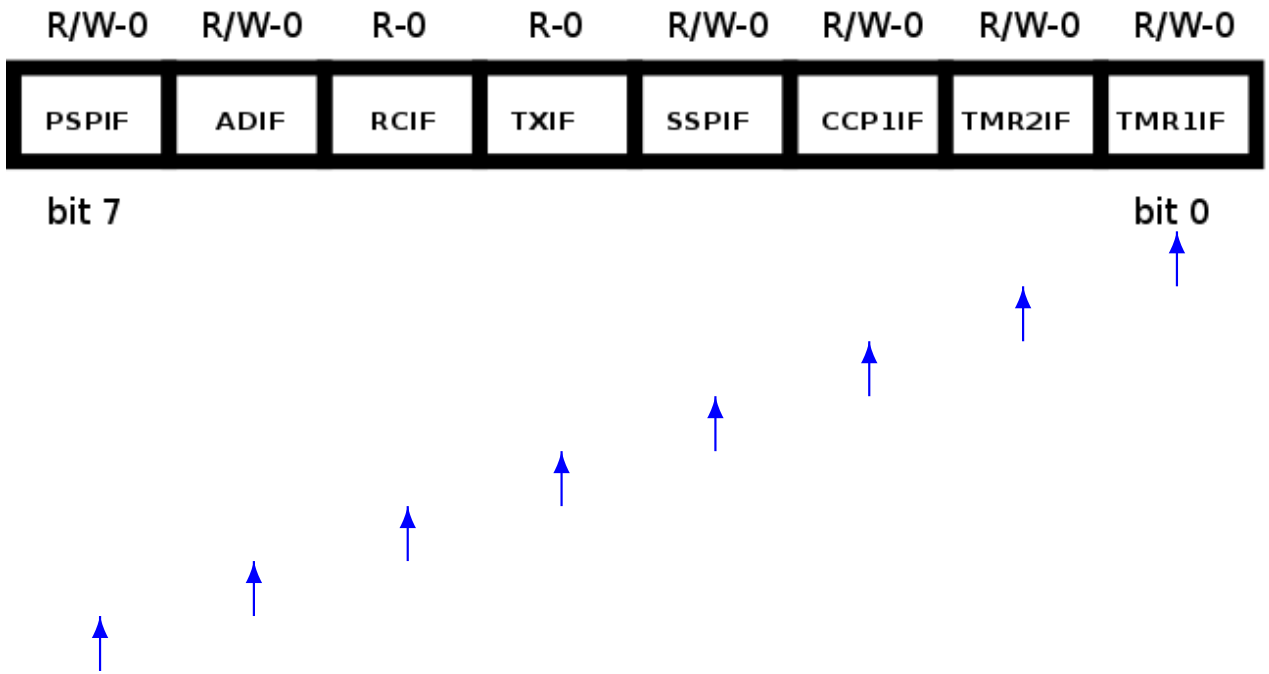
Bits in SSPCON1 register

PIR1

PIR1

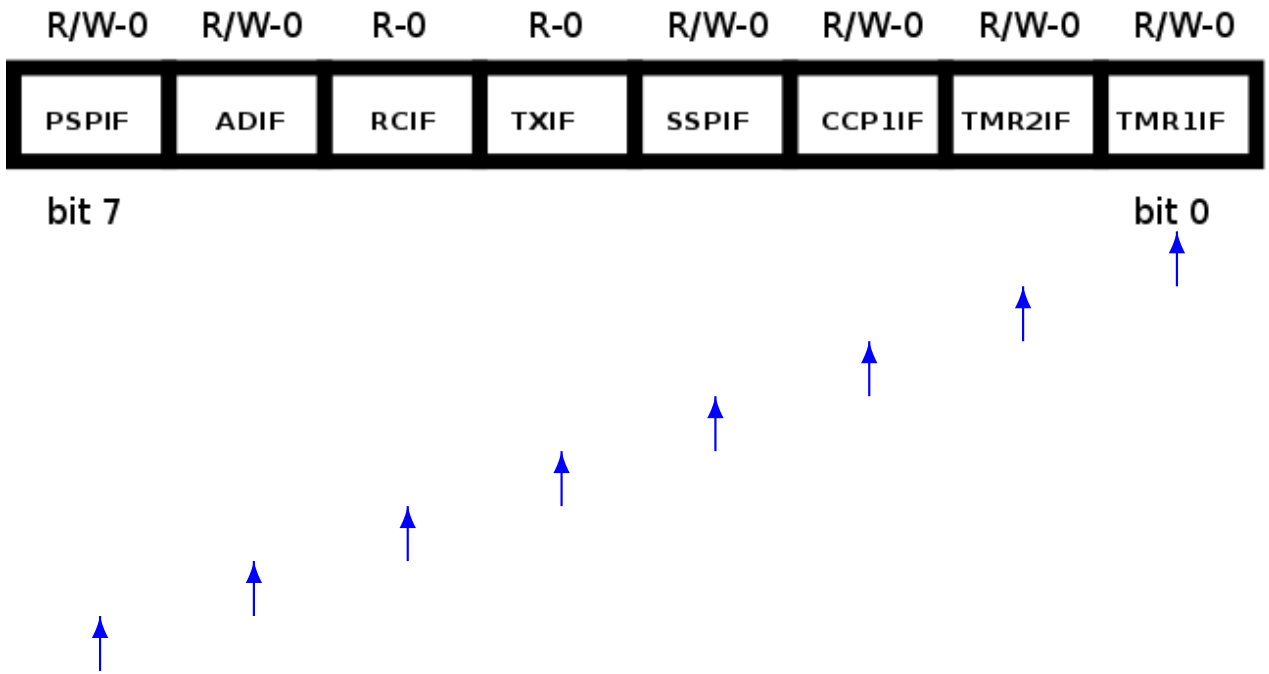

R/W-0
R/W-0
R-0
R-0
R/W-0
R/W-0
R/W-0
R/W-0
PSPIF
ADIF
RCIF
TXIF
SSPIF
CCP1IF
TMR2IF
TMR1IF
bit 7
bit 0

PIR1



Bits in PIR1 register

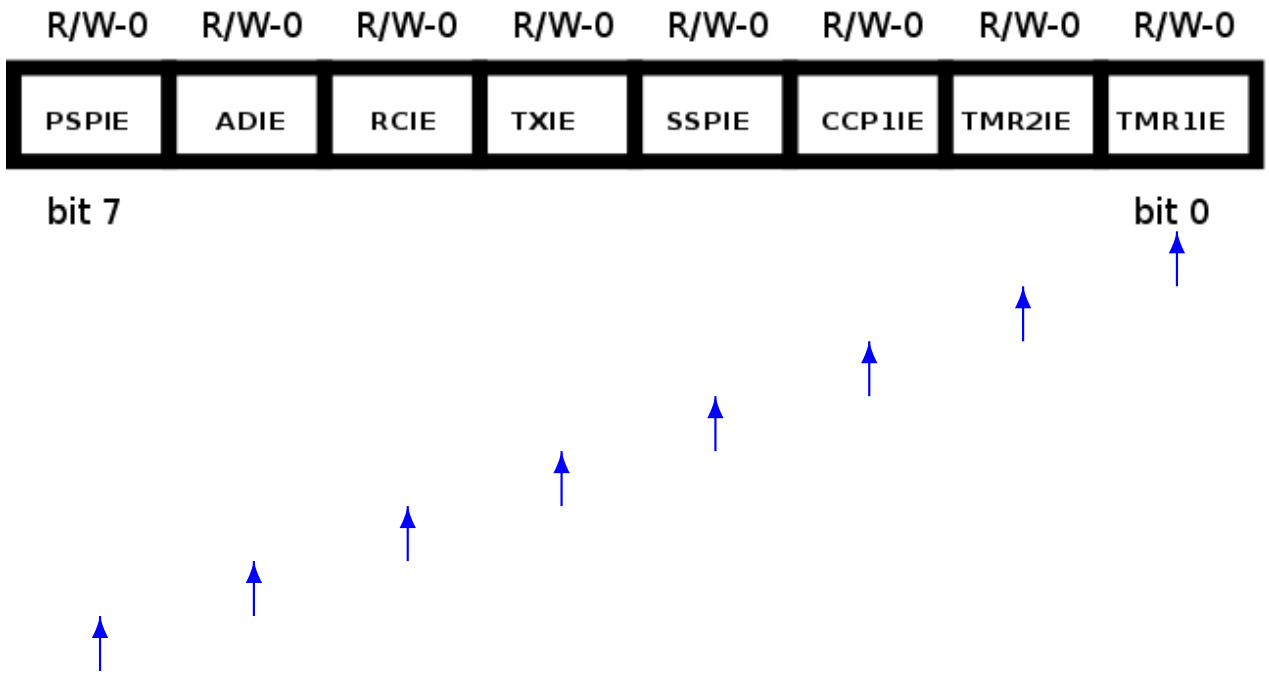
PIR1



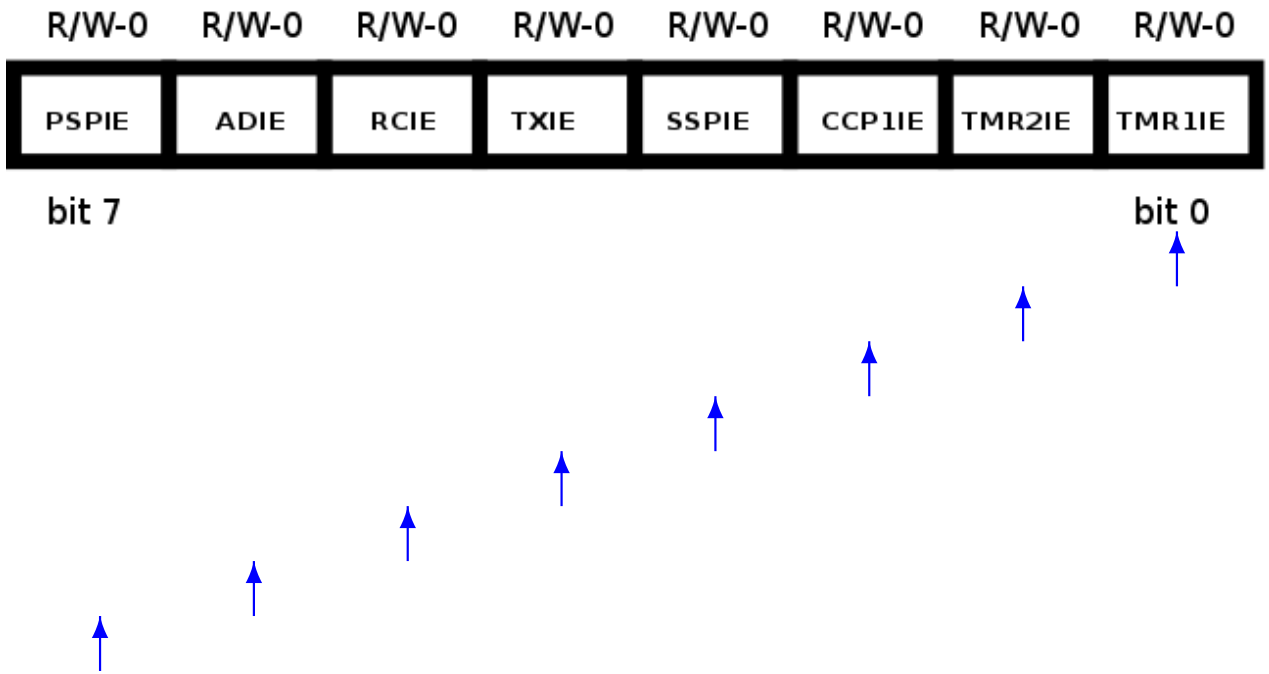
Bits in PIR1 register - Note SSPIF

PIE1

PIE1

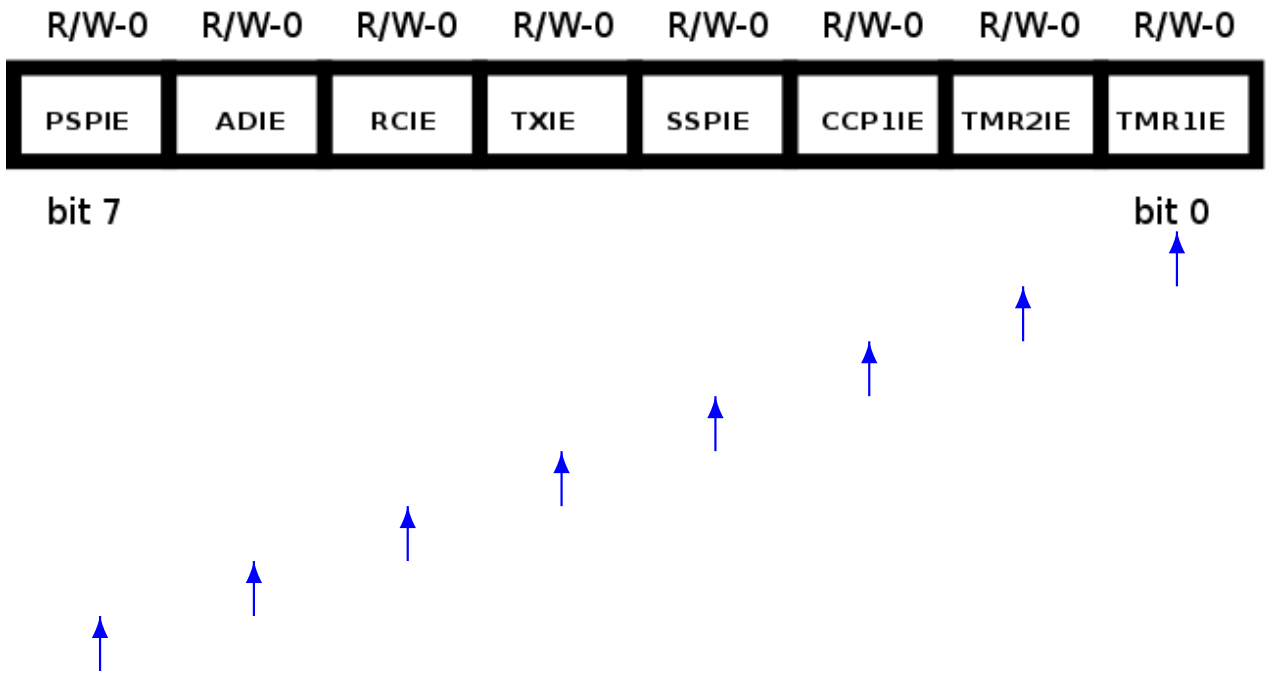

R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
PSPIE
ADIE
RCIE
TXIE
SSPIE
CCP1IE
TMR2IE
TMR1IE
bit 7
bit 0

PIE1



Bits in PIE1 register

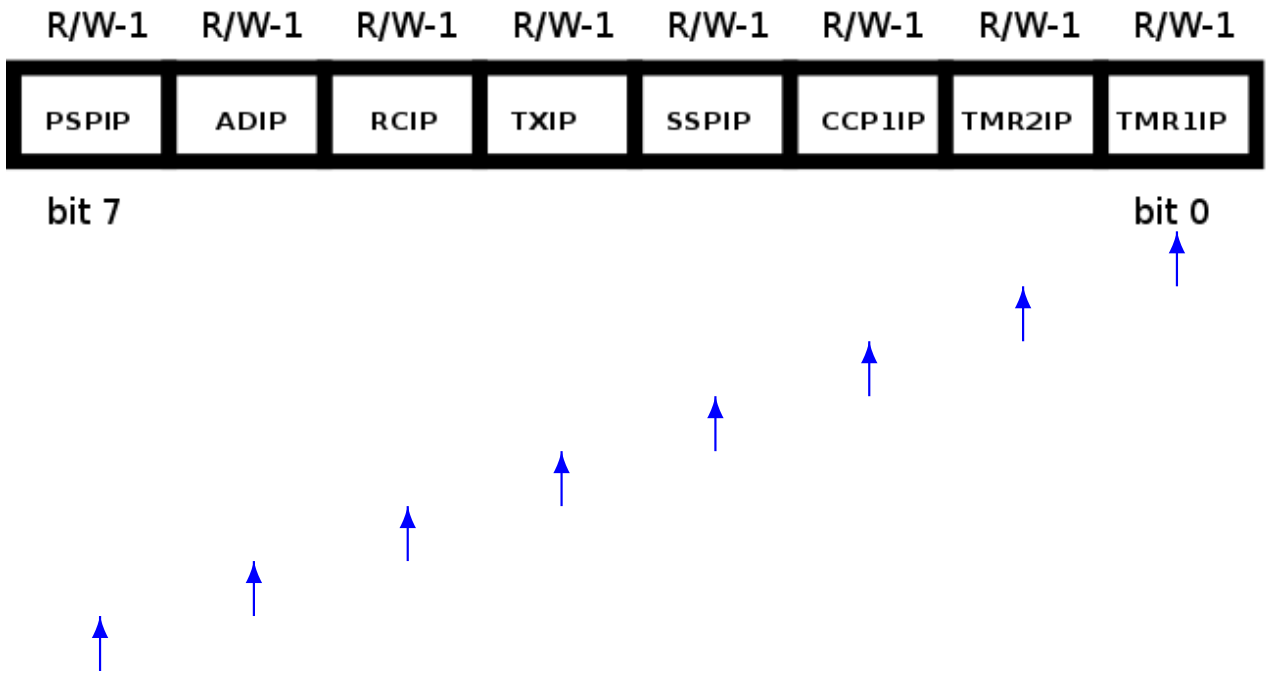
PIE1



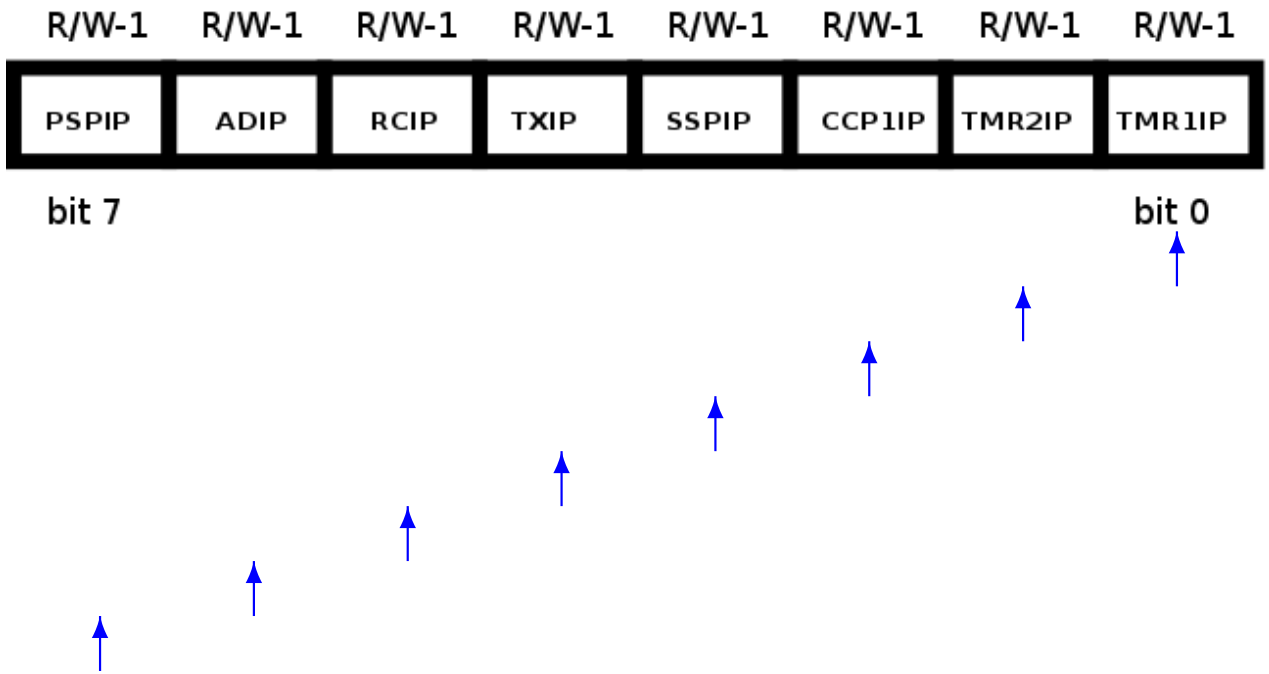
Bits in PIE1 register - Note SSPIE

IPR1

IPR1

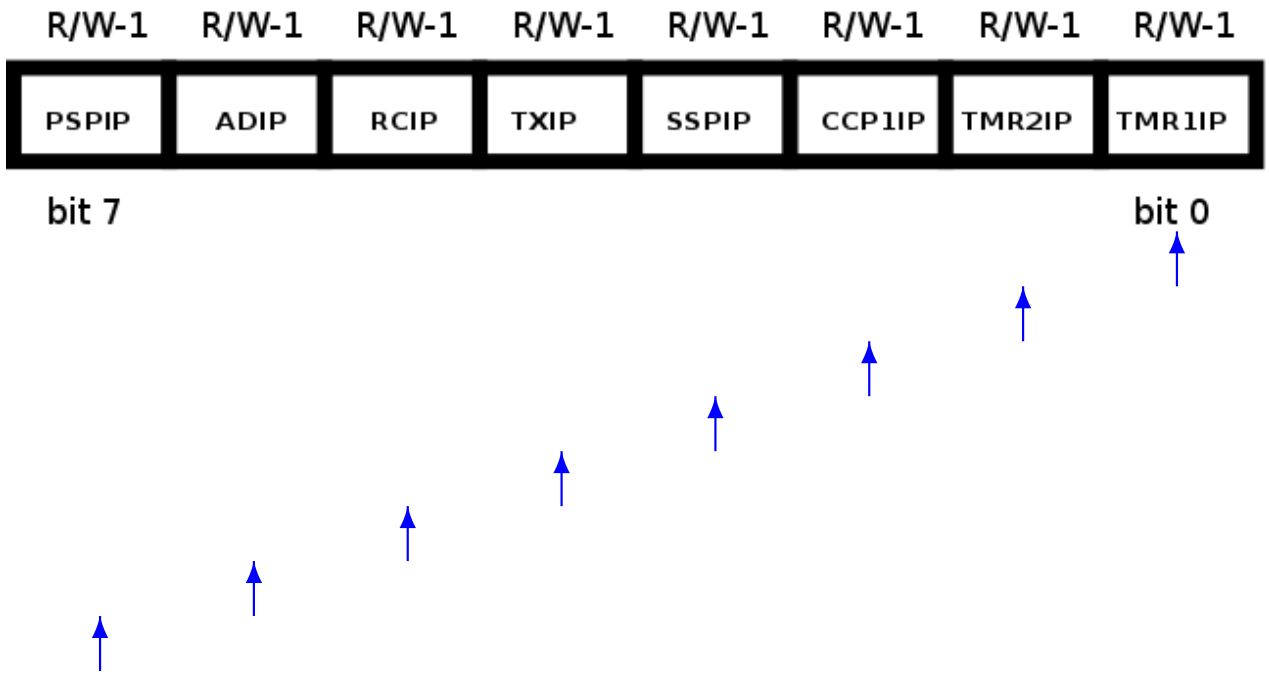

R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
PSPIP
ADIP
RCIP
TXIP
SSPIP
CCP1IP
TMR2IP
TMR1IP
bit 7
bit 0

IPR1



Bits in IPR1 register

IPR1



Bits in IPR1 register - Note SSPIP

Bit-bashing

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overview

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overview

reasons

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NIB

Code

Code

PORT configuration

Code

PORT configuration

$\rightarrow$ macro or subroutine?

Code

PORT configuration

$\rightarrow$ macro or subroutine?

Initialization

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Write to device

Code

PORT configuration

→ macro or subroutine?

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→ macro or subroutine?

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PORT configuration

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Read from device

Code

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4. enable interrupt (if using) (**PIE1**)
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   (if not using interrupts)
6. de-assert $\overline{CS}$ (**LATC**)
7. when no more characters to send,
   disable transmit interrupt (if using) (**PIE1**)