CP316
Interrupts

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Introduction to Interrupts

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A high priority interrupt can happen *during* a low priority interrupt, but not the other way around.

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  state of flag indicating pending or not

Interrupts

Interrupts

overview

Interrupts

overview

→ Section 6.2.5

Interrupts

overview

→ Section 6.2.5

→ Section 8.0

Interrupts

overview

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vectors

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status; clear, pending

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bits; enable, priority, flag

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→ Sections 6.4.2

Here's a code fragment from a typical program:

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```
;;;  vectors
   org    0x0000     ;reset vector
   goto   start      ;beginning of program

   org    0x0008     ;high priority int. vector
   goto   high_ISR   ;program memory label
;   goto $           ;none for now

   org    0x0018     ;low priority int. vector
   goto   $          ;none for now
;   goto low_ISR
```

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6. **retfie**

   like a subroutine return, but re-enables interrupts

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RETURN instruction

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RETURN	Return from Subroutine
Syntax:	[*label*] RETURN [s]
Operands:	s ∈ [0,1]
Operation:	(TOS) → PC, if s = 1 (WS) → W, (STATUSS) → STATUS, (BSRS) → BSR, PCLATU, PCLATH are unchanged

What does *s* indicate?

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Note the difference from a normal *RETURN*

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Why should you only use *retfie FAST* for *high* priority interrupts?

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s indicates the *FAST* option

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Why does it set *GIE/GIEH* **or** *PEIE/GIEL*?

RETLW instruction

RETLW instruction

RETLW	Return Literal to W
Syntax:	[*label*] RETLW k
Operands:	$0 \le k \le 255$
Operation:	$k \rightarrow W$, (TOS) $\rightarrow$ PC, PCLATU, PCLATH are unchanged

Why is *FAST* not an option?

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- Use interrupts for events of very short duration

  i.e. if polling may miss them entirely

Interrupt Sources

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internal, external

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→ Chapter 8 (Figure 8-1)

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portB, timers, serial, ADC, etc.

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PIC interrupts

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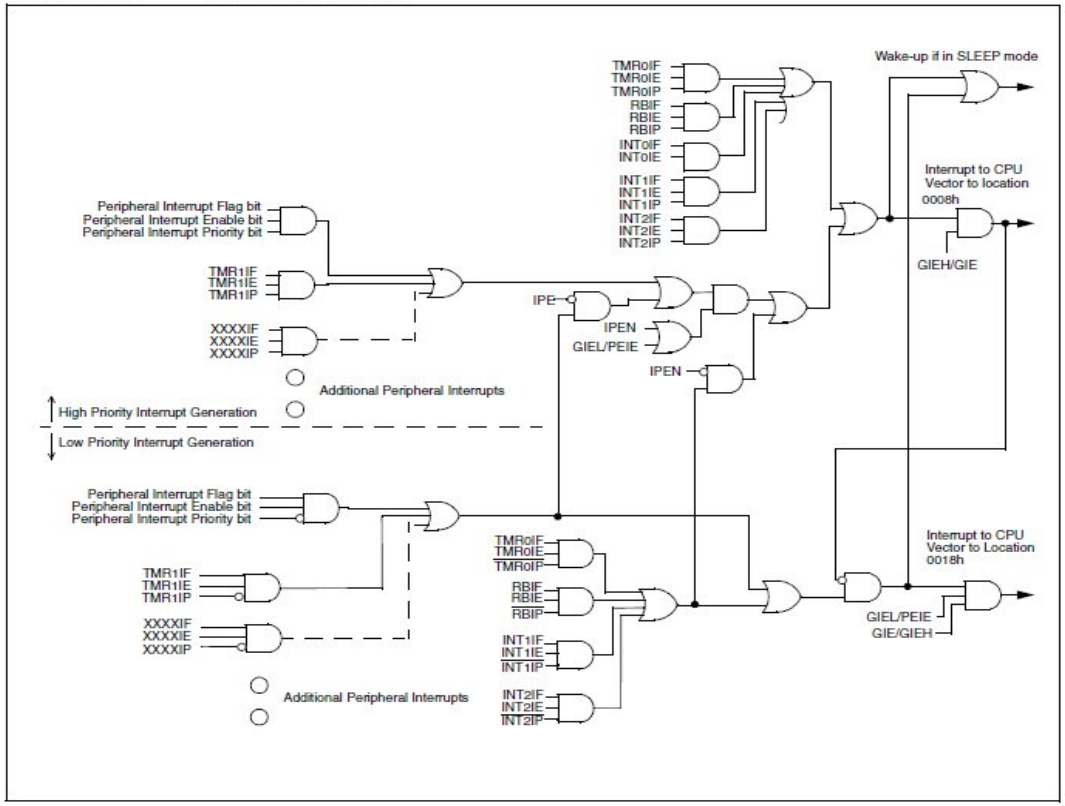
FIGURE 8-1: INTERRUPT LOGIC



Qwikflash interrupt connections

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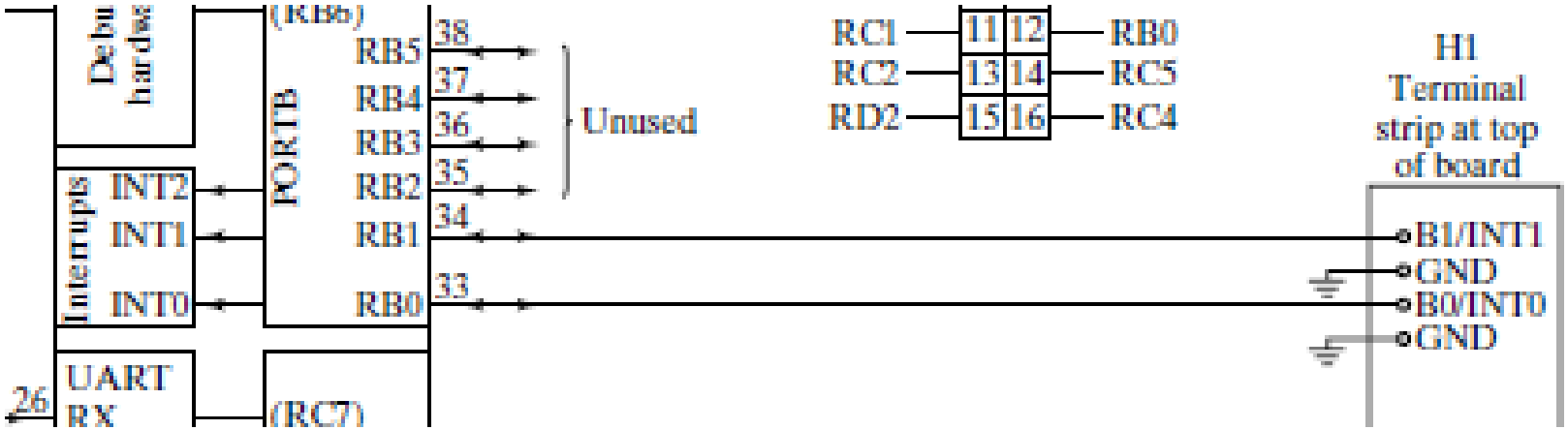

Interrupt Registers

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RCON

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RCON

→ Section 6.4.3

Interrupt Registers

RCON

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INTCON, **INTCON2**, **INTCON3**

Interrupt Registers

RCON

→ Section 6.4.3

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Interrupt Registers

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PIR1, **PIR2**

Interrupt Registers

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→ Section 6.4.3

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Interrupt Registers

RCON

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Interrupt Registers

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IPR1, **IPR2**

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→ Section 6.4.5

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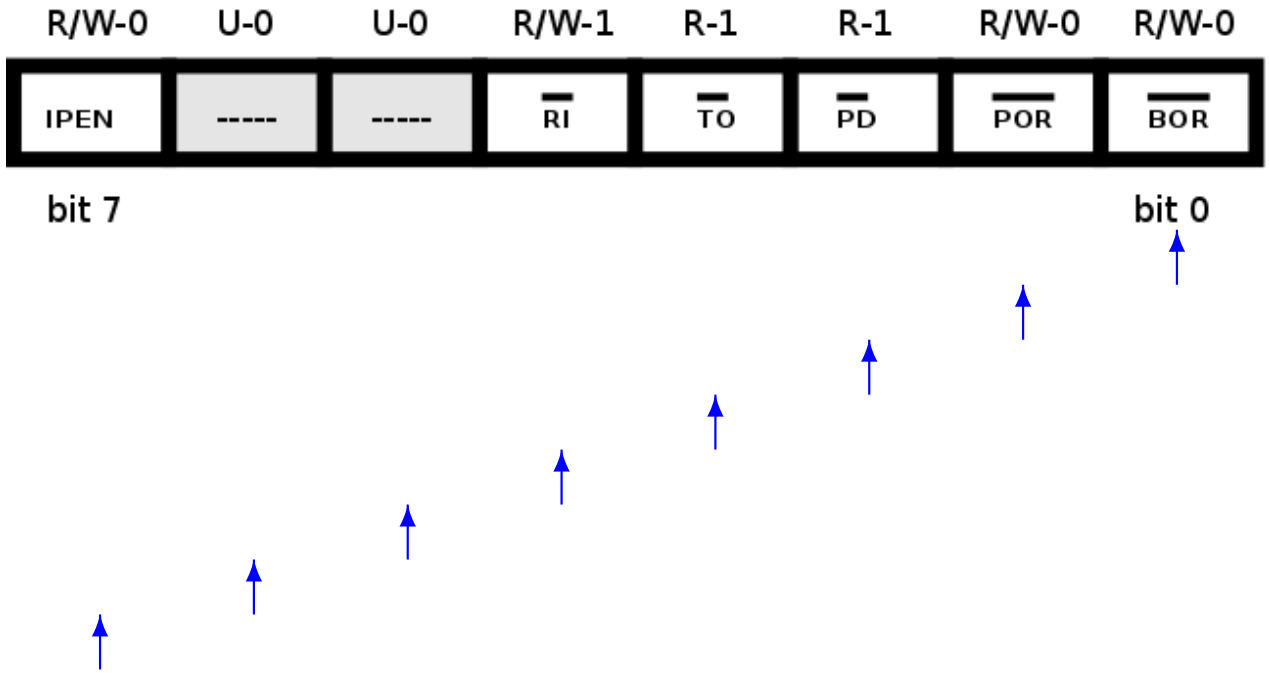
→ Section 6.4.6

IPR1, **IPR2**

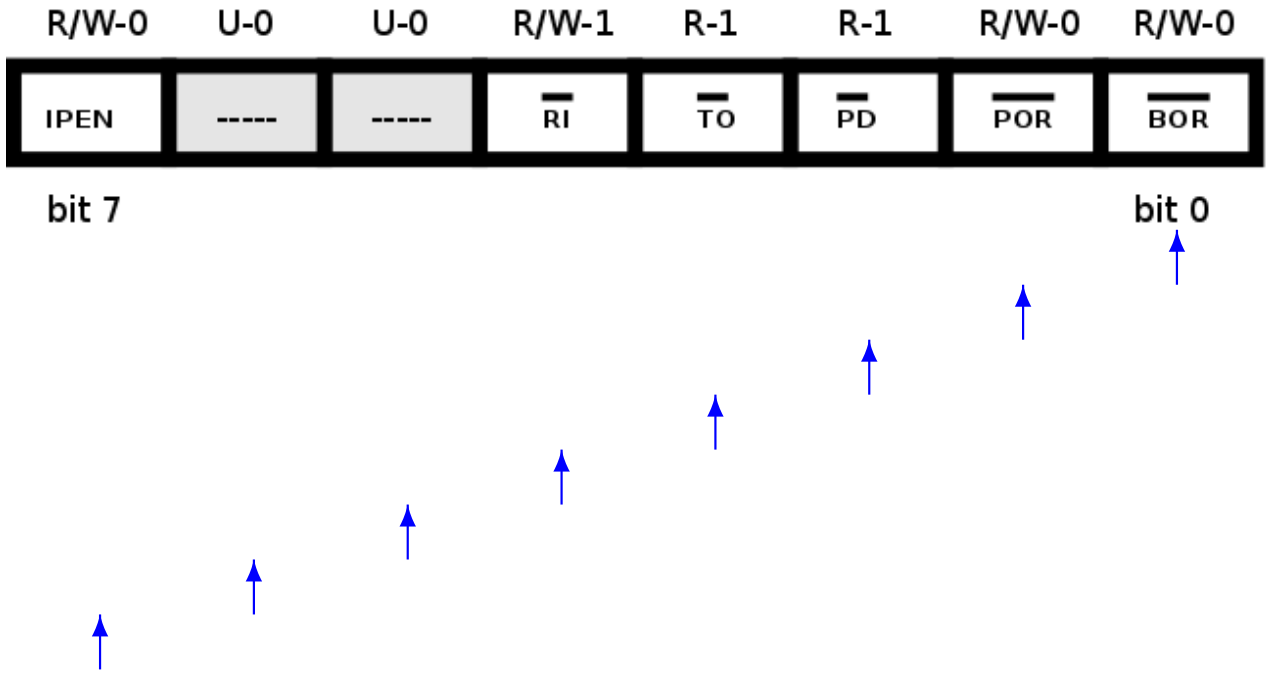
→ Section 6.4.7

RCON

RCON

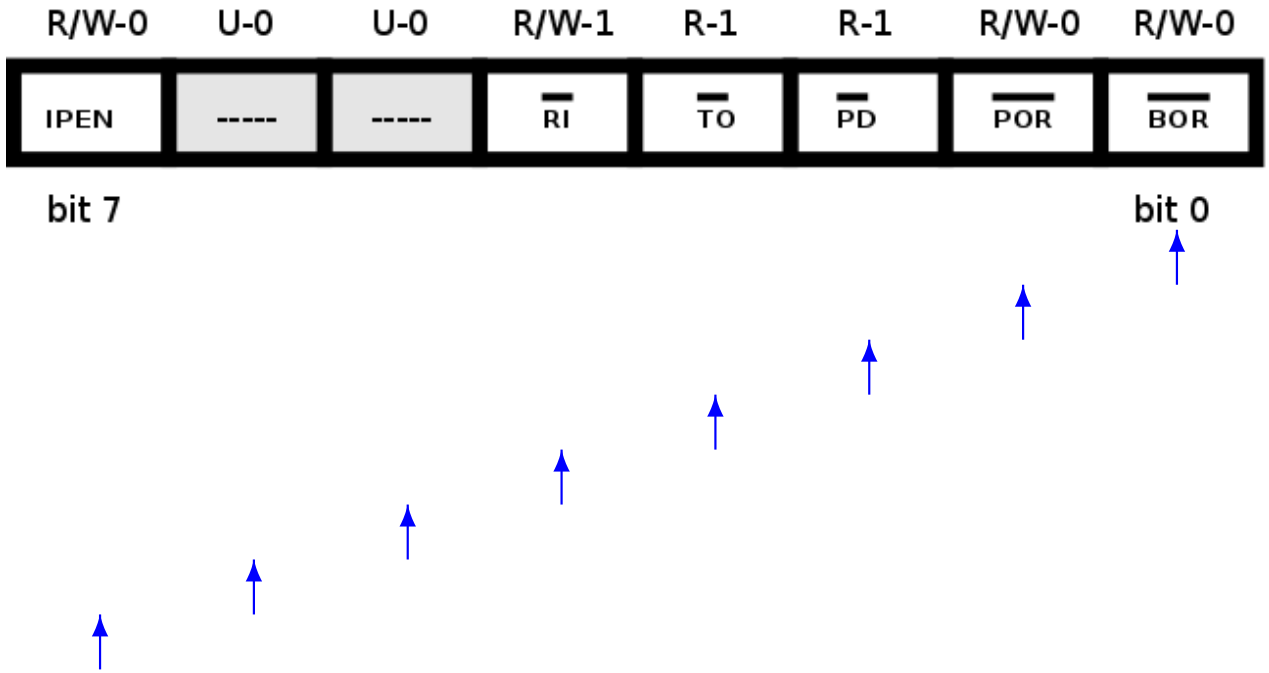


RCON



Bits in RCON register

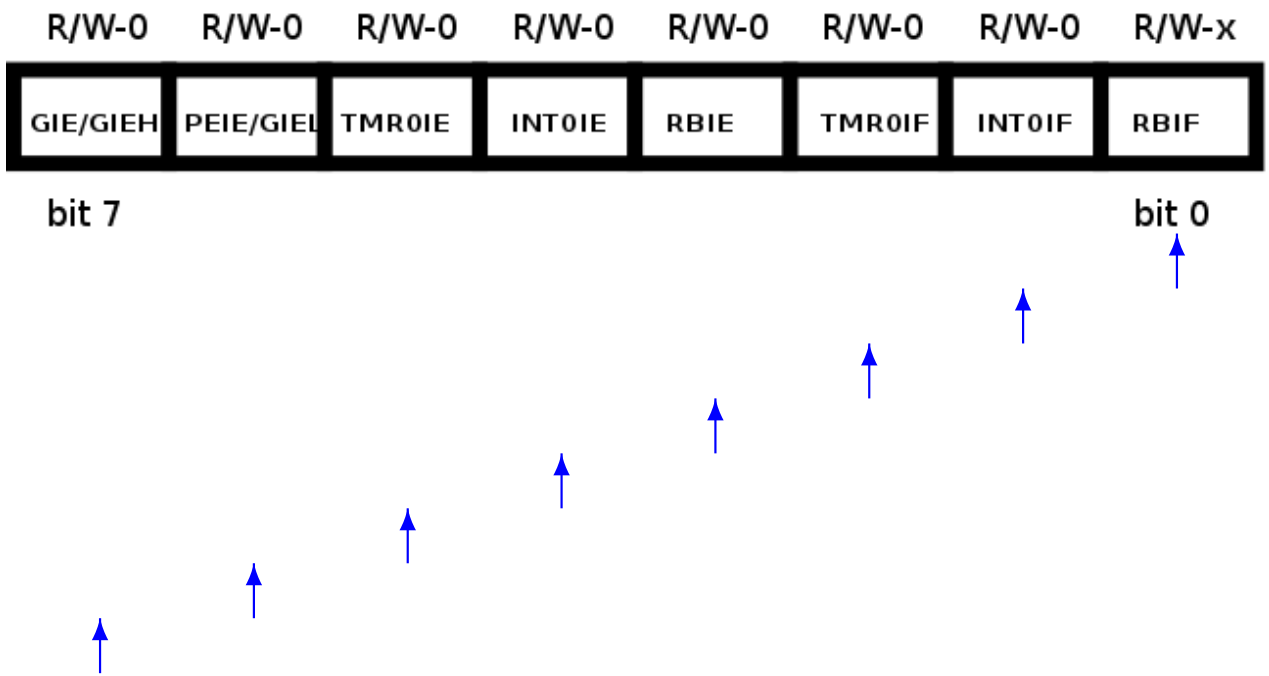
RCON



Bits in RCON register -Set IPEN for priority

INTCON

INTCON


R/W-0
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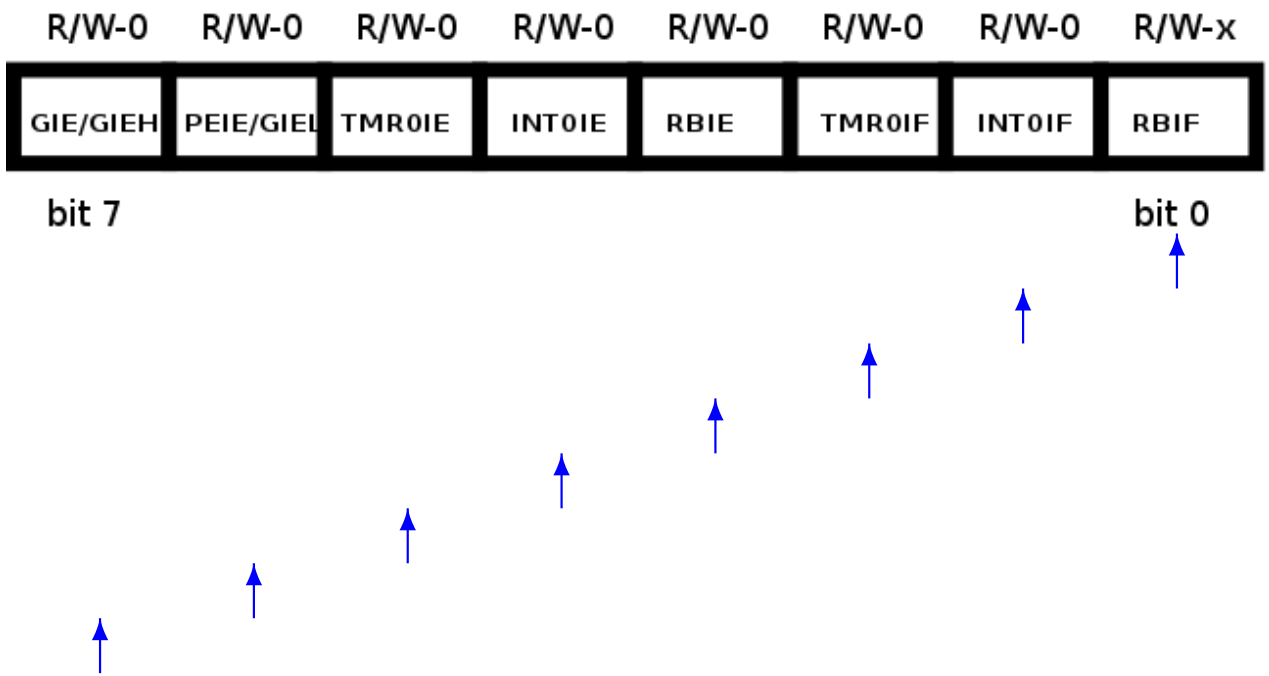
R/W-0
R/W-x
GIE/GIEH
PEIE/GIEL
TMR0IE
INT0IE
RBIE
TMR0IF
INT0IF
RBIF
bit 7
bit 0

INTCON



Bits in INTCON register

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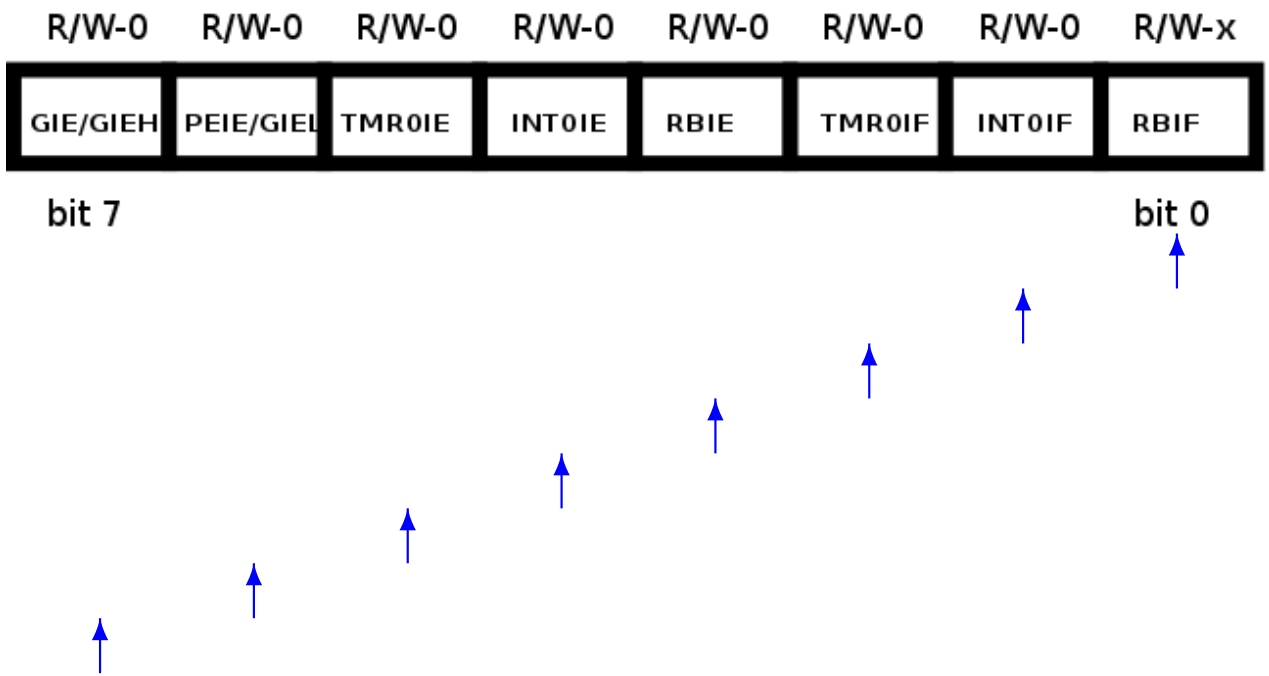
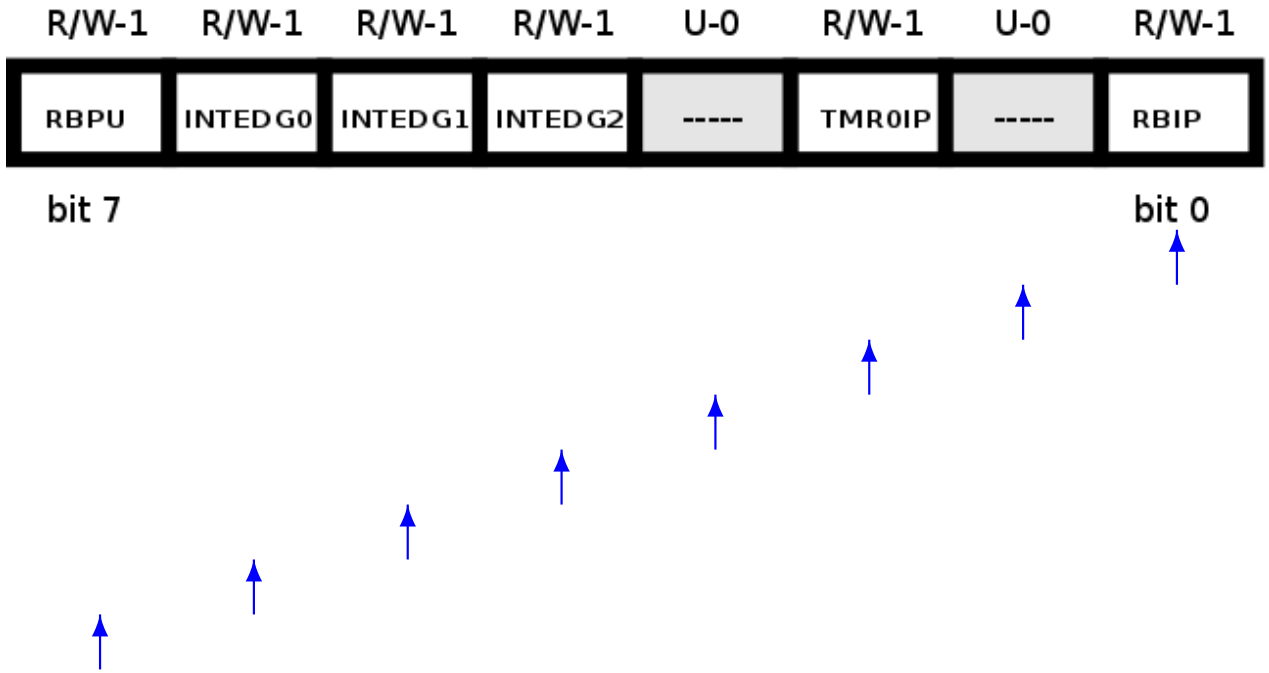


Bits in INTCON register -Set GIEH to enable high priority, GIEL to enable low priority (if GIEH set)

INTCON2

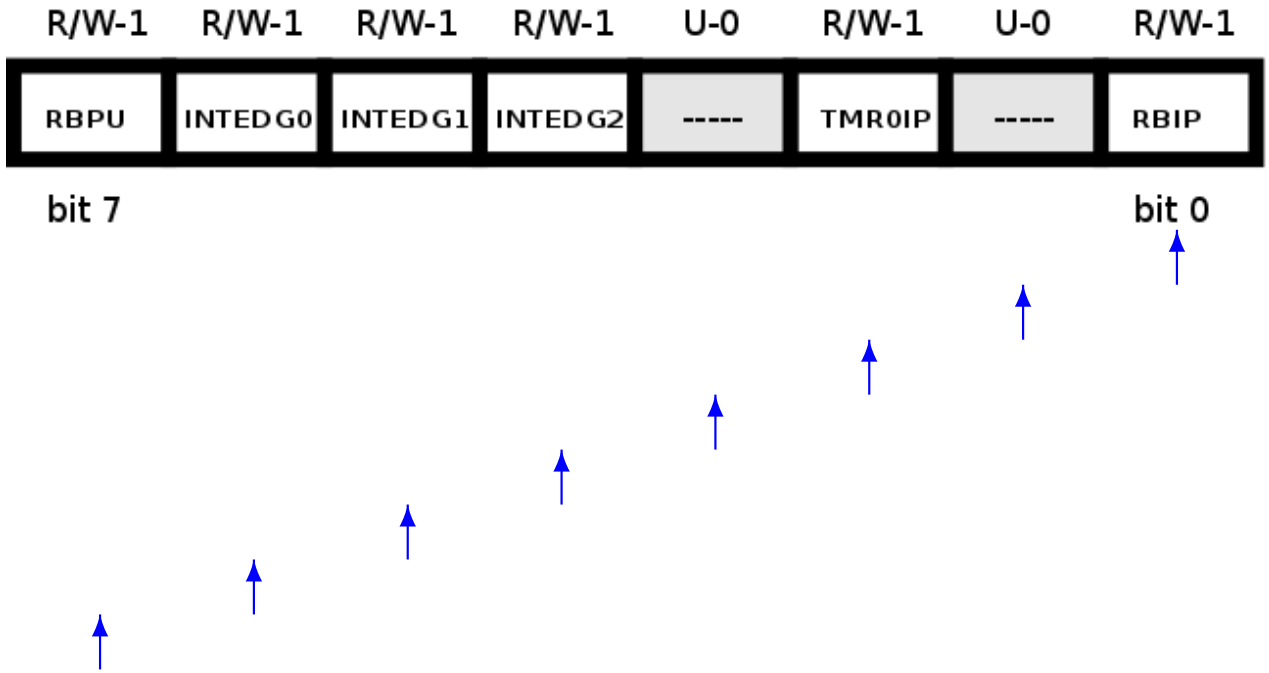
INTCON2


R/W-1
R/W-1
R/W-1
R/W-1
U-0
R/W-1
U-0
R/W-1
RBPU
INTEDG0
INTEDG1
INTEDG2

TMR0IP

RBIP
bit 7
bit 0

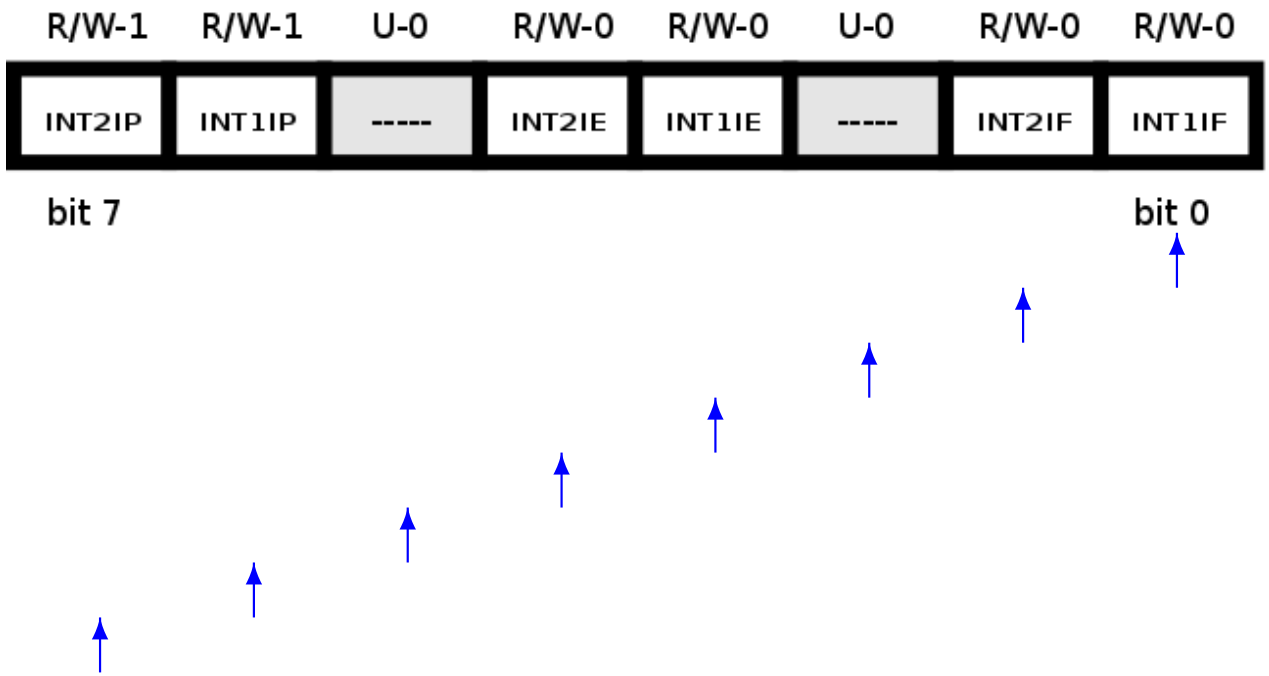
INTCON2



Bits in INTCON2 register

INTCON3

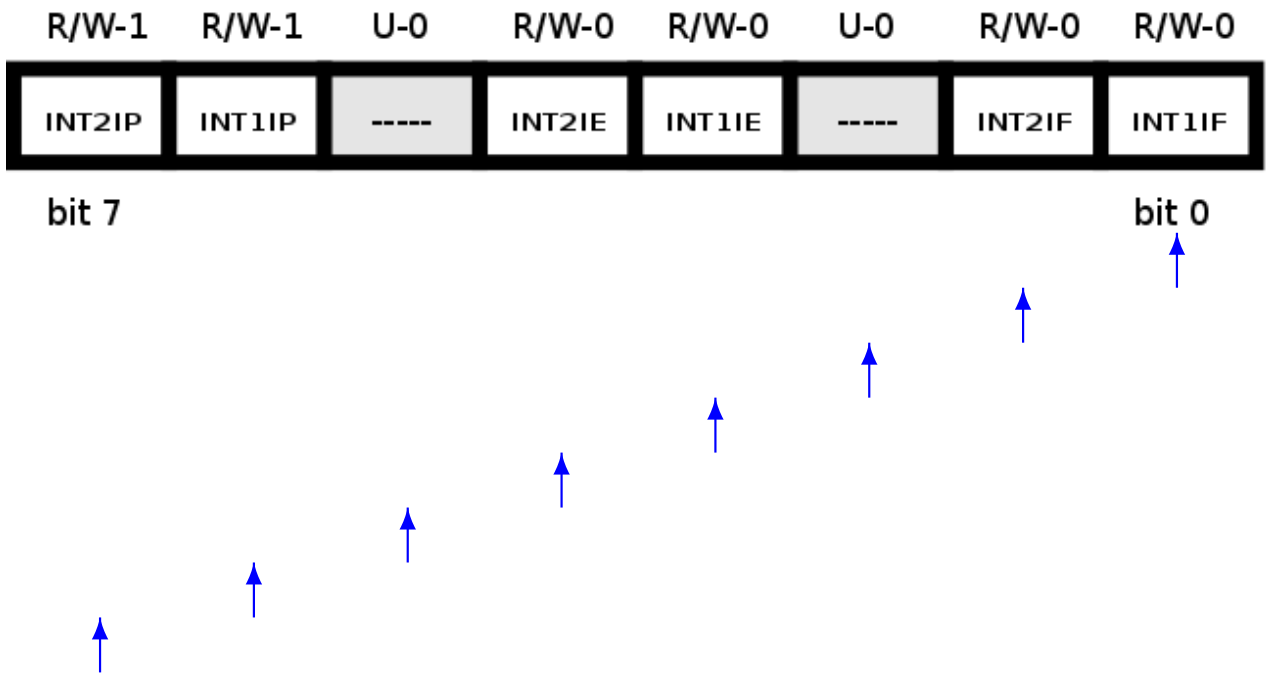
INTCON3


R/W-1
R/W-1
U-0
R/W-0
R/W-0
U-0
R/W-0
R/W-0
INT2IP
INT1IP

INT2IE
INT1IE

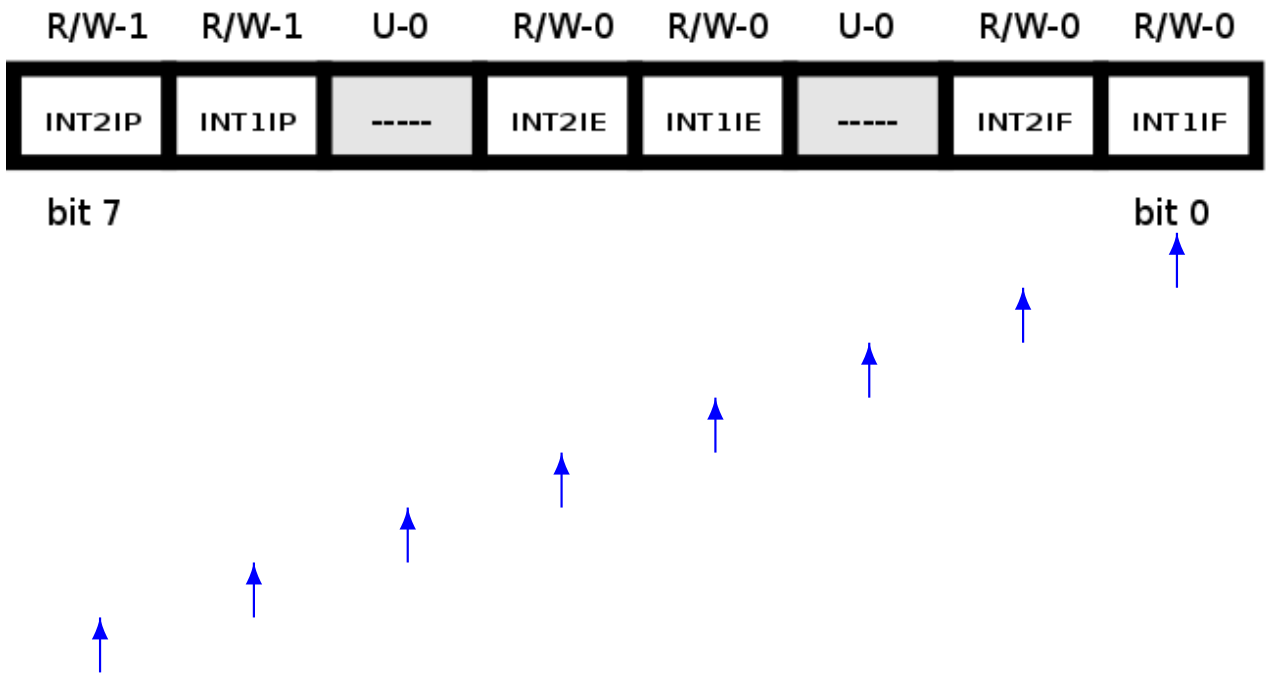
INT2IF
INT1IF
bit 7
bit 0

INTCON3



Bits in INTCON3 register

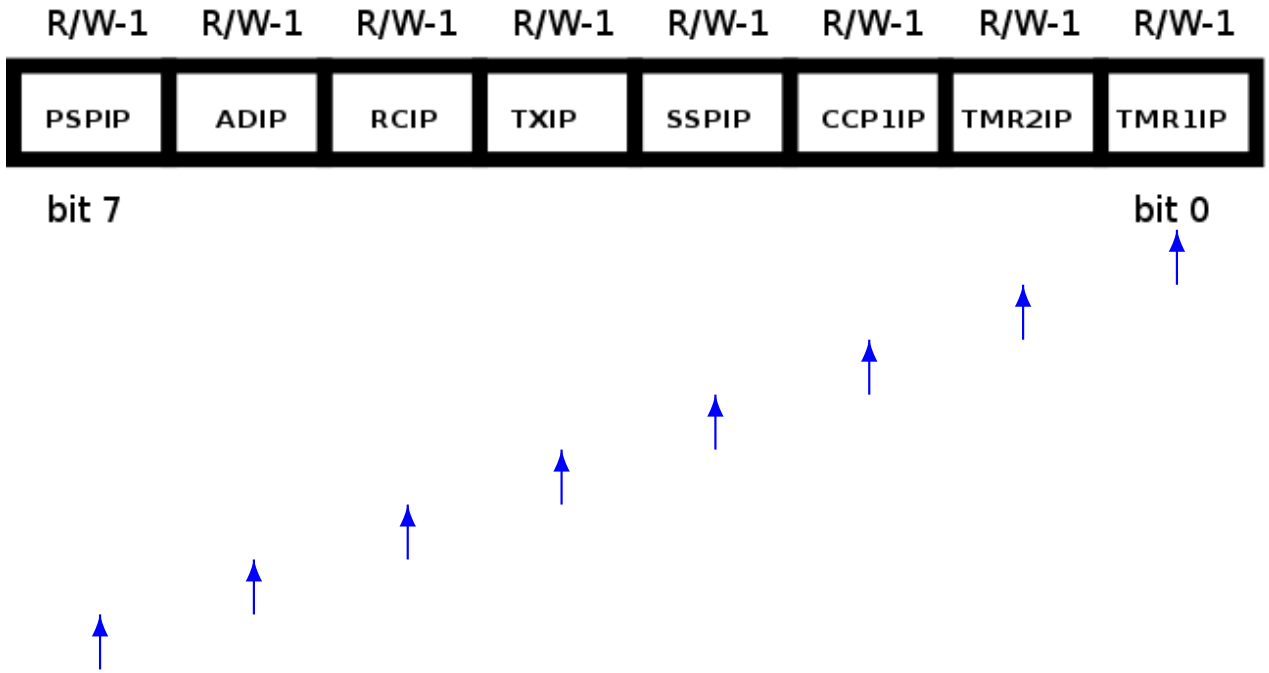
INTCON3



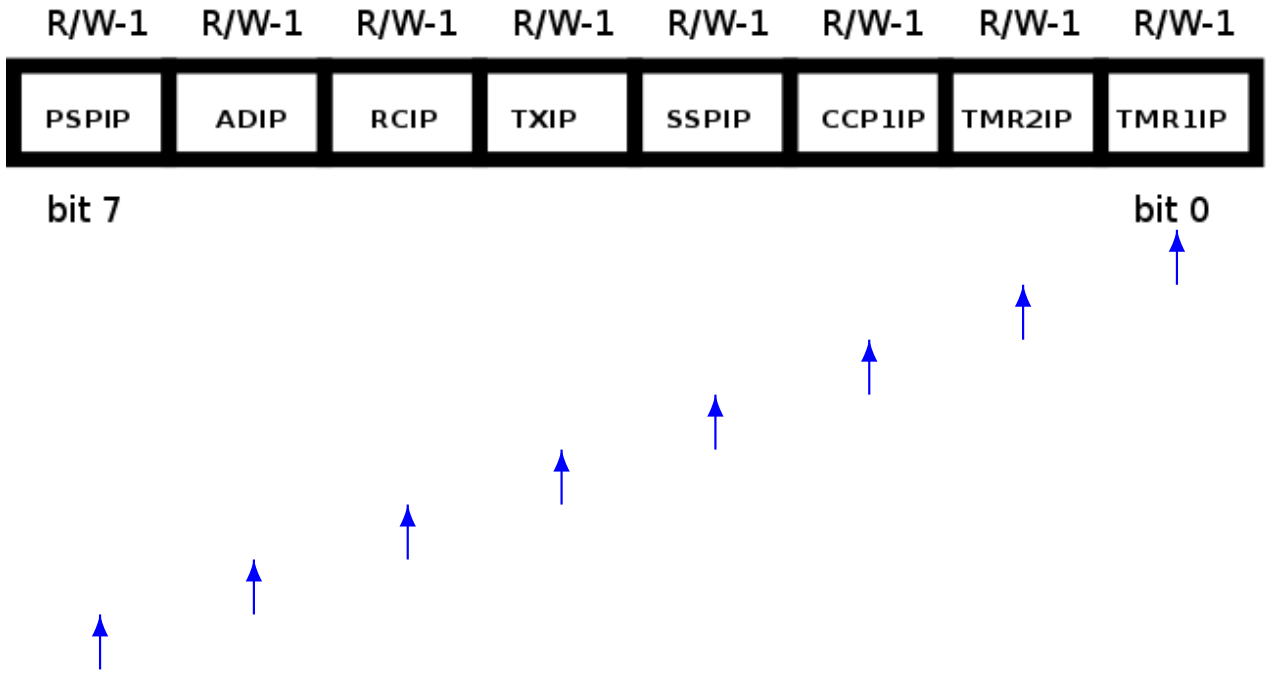
Bits in INTCON3 register -Note INT0 is not mentioned

IPR1

IPR1


R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
PSPIP
ADIP
RCIP
TXIP
SSPIP
CCP1IP
TMR2IP
TMR1IP
bit 7
bit 0

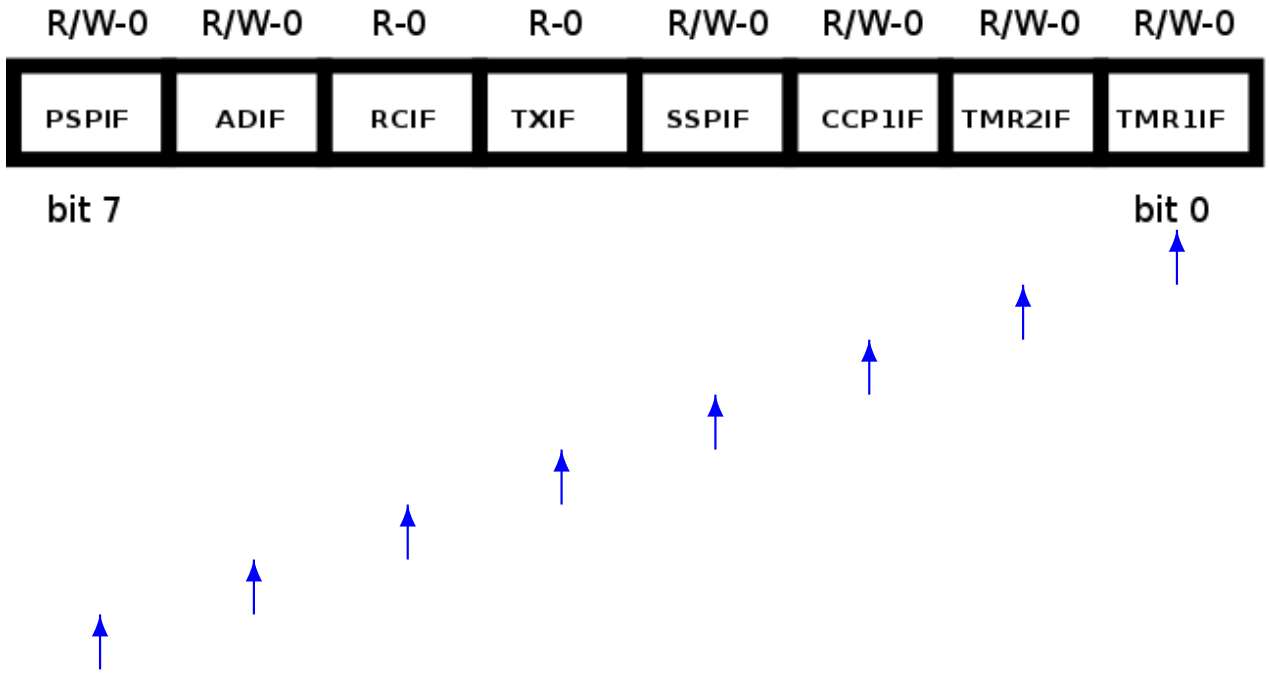
IPR1



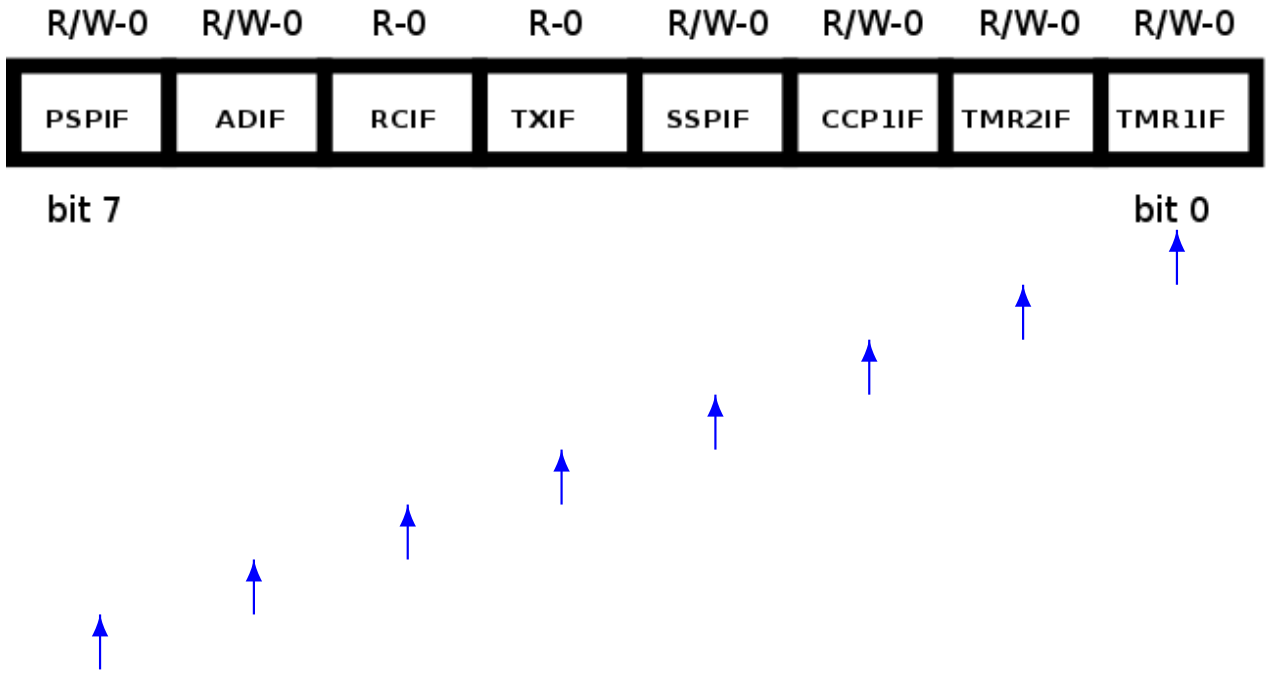
Bits in IPR1 register

PIR1

PIR1


R/W-0
R/W-0
R-0
R-0
R/W-0
R/W-0
R/W-0
R/W-0
PSPIF
ADIF
RCIF
TXIF
SSPIF
CCP1IF
TMR2IF
TMR1IF
bit 7
bit 0

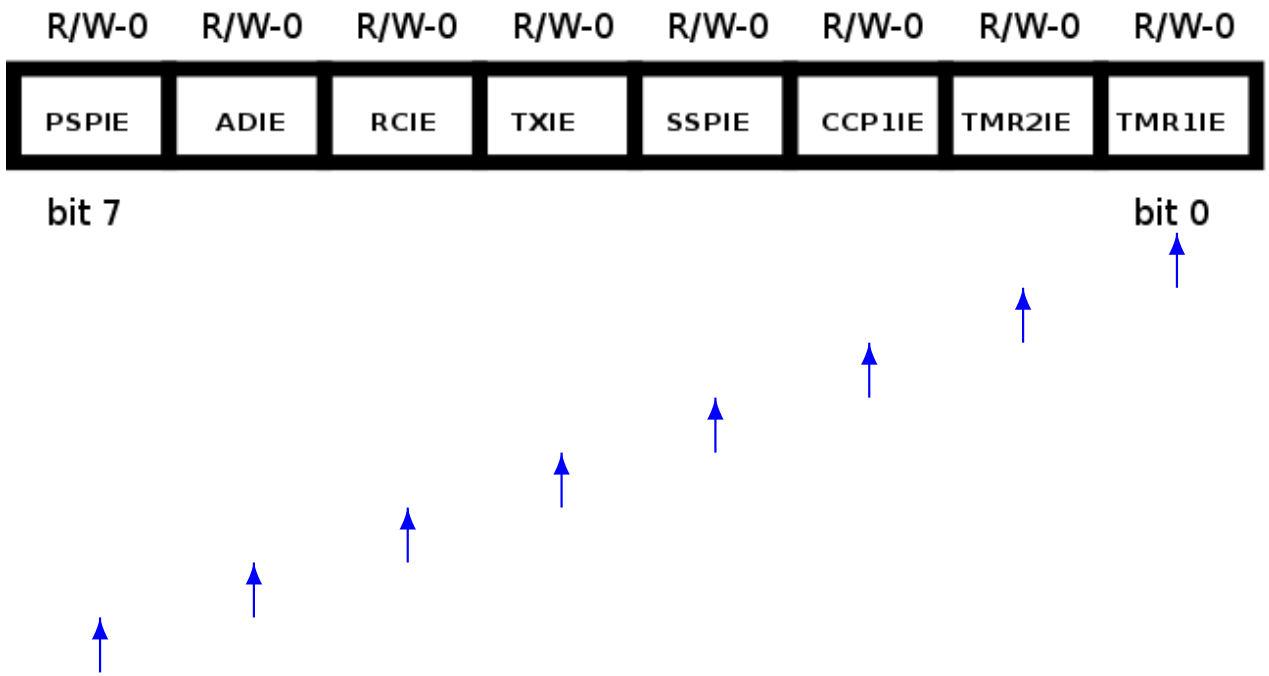
PIR1



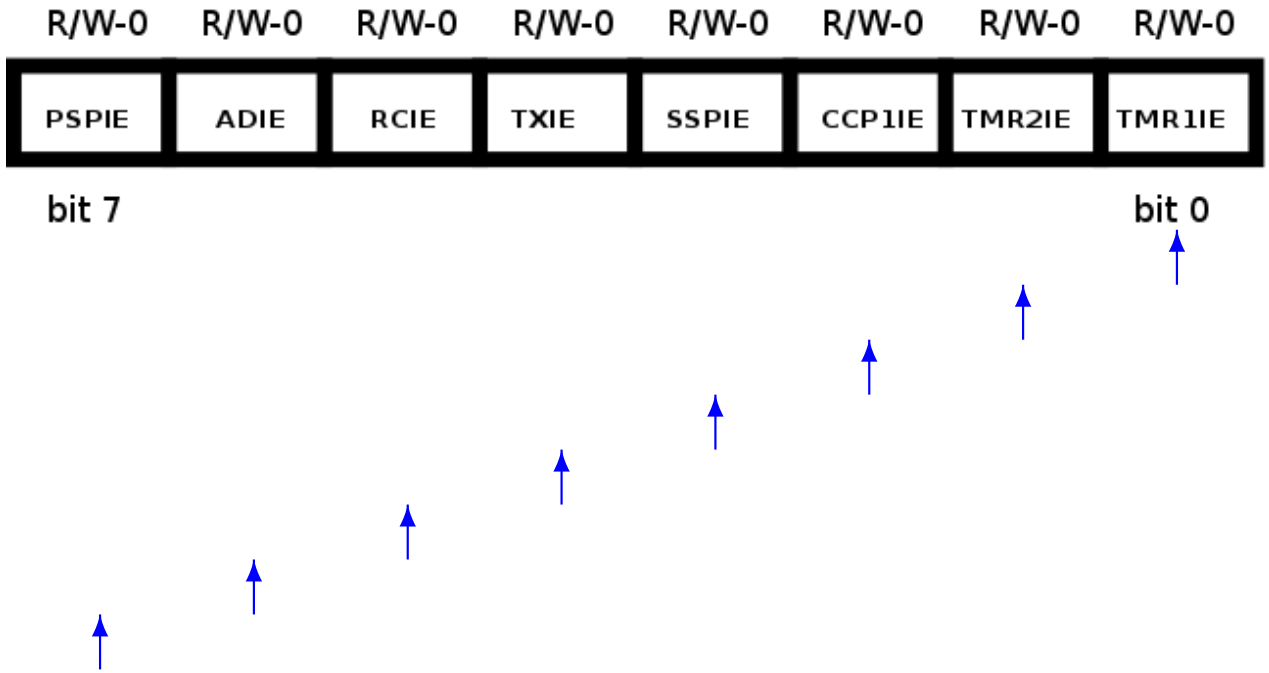
Bits in PIR1 register

PIE1

PIE1


R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
PSPIE
ADIE
RCIE
TXIE
SSPIE
CCP1IE
TMR2IE
TMR1IE
bit 7
bit 0

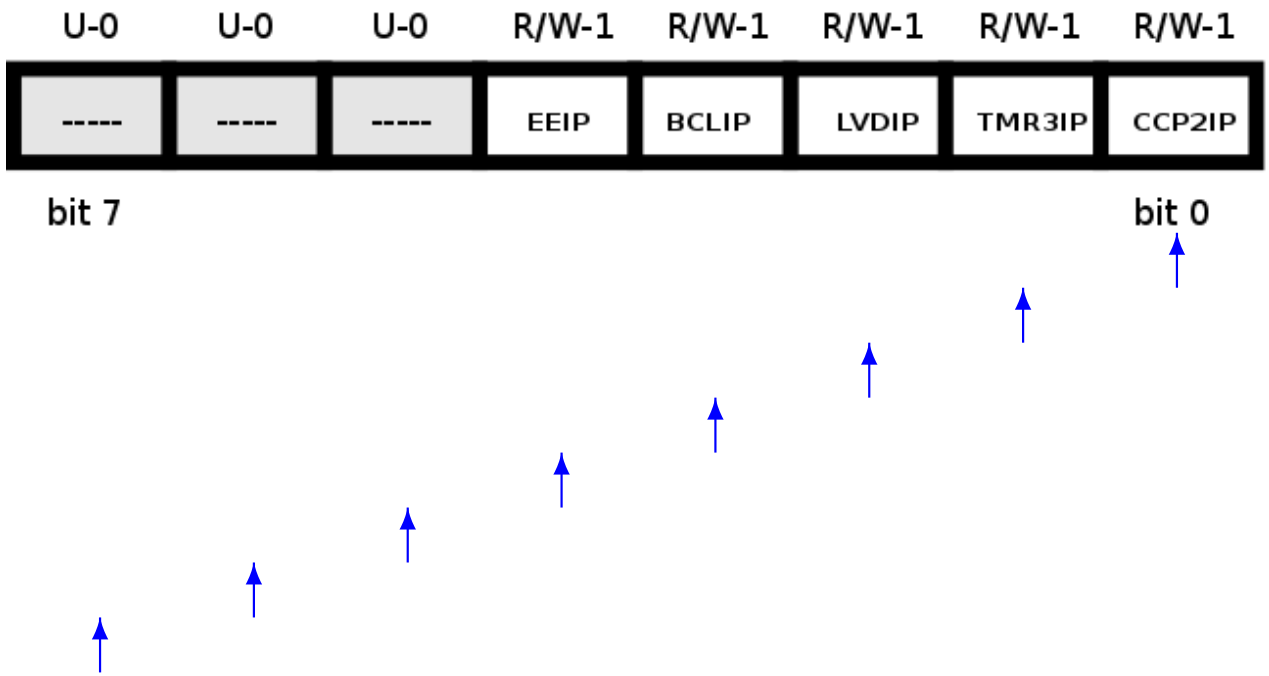
PIE1



Bits in PIE1 register

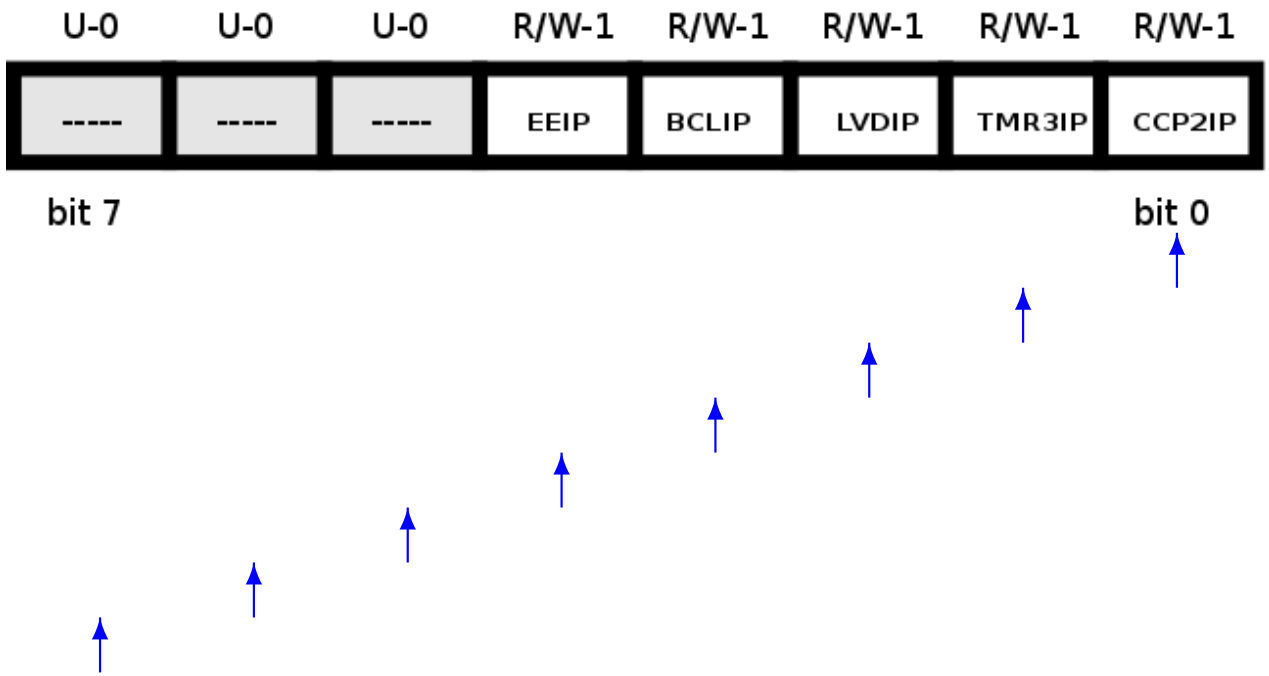
IPR2

IPR2


U-0
U-0
U-0
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1

EEIP
BCLIP
LVDIP
TMR3IP
CCP2IP
bit 7
bit 0

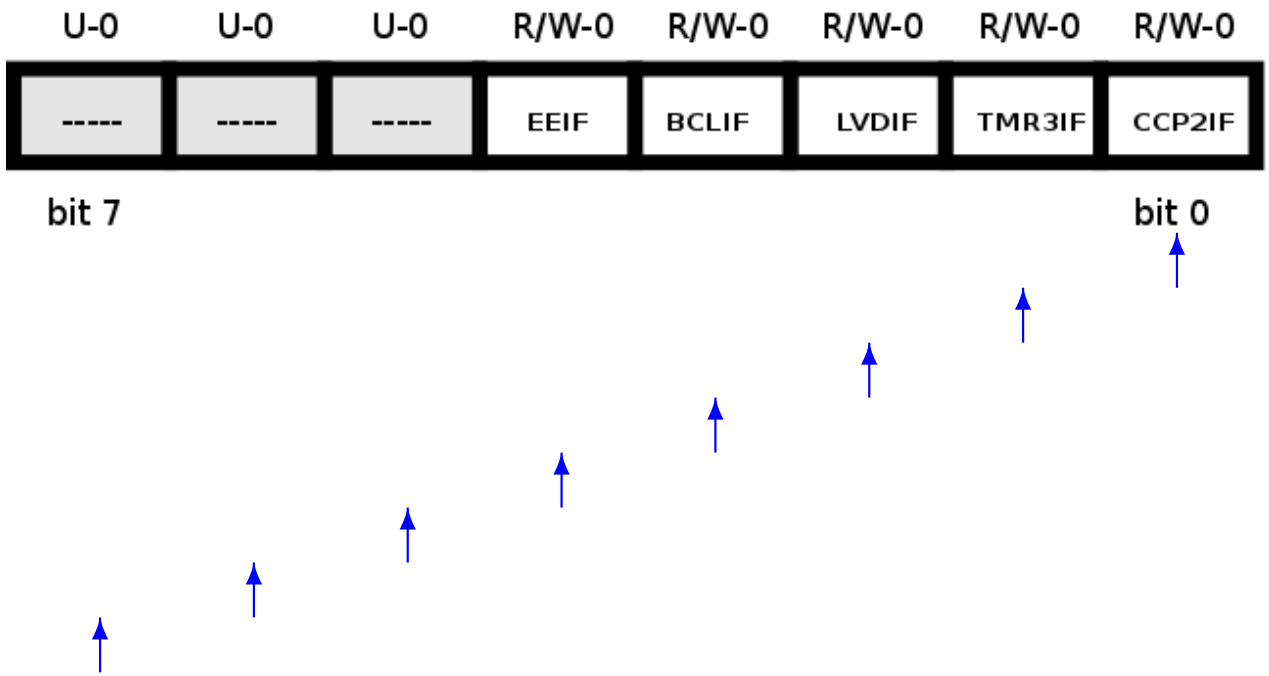
IPR2



Bits in IPR2 register

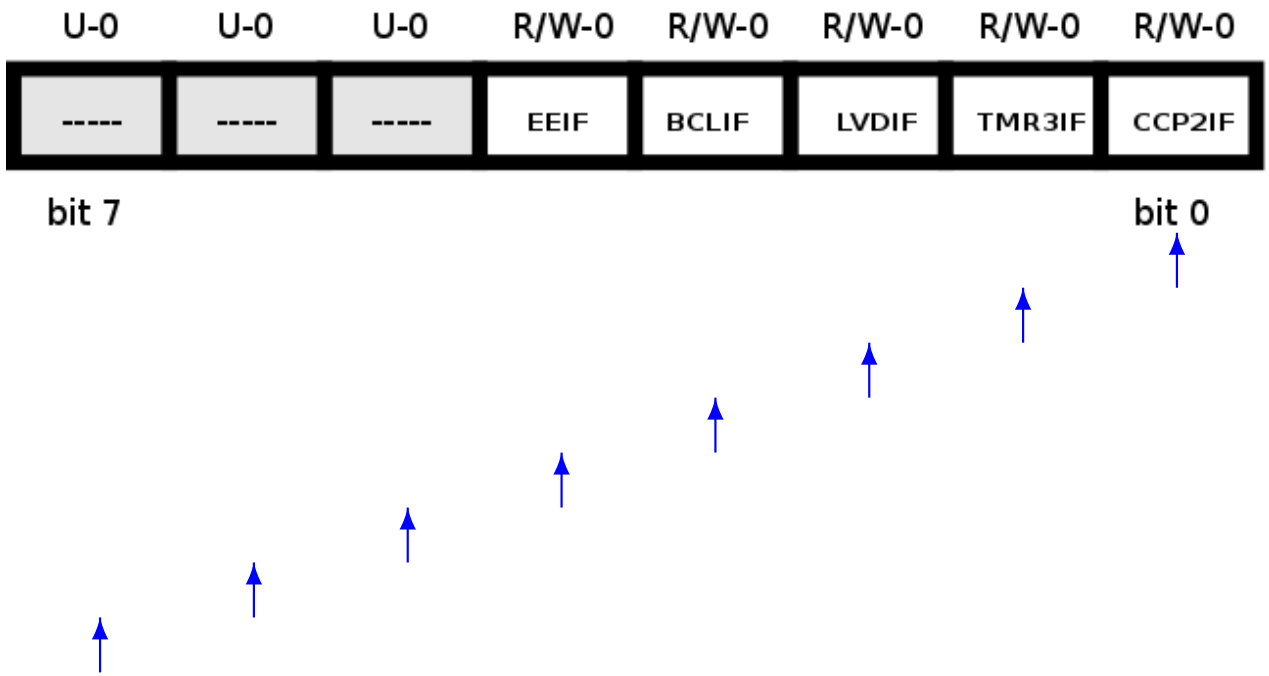
PIR2

PIR2


U-0
U-0
U-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0

EEIF
BCLIF
LVDIF
TMR3IF
CCP2IF
bit 7
bit 0

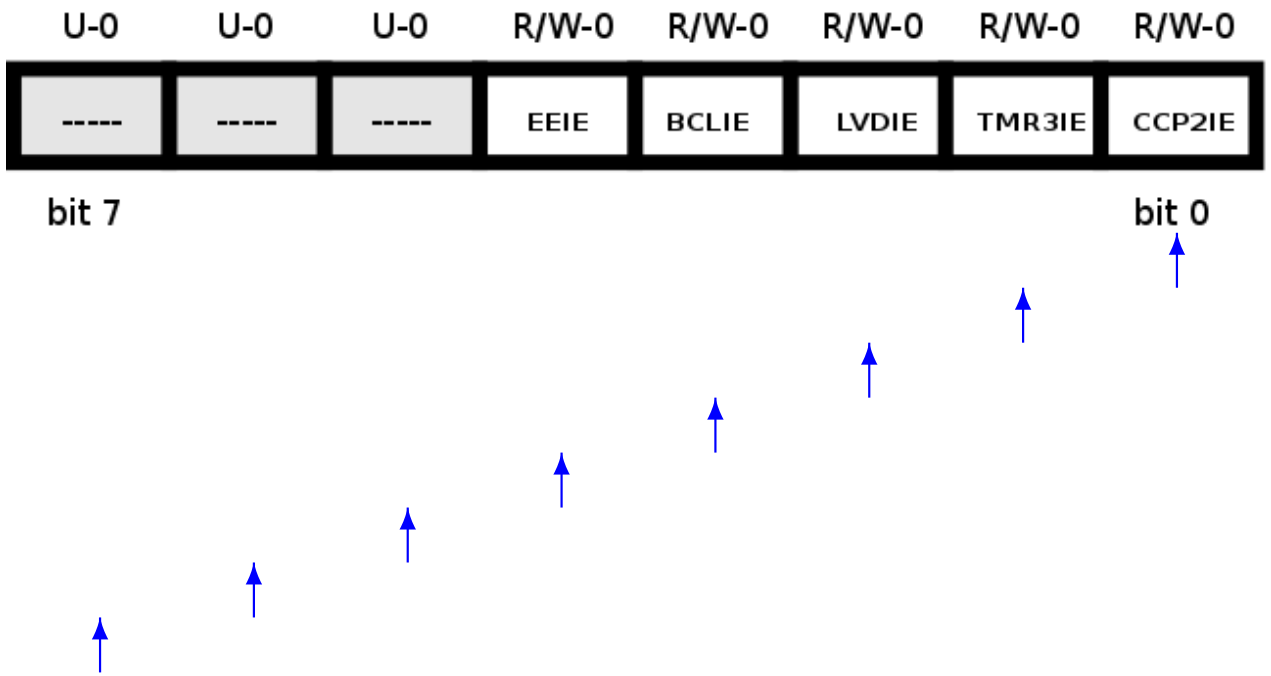
PIR2



Bits in PIR2 register

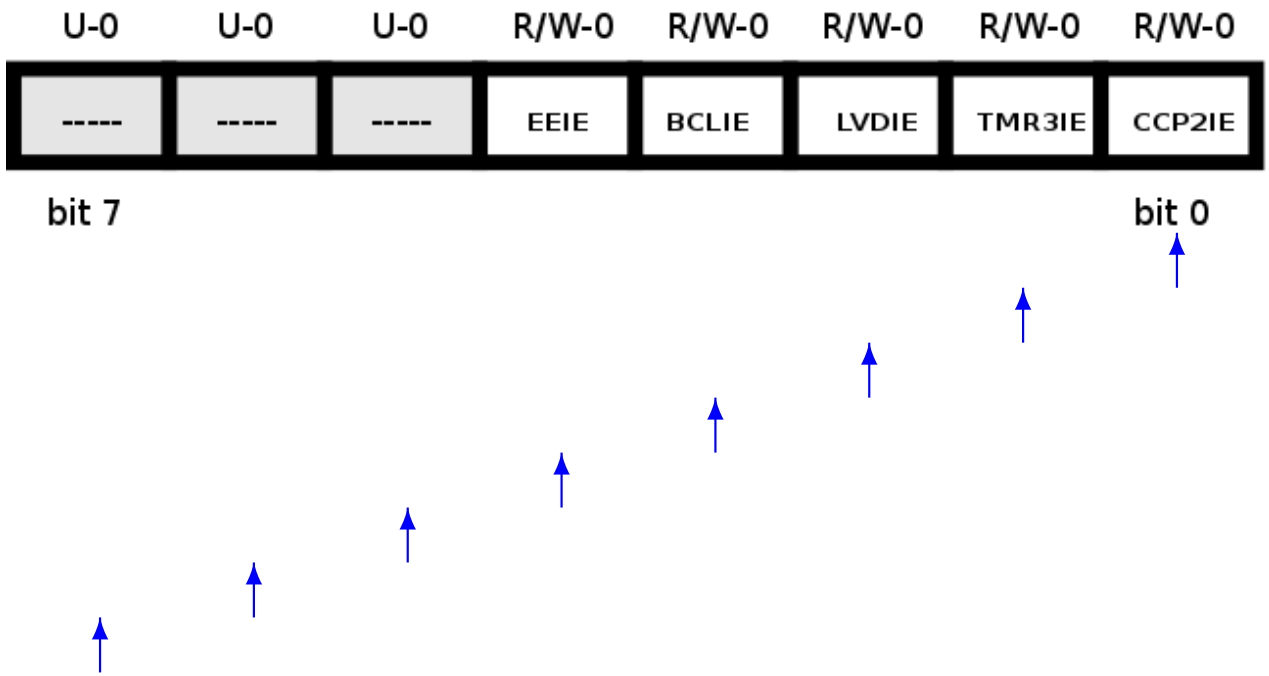
PIE2

PIE2


U-0
U-0
U-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0

EEIE
BCLIE
LVDIE
TMR3IE
CCP2IE
bit 7
bit 0

PIE2



Bits in PIE2 register