CP316
Serial Communication-I2C

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Serial Communication -I^2C

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- Inter-Integrated Circuit Interface

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- Master/slave communication

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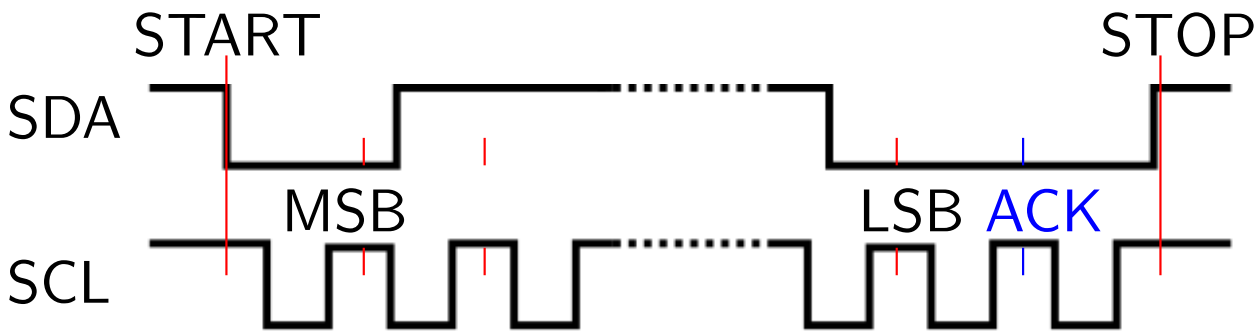
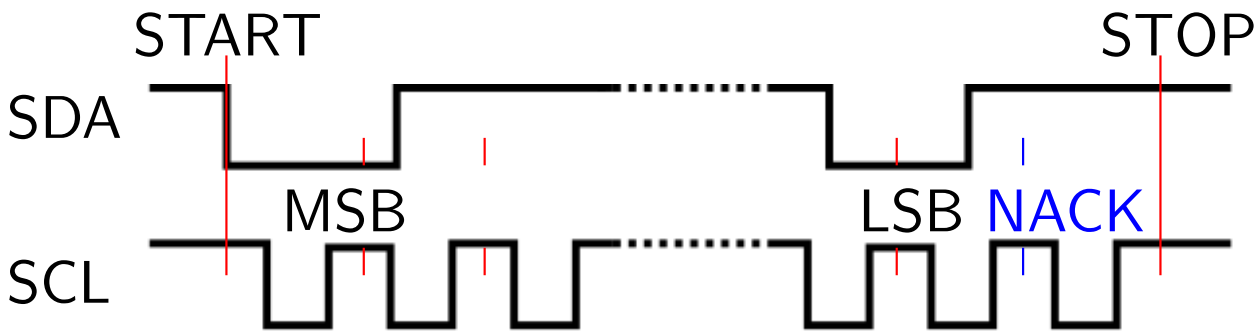
- Synchronous, so master controls clock rate



- I^2C ; bits are read when SCL is HIGH
- ACK is sent by receiver if OK

  sender must release SDA after LSB



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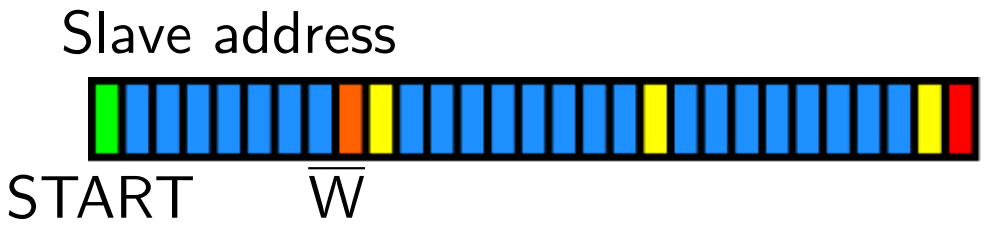
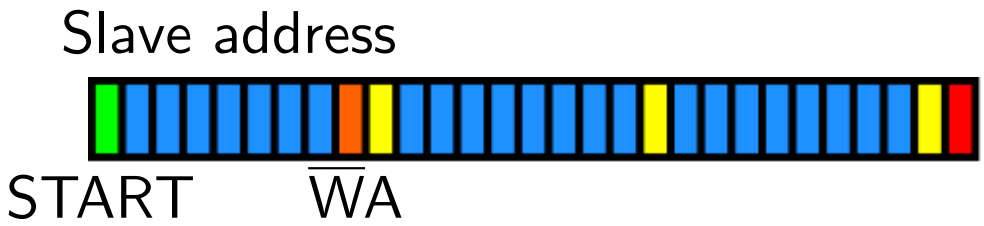
- I^2C write to slave register



- I^2C write to slave register



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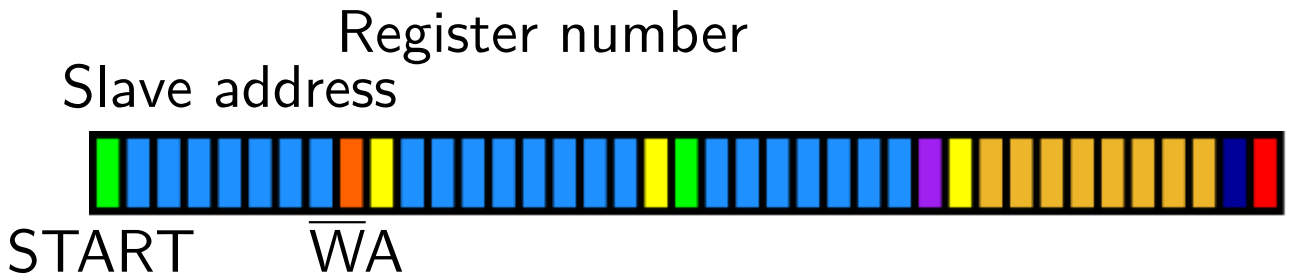
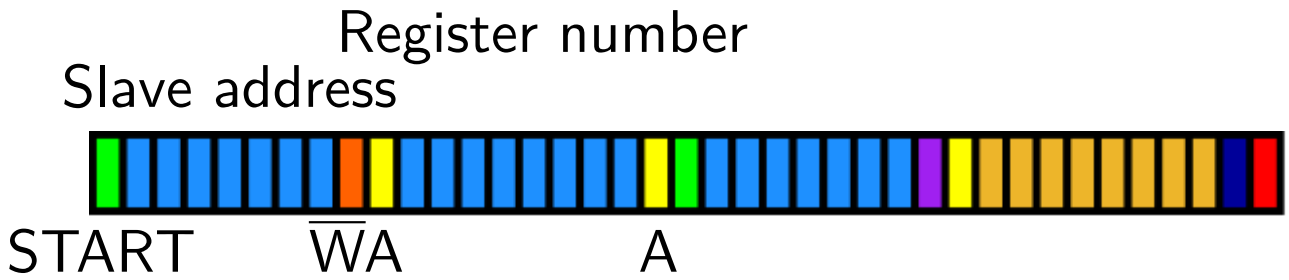


- I^2C read from slave register



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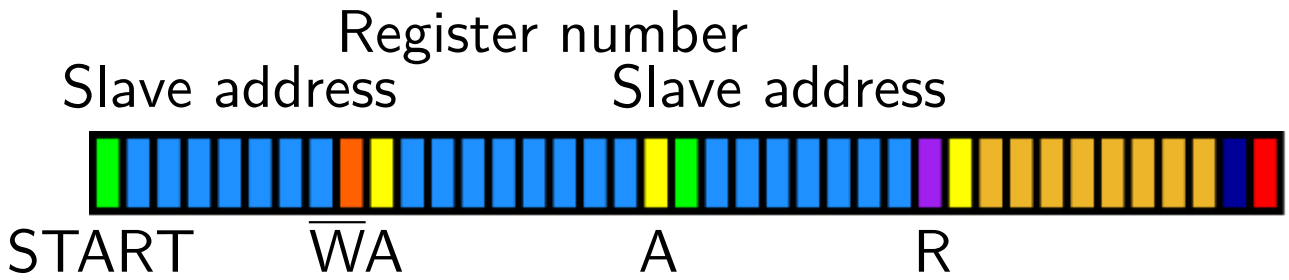

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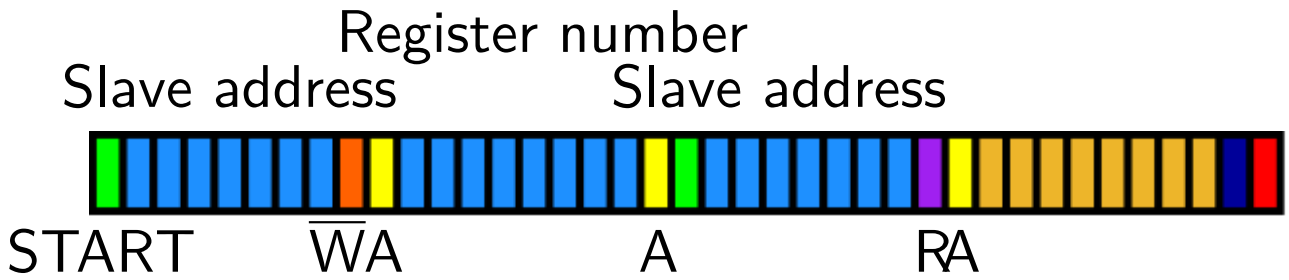

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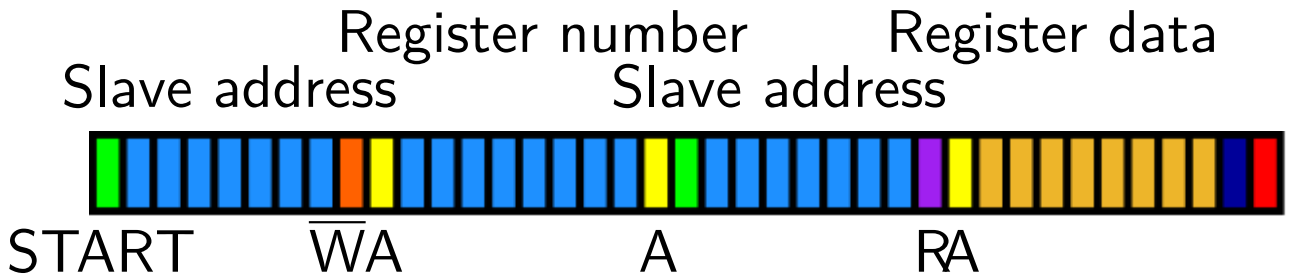

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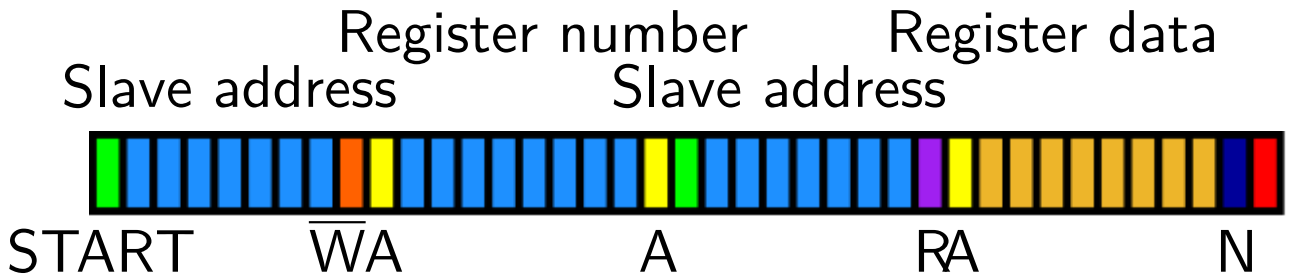

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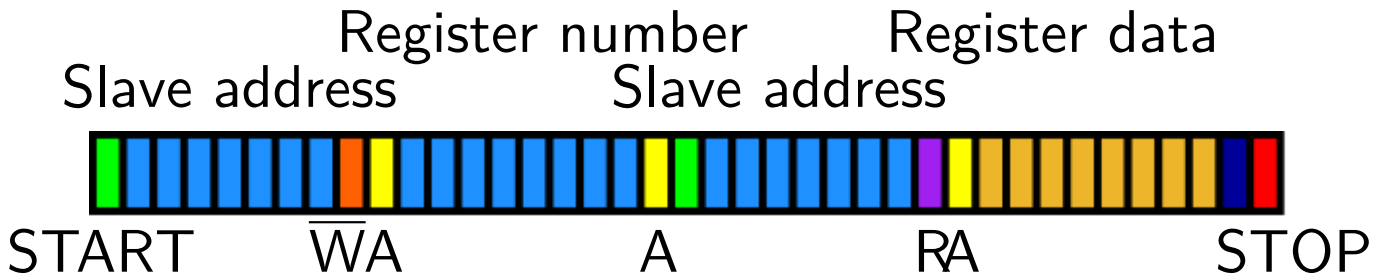

- I^2C read from slave register

Introduction

Introduction

QwikFlash modules

Introduction

QwikFlash modules

ramifications???

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interrupts; transmit and receive

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interrupts; transmit and receive

$\rightarrow$ Sections 6.4.5 to 6.4.7

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QwikFlash modules

ramifications???

interrupts; transmit and receive

→ Sections 6.4.5 to 6.4.7

→ Section 8.2

QwikFlash I^2C connections

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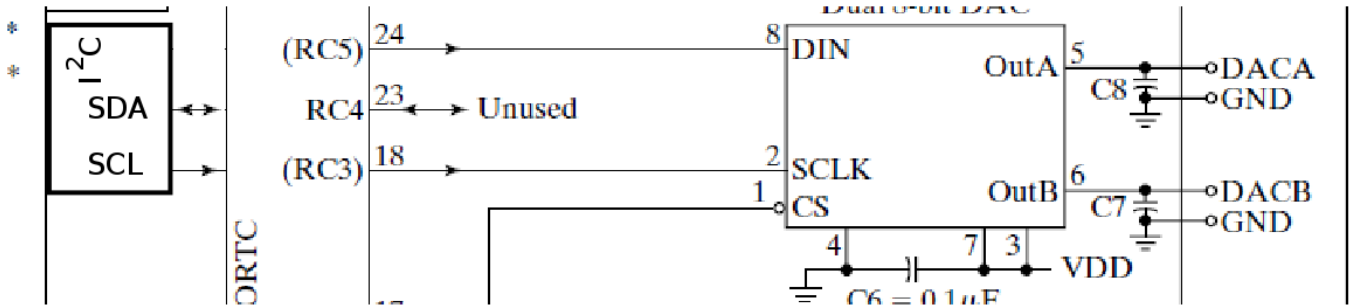

Master Synchronous Serial Port (MSSP) module

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2 modes; **SPI** and $\mathrm{I}^2\mathrm{C}$

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2 modes; **SPI** and I^2C

$\rightarrow$ Section 15.0 -15.2

I^2C

I^2C

2 wires, master-multiple slave

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2 wires, master-multiple slave

overview

I^2C

2 wires, master-multiple slave

overview

$\rightarrow$ Section 11.2

I^2C

2 wires, master-multiple slave

overview

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I^2C module

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2 wires, master-multiple slave

overview

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I^2C module

$\rightarrow$ Sections 11.3 to 11.6

I^2C

2 wires, master-multiple slave

overview

→ Section 11.2

I^2C module

→ Sections 11.3 to 11.6

→ Section 15.4

I^2C summary

I^2C summary

2 wires (+ ground), one-to-many

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SCL (from master)

I^2C summary

2 wires (+ ground), one-to-many

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SDA (serial data)

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2 wires (+ ground), one-to-many

SCL (from master)

SDA (serial data)

data transmission rate set by SCL

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2 wires (+ ground), one-to-many

SCL (from master)

SDA (serial data)

data transmission rate set by SCL

address for each device, preset (but possibly programmable)

I^2C summary

2 wires (+ ground), one-to-many

SCL (from master)

SDA (serial data)

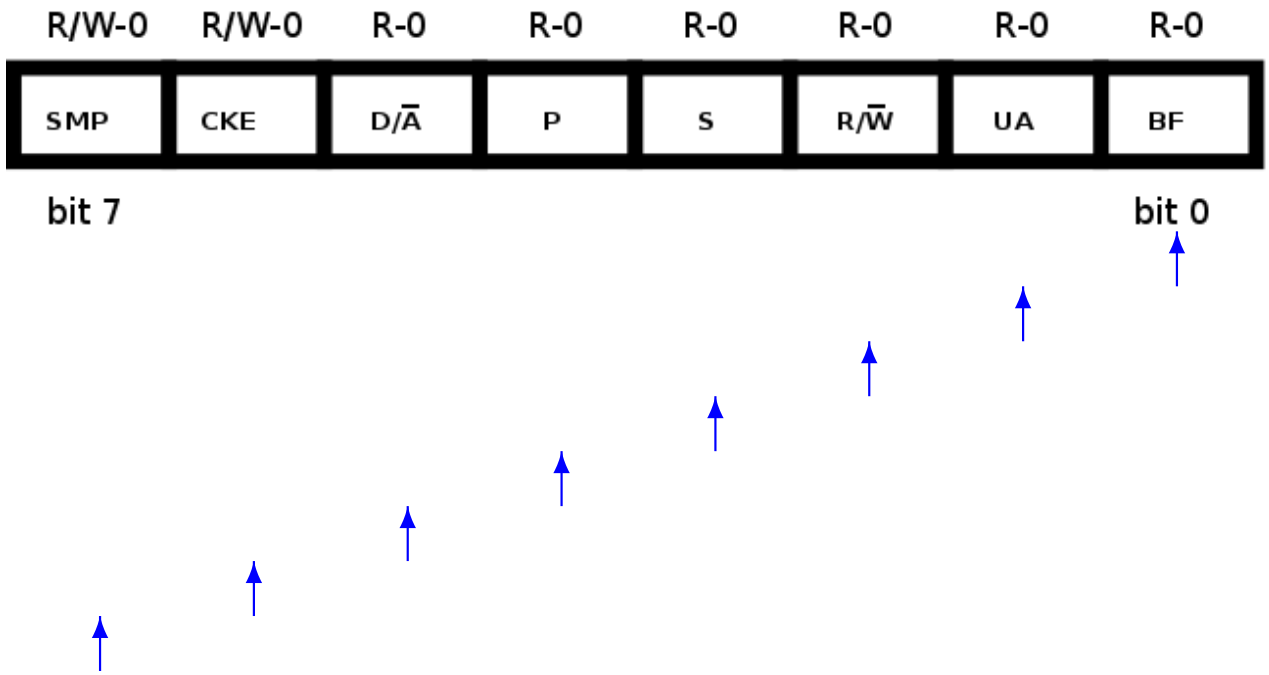
data transmission rate set by SCL

address for each device, preset (but possibly programmable)

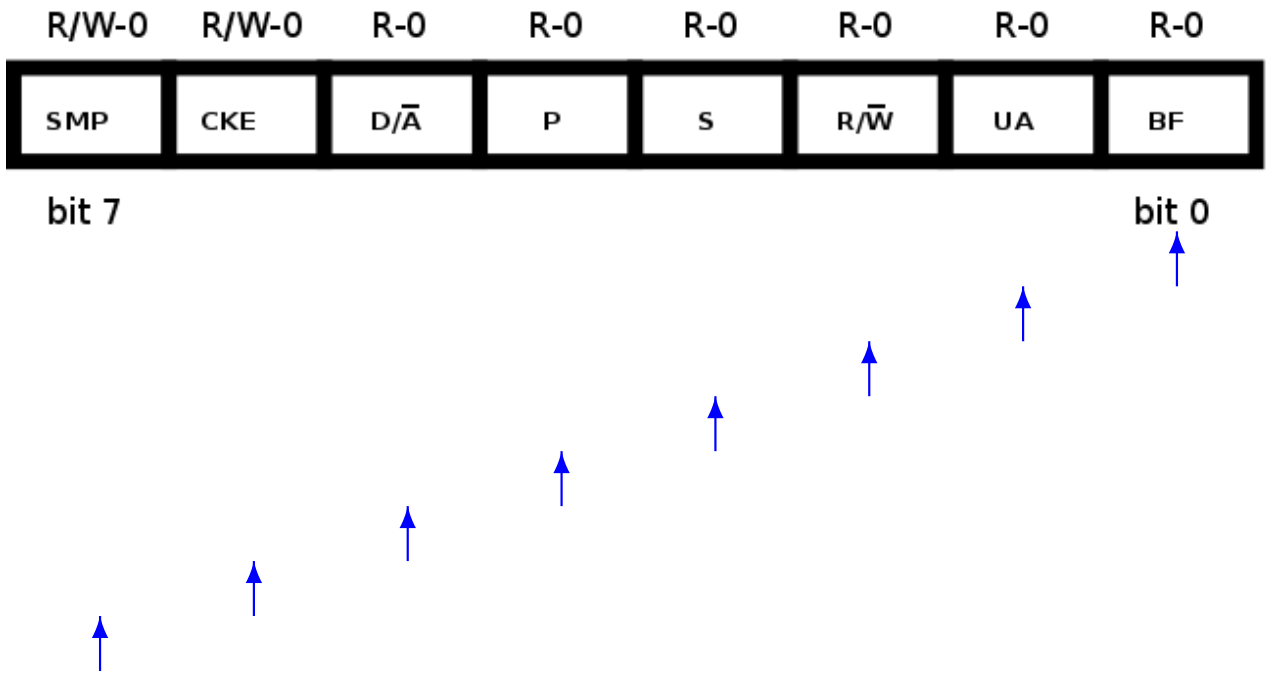
packets are complex; address of recipient, read or write, data (variable number of bytes)

SSPSTAT

SSPSTAT



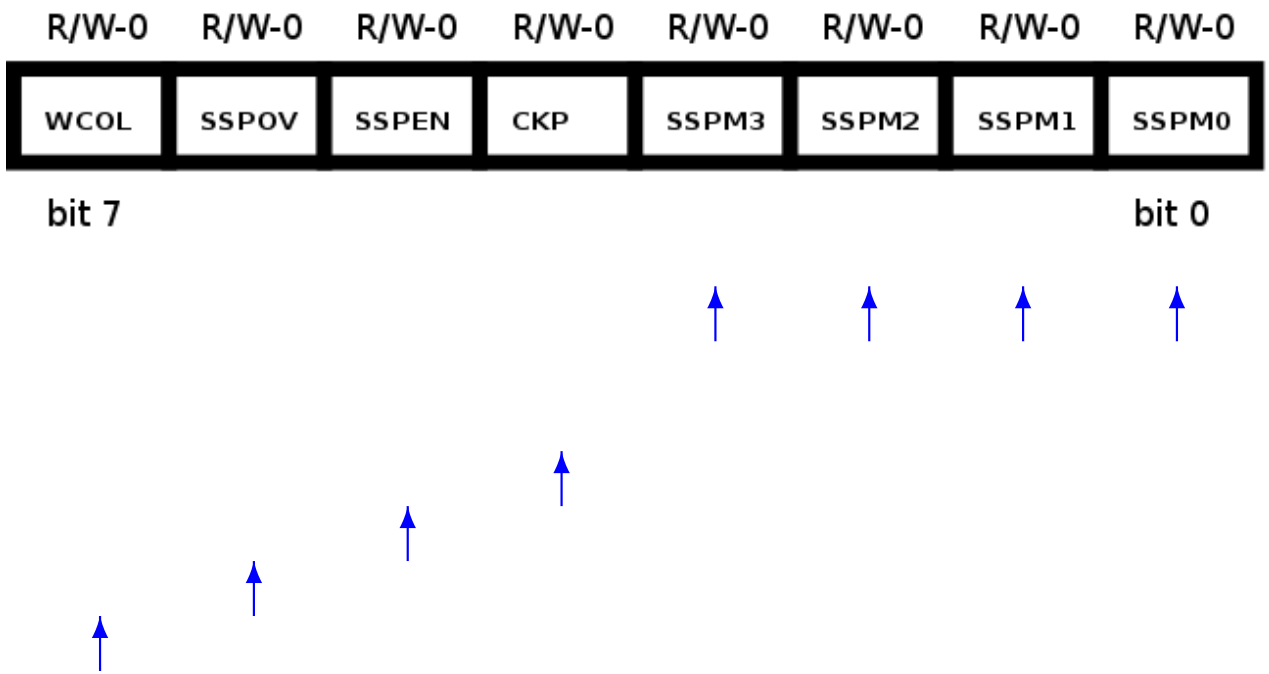
SSPSTAT



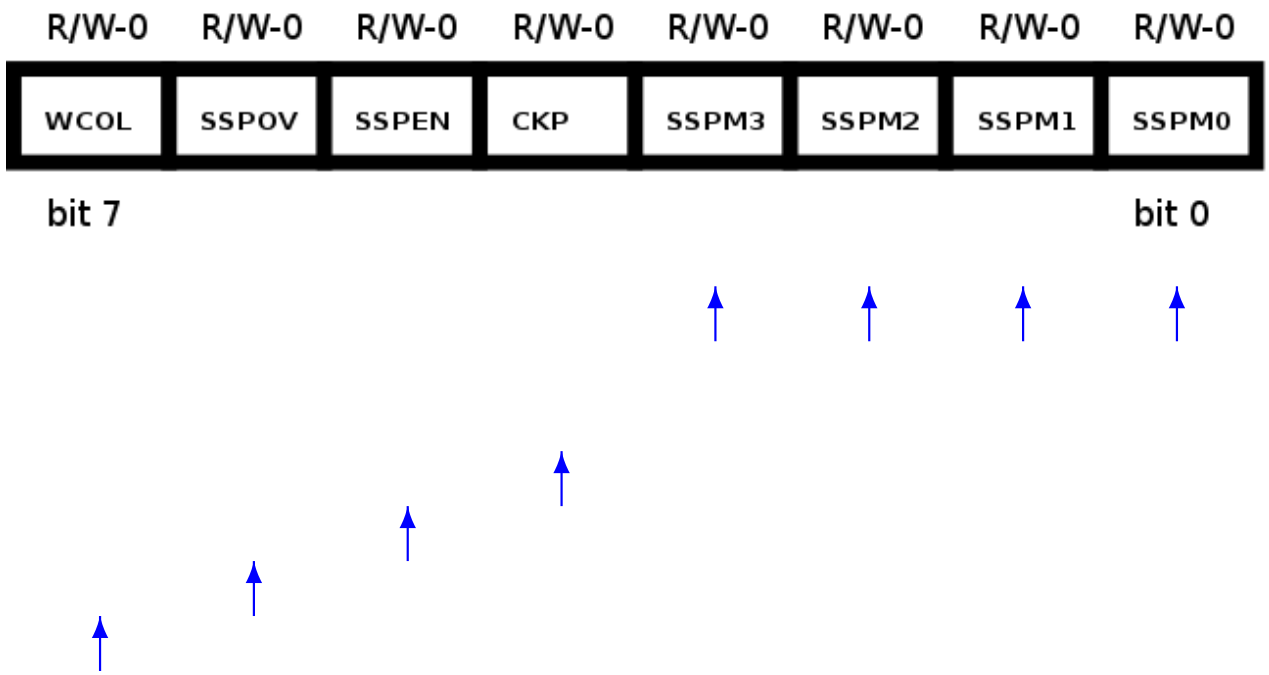
Bits in SSPSTAT register

SSPCON1

SSPCON1


R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
WCOL
SSPOV
SSPEN
CKP
SSPM3
SSPM2
SSPM1
SSPM0
bit 7
bit 0

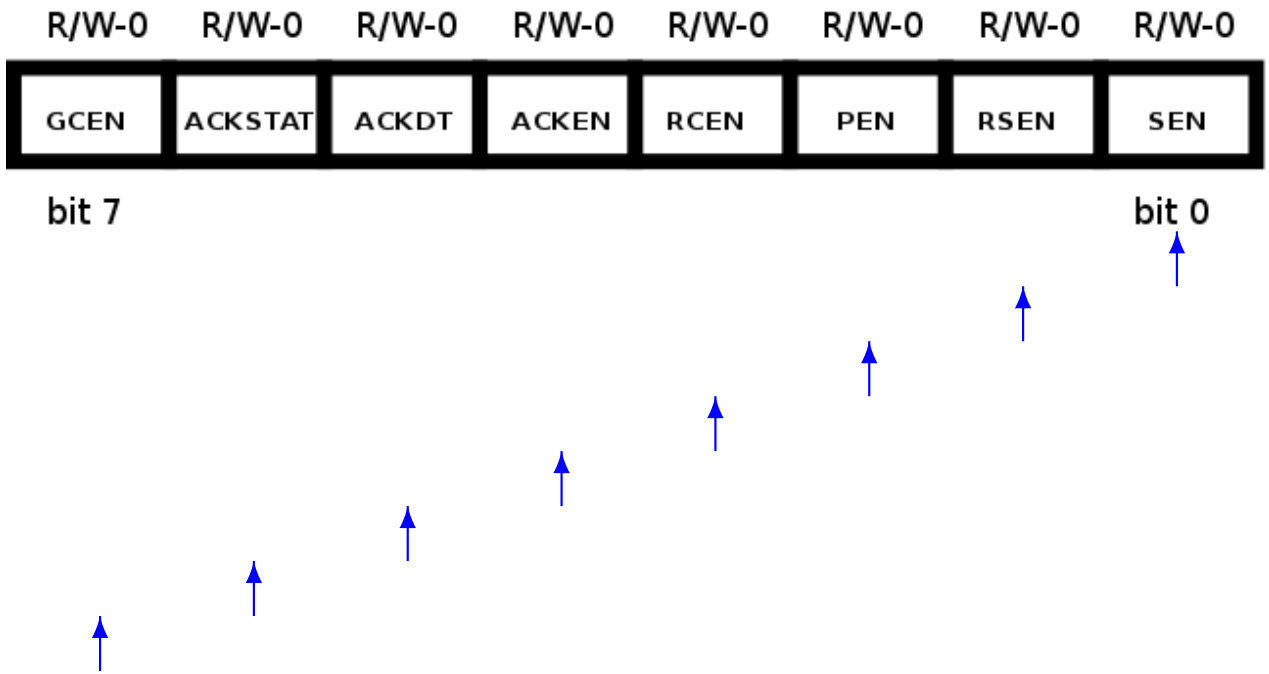
SSPCON1



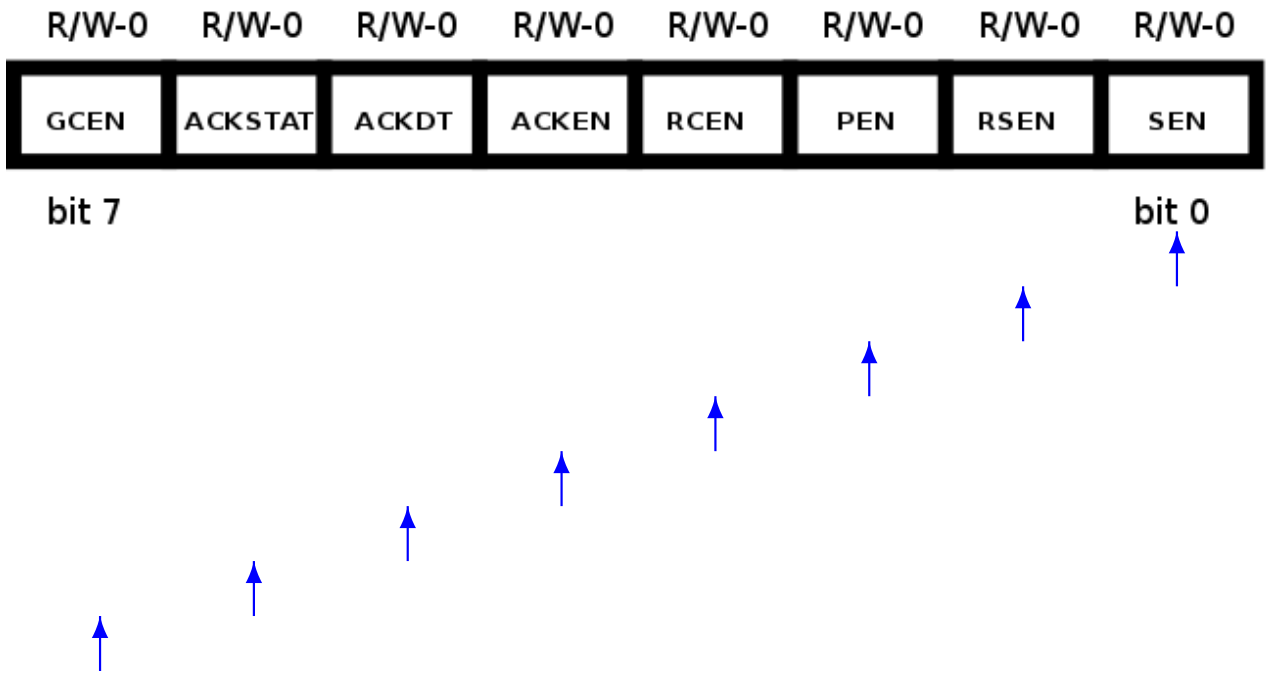
Bits in SSPCON1 register

SSPCON2

SSPCON2


R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
GCEN
ACKSTAT
ACKDT
ACKEN
RCEN
PEN
RSEN
SEN
bit 7
bit 0

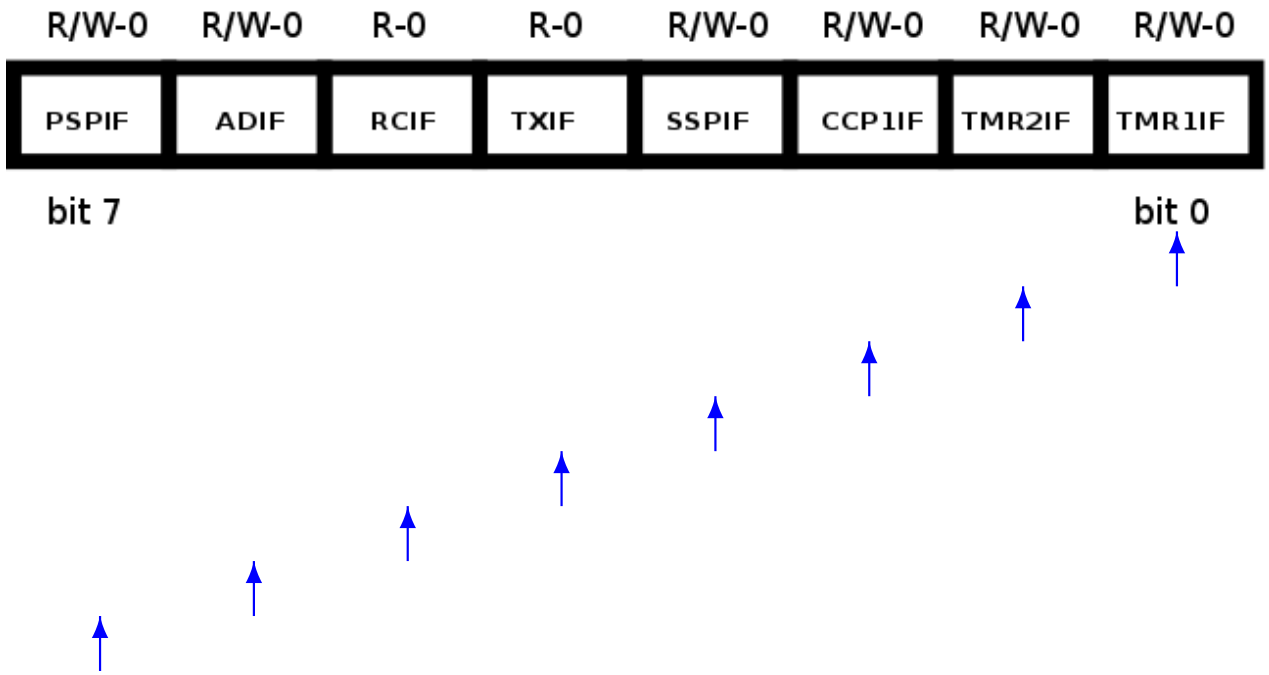
SSPCON2



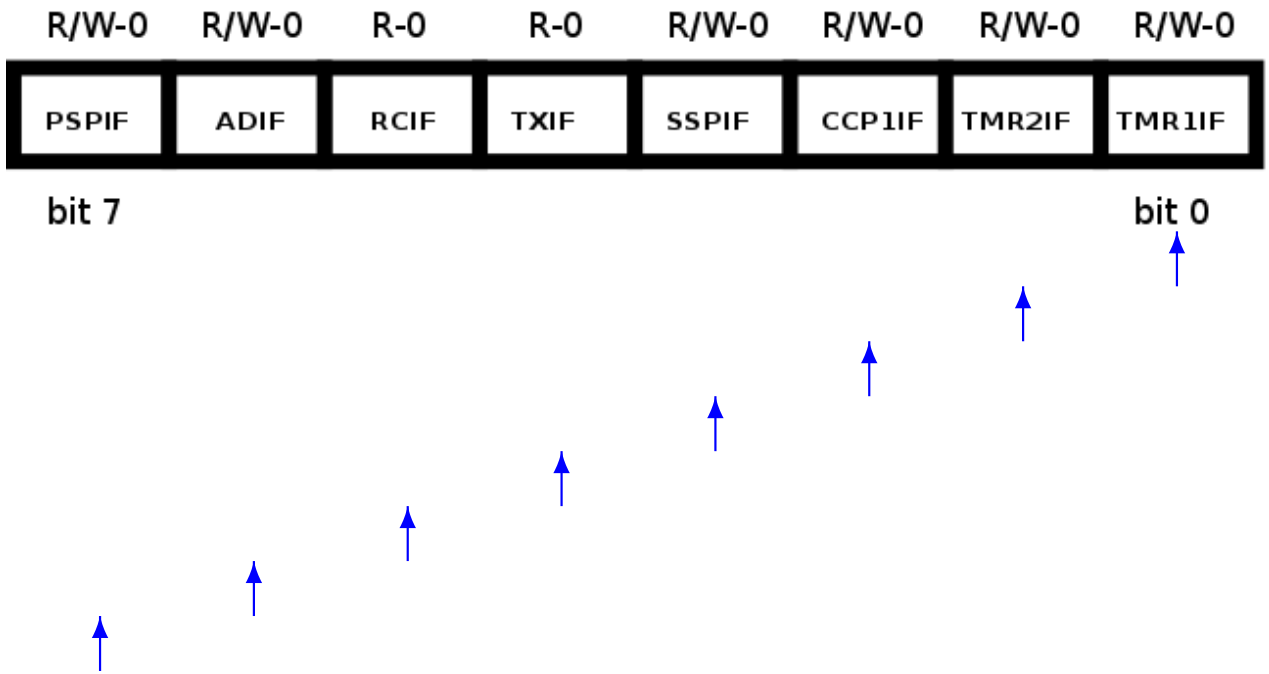
Bits in SSPCON2 register

PIR1

PIR1

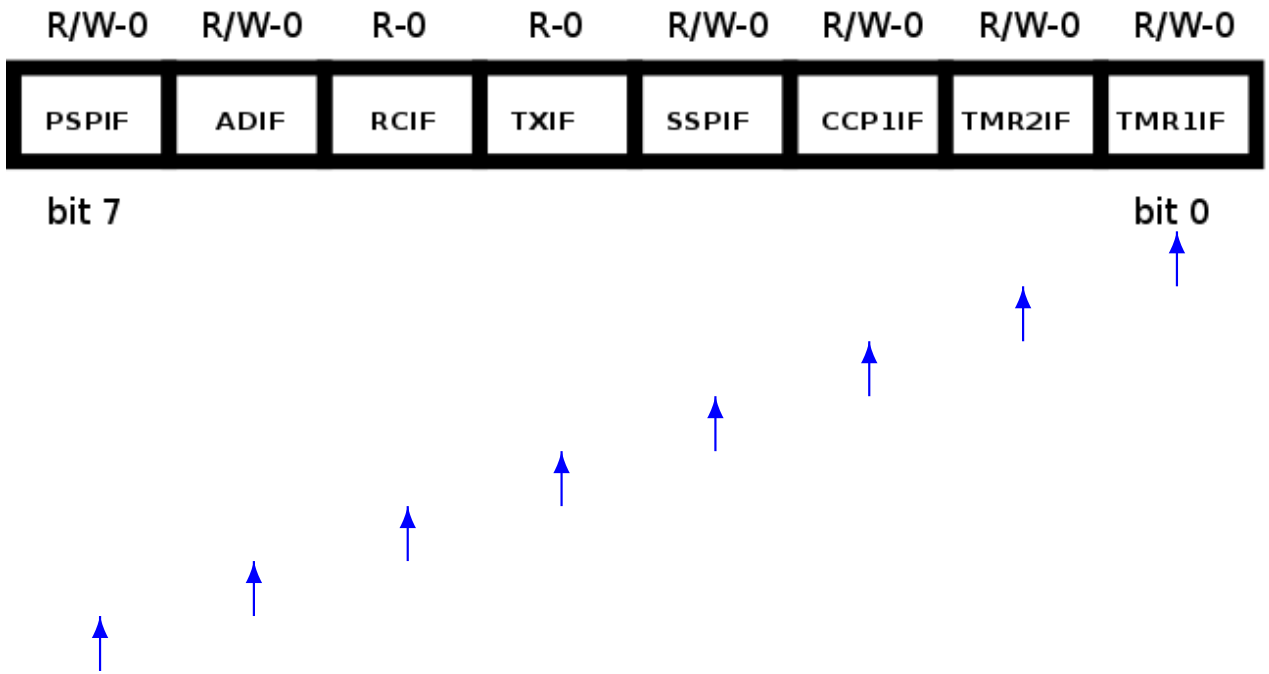

R/W-0
R/W-0
R-0
R-0
R/W-0
R/W-0
R/W-0
R/W-0
PSPIF
ADIF
RCIF
TXIF
SSPIF
CCP1IF
TMR2IF
TMR1IF
bit 7
bit 0

PIR1



Bits in PIR1 register

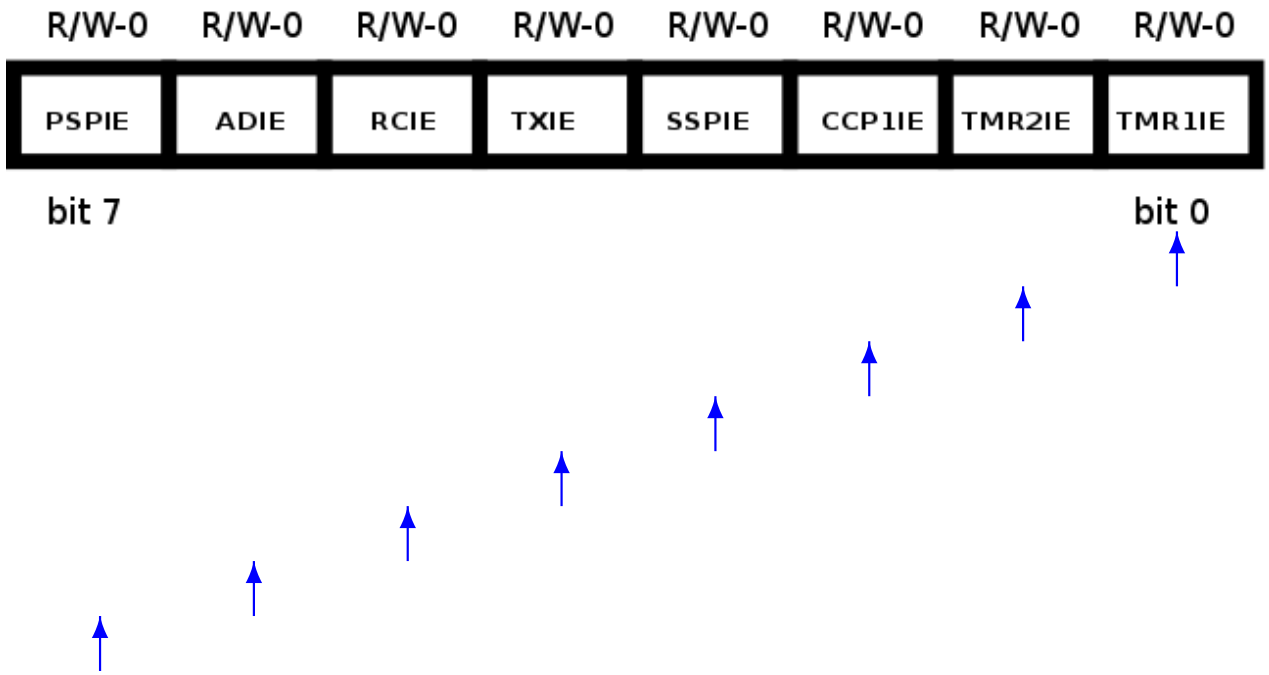
PIR1



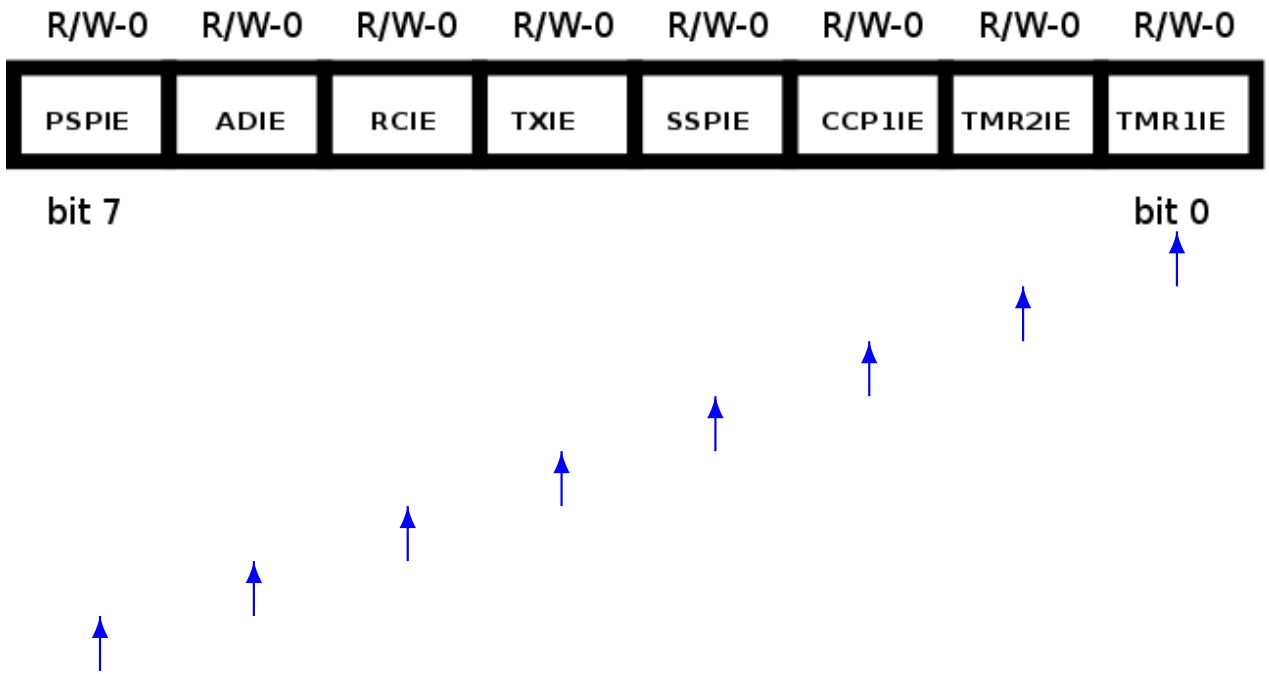
Bits in PIR1 register - Note SSPIF

PIE1

PIE1

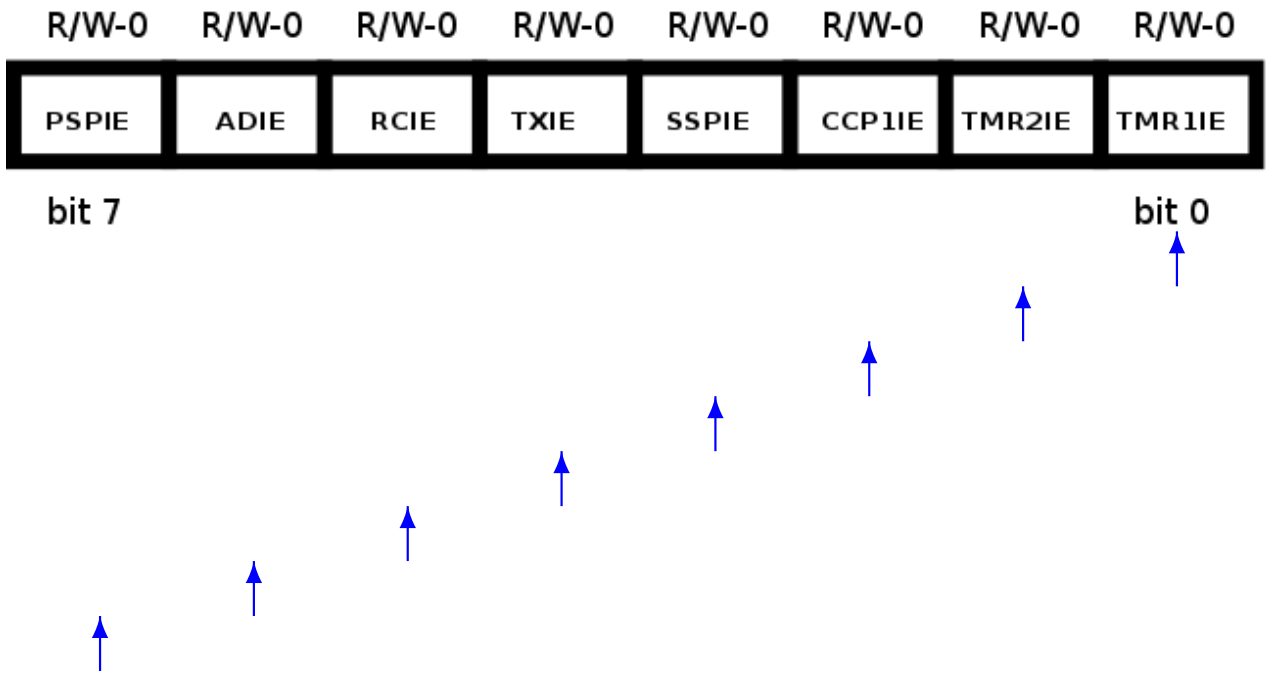

R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
R/W-0
PSPIE
ADIE
RCIE
TXIE
SSPIE
CCP1IE
TMR2IE
TMR1IE
bit 7
bit 0

PIE1



Bits in PIE1 register

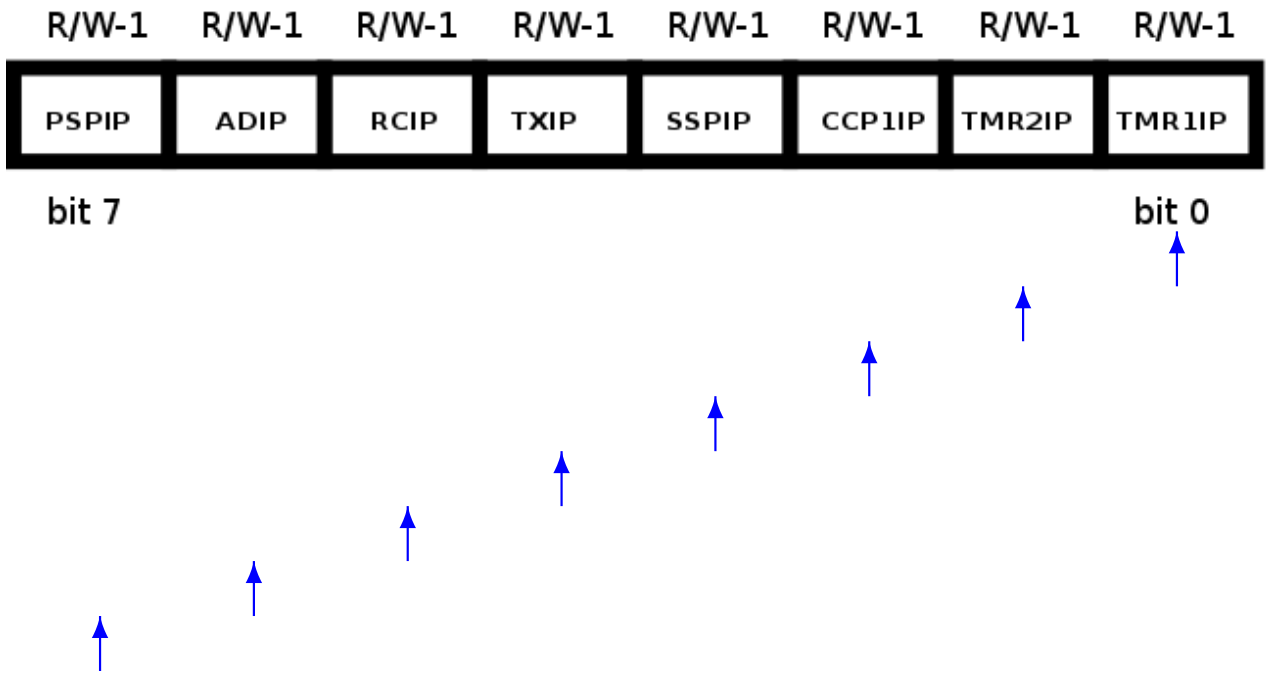
PIE1



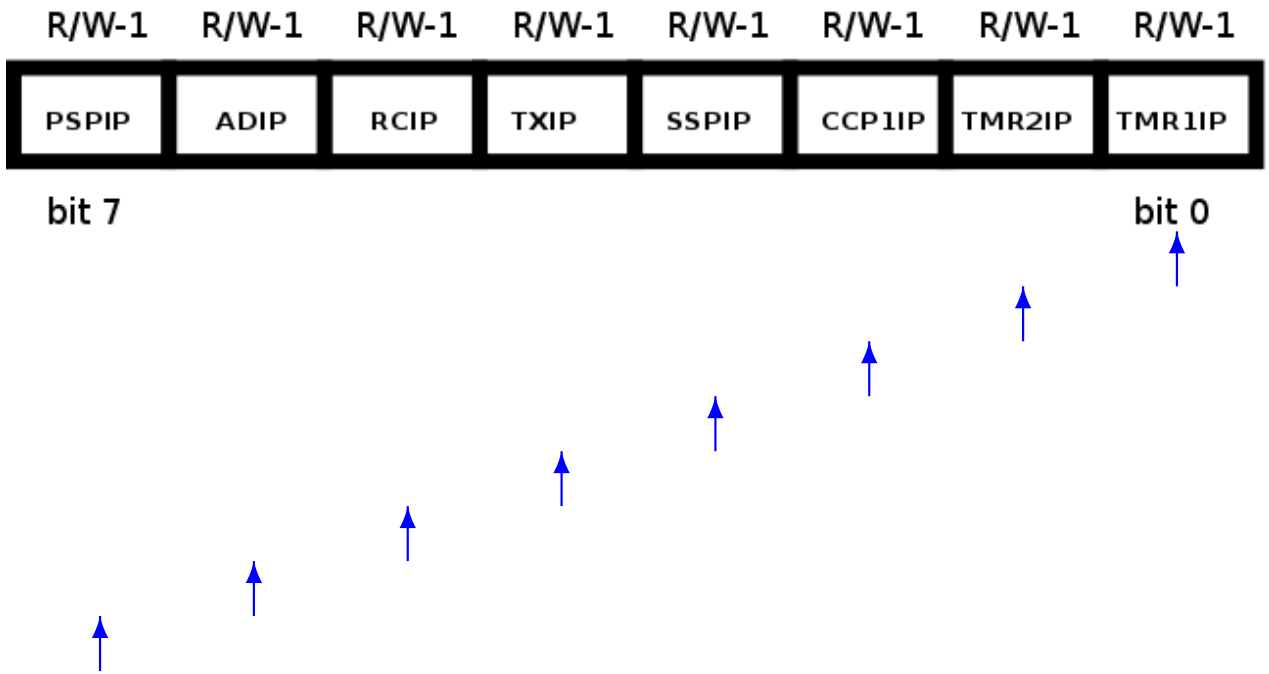
Bits in PIE1 register - Note SSPIE

IPR1

IPR1


R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
R/W-1
PSPIP
ADIP
RCIP
TXIP
SSPIP
CCP1IP
TMR2IP
TMR1IP
bit 7
bit 0

IPR1



Bits in IPR1 register

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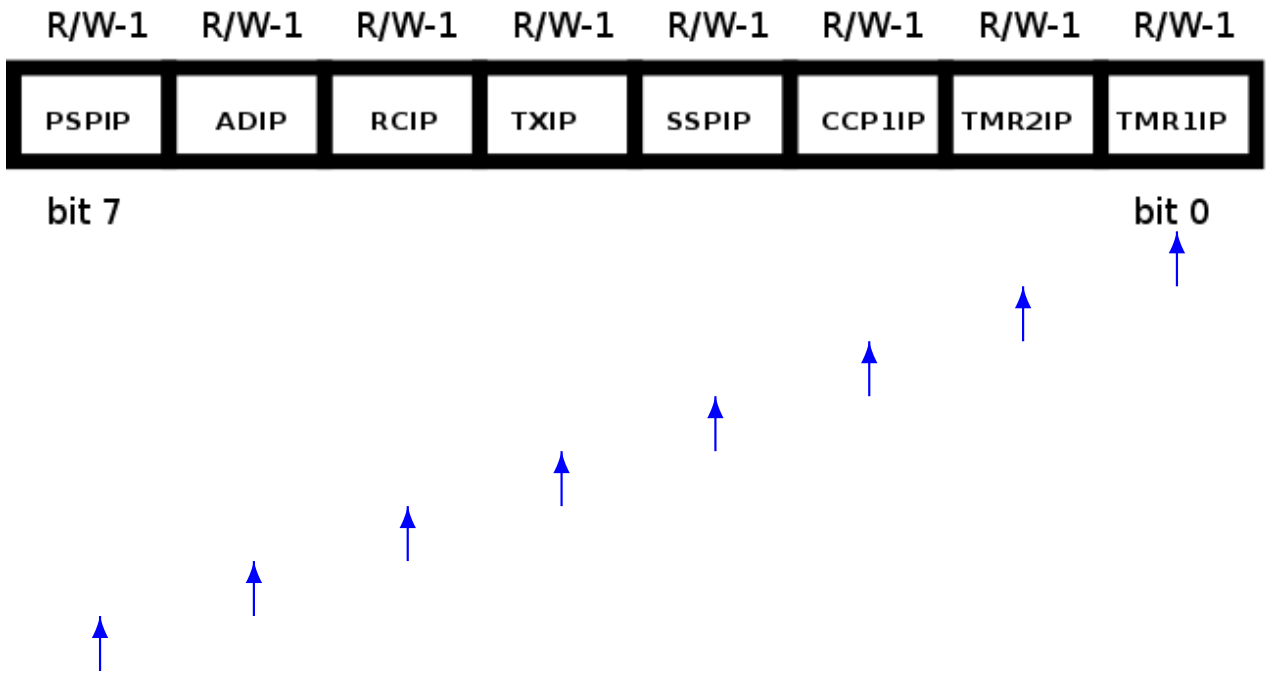

Bits in IPR1 register - Note SSPIP

Bit-bashing

Bit-bashing

overview

Bit-bashing

overview

reasons

Bit-bashing

overview

reasons

NIB

Code

Code

PORT configuration

Code

PORT configuration

$\rightarrow$ macro or subroutine?

Code

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$\rightarrow$ macro or subroutine?

Initialization

Code

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Code

PORT configuration

$\rightarrow$ macro or subroutine?

Initialization

$\rightarrow$ macro or subroutine?

Write to device

Code

PORT configuration

→ macro or subroutine?

Initialization

→ macro or subroutine?

Write to device

→ macro or subroutine?

Code

PORT configuration

→ macro or subroutine?

Initialization

→ macro or subroutine?

Write to device

→ macro or subroutine?

Read from device

Code

PORT configuration

→ macro or subroutine?

Initialization

→ macro or subroutine?

Write to device

→ macro or subroutine?

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Initialization

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4. enable interrupts (if desired) (**PIE1** , **IPR1**)

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   I^2C , master, enable, etc.
3. set other parameters (**SSPSTAT**,**SSPADD**)

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4. enable interrupts (if desired) (**PIE1** , **IPR1**)

   assuming interrupts are enabled globally

Sending

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Sending data to slave

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1. *start*; (**SSPSTAT**)

Sending

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1. *start*; (**SSPSTAT**)
2. *write address*; (**SSPBUF**,**SSPSTAT**)

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1. *start*; (**SSPSTAT**)
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3. *idle*; (**SSPCON2**, **SSPSTAT**)

Sending

Sending data to slave

1. *start*; (**SSPSTAT**)
2. *write address*; (**SSPBUF**,**SSPSTAT**)
3. *idle*; (**SSPCON2**, **SSPSTAT**)
4. *wait for ACK from receiver*; (**SSPCON2**)

Sending

Sending data to slave

1. *start*; (**SSPSTAT**)
2. *write address*; (**SSPBUF**,**SSPSTAT**)
3. *idle*; (**SSPCON2**, **SSPSTAT**)
4. *wait for ACK from receiver*; (**SSPCON2**)
5. *write data*; (**SSPBUF**,**SSPSTAT**)

Sending

Sending data to slave

1. *start*; (**SSPSTAT**)
2. *write address*; (**SSPBUF**,**SSPSTAT**)
3. *idle*; (**SSPCON2**, **SSPSTAT**)
4. *wait for ACK from receiver*; (**SSPCON2**)
5. *write data*; (**SSPBUF**,**SSPSTAT**)
6. *idle*; (**SSPCON2**, **SSPSTAT**)

Sending

Sending data to slave

1. *start*; (**SSPSTAT**)
2. *write address*; (**SSPBUF**,**SSPSTAT**)
3. *idle*; (**SSPCON2**, **SSPSTAT**)
4. *wait for ACK from receiver*; (**SSPCON2**)
5. *write data*; (**SSPBUF**,**SSPSTAT**)
6. *idle*; (**SSPCON2**, **SSPSTAT**)
7. *wait for ACK from receiver*; (**SSPCON2**)

Sending

Sending data to slave

1. *start*; (**SSPSTAT**)
2. *write address*; (**SSPBUF**,**SSPSTAT**)
3. *idle*; (**SSPCON2**, **SSPSTAT**)
4. *wait for ACK from receiver*; (**SSPCON2**)
5. *write data*; (**SSPBUF**,**SSPSTAT**)
6. *idle*; (**SSPCON2**, **SSPSTAT**)
7. *wait for ACK from receiver*; (**SSPCON2**)
8. *stop*; (**SSPSTAT**)

Sending

Sending data to slave

1. *start*; (**SSPSTAT**)
2. *write address*; (**SSPBUF**,**SSPSTAT**)
3. *idle*; (**SSPCON2**, **SSPSTAT**)
4. *wait for ACK from receiver*; (**SSPCON2**)
5. *write data*; (**SSPBUF**,**SSPSTAT**)
6. *idle*; (**SSPCON2**, **SSPSTAT**)
7. *wait for ACK from receiver*; (**SSPCON2**)
8. *stop*; (**SSPSTAT**)

Receiving

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1. *start*; (**SSPSTAT**)

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2. *write address*; (**SSPBUF**,**SSPSTAT**)
3. *idle*; (**SSPCON2**, **SSPSTAT**)

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5. *read data*; (**SSPBUF**,**SSPSTAT**)
6. *idle*; (**SSPCON2**, **SSPSTAT**)
7. *wait for NACK from receiver*; (**SSPCON2**)

Receiving

Receiving data from slave

1. *start*; (**SSPSTAT**)
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4. *wait for ACK from receiver*; (**SSPCON2**)
5. *read data*; (**SSPBUF**,**SSPSTAT**)
6. *idle*; (**SSPCON2**, **SSPSTAT**)
7. *wait for NACK from receiver*; (**SSPCON2**)
8. *stop*; (**SSPSTAT**)

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