

# CP316

## Serial Communication-I2C

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# Serial Communication -I<sup>2</sup>C

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- Inter-Integrated Circuit Interface

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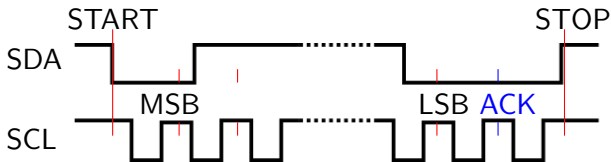
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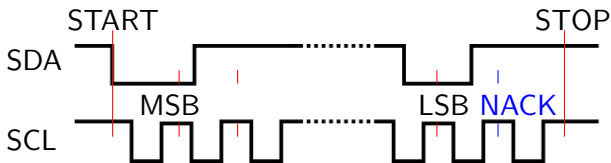
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SDA and SCL
- Many slaves can be on the same bus since each has an address  
*Device addresses are pre-programmed, but can usually be changed*
- Synchronous, so master controls clock rate





- I<sup>2</sup>C ; bits are read when SCL is HIGH
- ACK is sent by receiver if OK  
sender must release SDA after LSB



- I<sup>2</sup>C ; bits are read when SCL is HIGH
- NACK is sent by master-receiver if OK sender must release SDA after LSB



- I<sup>2</sup>C write to slave register



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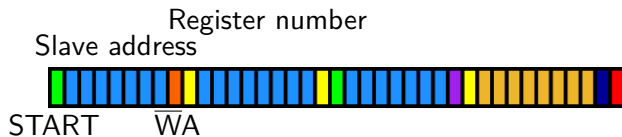
- I<sup>2</sup>C read from slave register



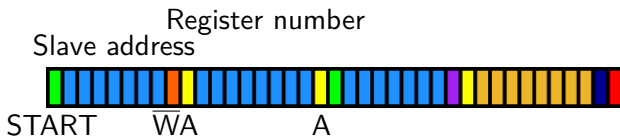
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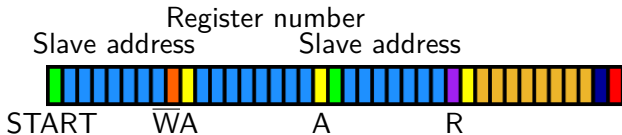
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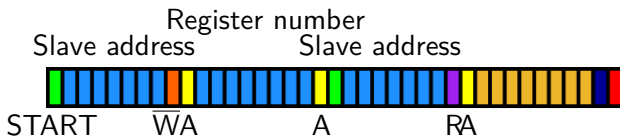
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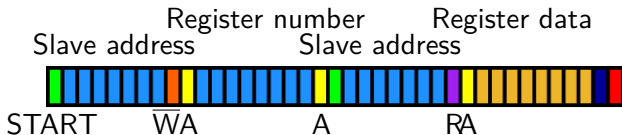


- I<sup>2</sup>C read from slave register

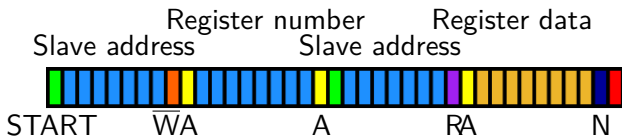


- I<sup>2</sup>C read from slave register

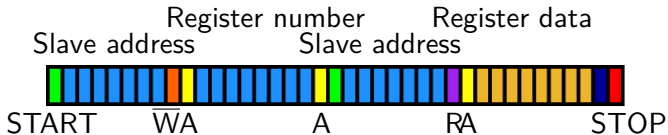




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# Introduction

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QwikFlash modules

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ramifications???

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interrupts; transmit and receive

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→ Sections 6.4.5 to 6.4.7



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QwikFlash modules

ramifications???

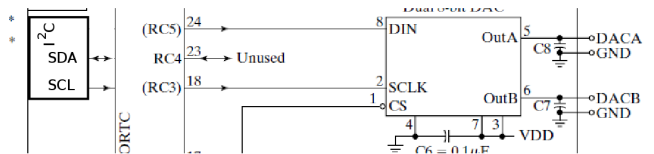
interrupts; transmit and receive

→ Sections 6.4.5 to 6.4.7

→ **Section 8.2**

# QwikFlash I<sup>2</sup>C connections

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# Master Synchronous Serial Port (MSSP) module

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2 modes; **SPI** and **I<sup>2</sup>C**

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→ Section 15.0 -15.2

# I<sup>2</sup>C

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2 wires, master-multiple slave



# I<sup>2</sup>C

2 wires, master-multiple slave  
overview

# I<sup>2</sup>C

2 wires, master-multiple slave

overview

→ Section 11.2

# I<sup>2</sup>C

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I<sup>2</sup>C module

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I<sup>2</sup>C module

→ Sections 11.3 to 11.6

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I<sup>2</sup>C module

→ Sections 11.3 to 11.6

→ Section 15.4

# I<sup>2</sup>C summary

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2 wires (+ ground), one-to-many

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SCL (from master)



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2 wires (+ ground), one-to-many  
SCL (from master)  
SDA (serial data)

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2 wires (+ ground), one-to-many  
SCL (from master)  
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data transmission rate set by SCL

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address for each device, preset (but possibly programmable)

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2 wires (+ ground), one-to-many

SCL (from master)

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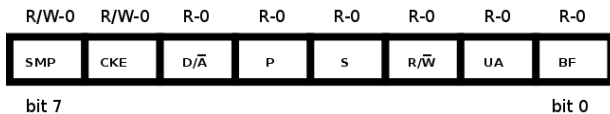
data transmission rate set by SCL

address for each device, preset (but possibly programmable)

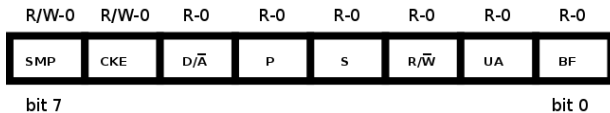
packets are complex; address of recipient, read or write, data  
(variable number of bytes)

# SSPSTAT

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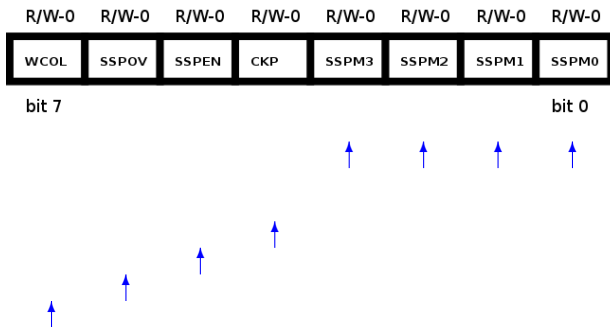


Bits in SSPSTAT register

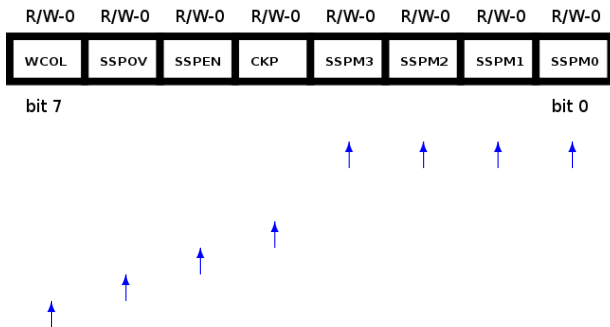
# SSPCON1



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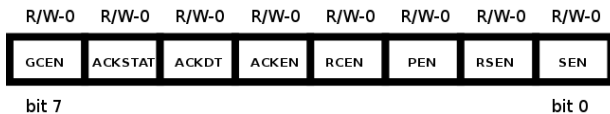
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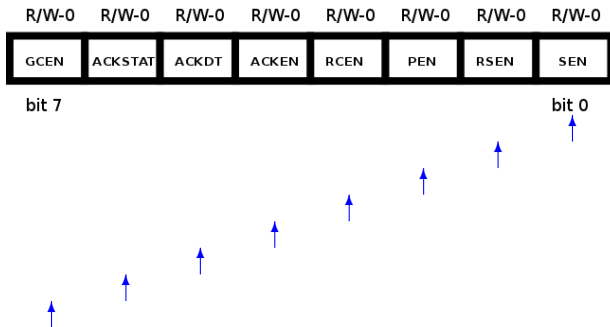
Bits in SSPCON1 register

# SSPCON2

# SSPCON2



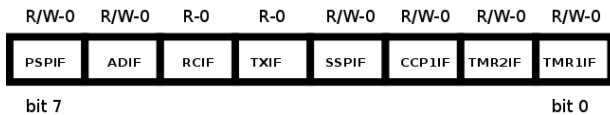
# SSPCON2



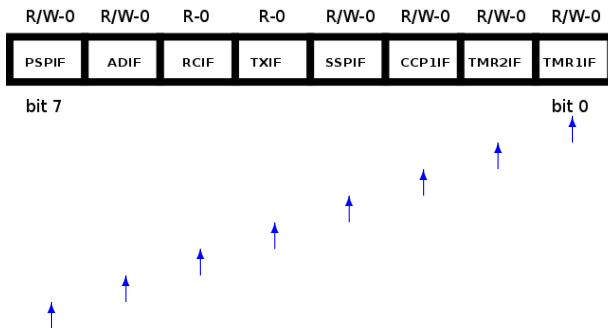
Bits in SSPCON2 register

# PIR1

# PIR1



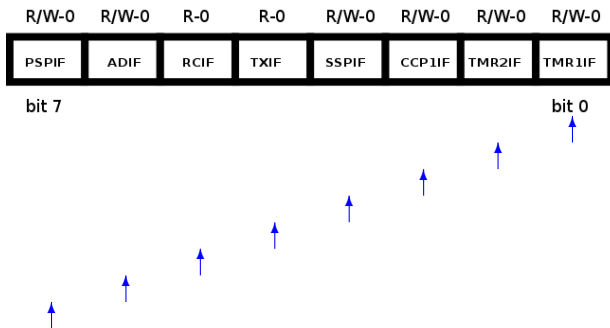
# PIR1



Bits in PIR1 register



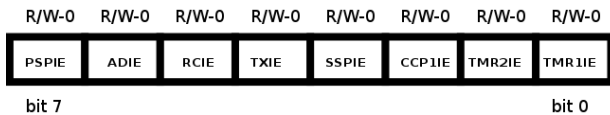
# PIR1



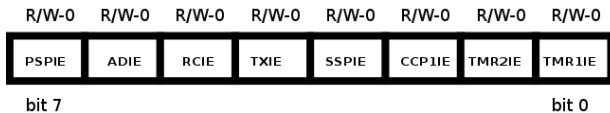
Bits in PIR1 register - Note SSPIF

# PIE1

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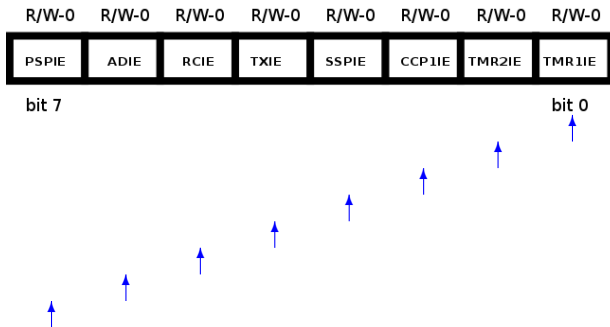


# PIE1



Bits in PIE1 register

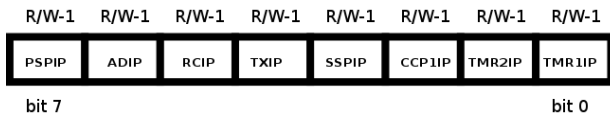
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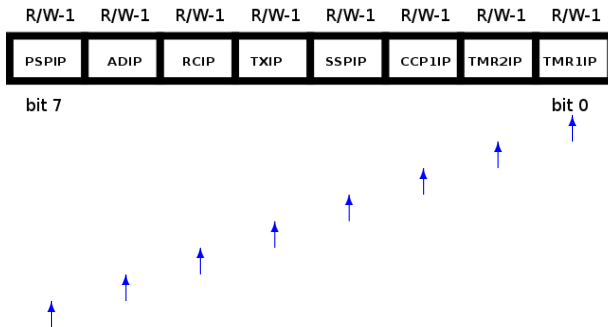
Bits in PIE1 register - Note SSPIE

# IPR1

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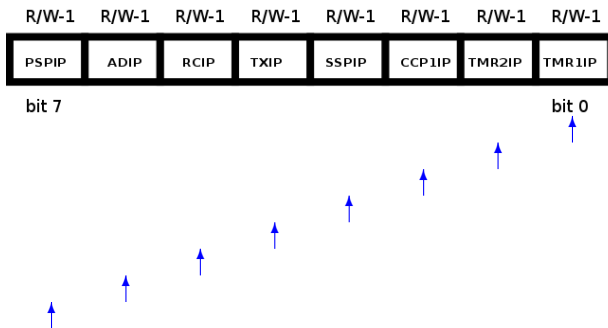
# IPR1



Bits in IPR1 register



# IPR1



Bits in IPR1 register - Note SSPIP

# Bit-bashing

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overview

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overview

reasons

# Bit-bashing

overview

reasons

*NIB*

# Code

# Code

## PORT configuration

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PORT configuration

→ macro or subroutine?



# Code

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→ macro or subroutine?

Initialization

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Write to device

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