

LCD Timing

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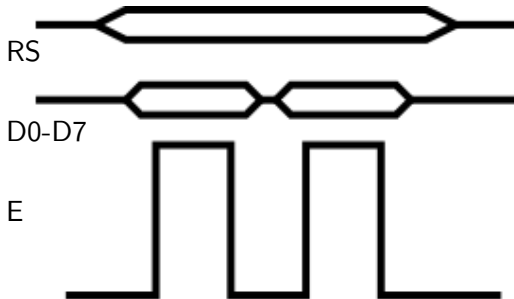
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Note: until initialization is complete, and 4 bit mode is set, the interface is 8 bits wide, although the bottom four bits are ignored.

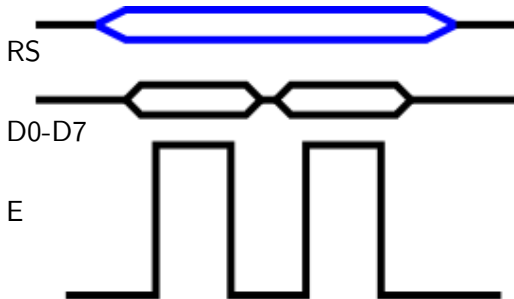
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Note: until initialization is complete, and 4 bit mode is set, the interface is 8 bits wide, although the bottom four bits are ignored. This means only one enable per byte until 4 bit mode is set.

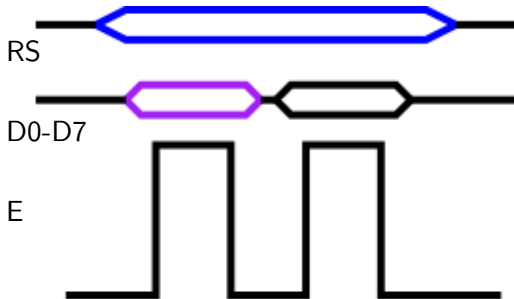
The following illustration applies after initialization is complete.



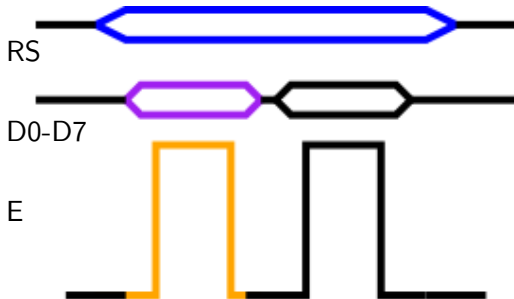
Character timing



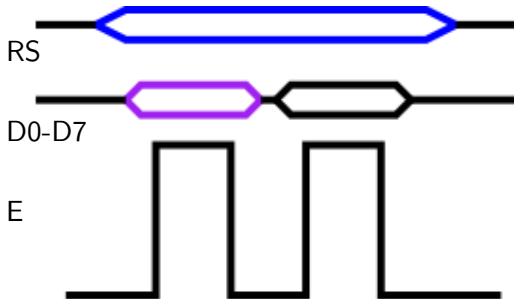
Set RS. Time required before asserting enable t_{AS} - (140ns)



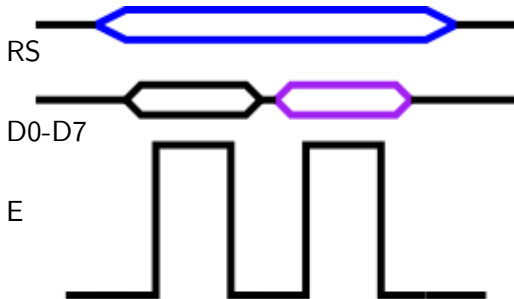
Set up the first (high) nibble.



Assert the enable (E). De-assert after appropriate time PW_{EH} (450ns).

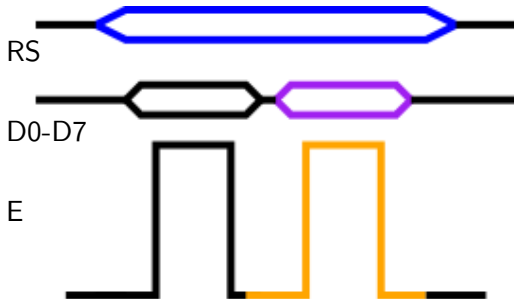


Time required before changing data pins t_H - (10ns)

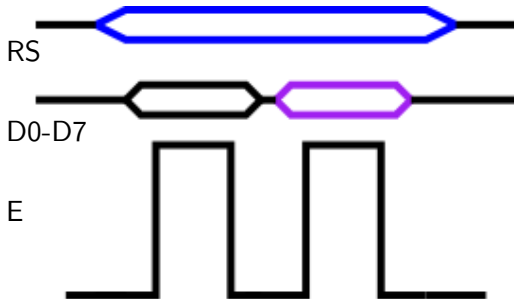


Set up the second (low) nibble.

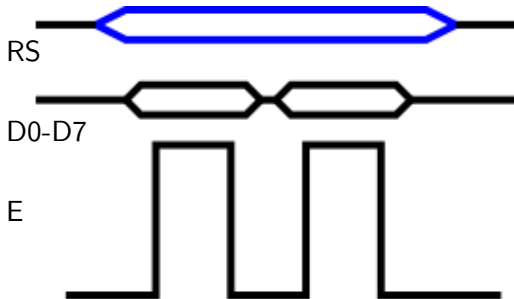
Time required before asserting enable t_{cycle} - (1000ns)



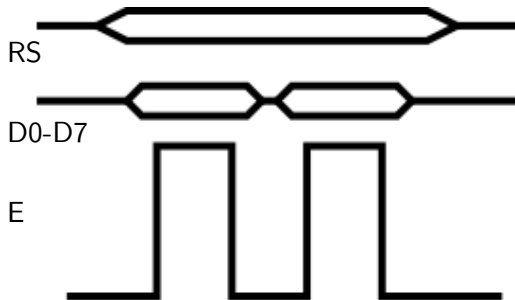
Assert the enable (E). De-assert after appropriate time PW_{EH} (450ns).

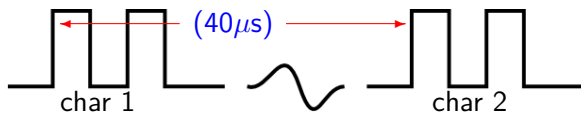


Time required before changing data pins t_H - (10ns)

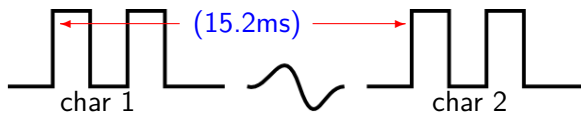


Character complete.





Delay before next character ($40\mu s$).



Clear Display and *Return Home* each require 15.2ms.