Engagement in a Lab Setting

Terry Sturtevant

Wilfrid Laurier University

April 18, 2019

Truth in Advertising

Truth in Advertising

My labs are not all wildly engaging.

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I'm still figuring this out.

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These ideas are from several courses over many years.

Overview of Ideas

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- Projects students enjoy

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- Projects students enjoy
- Student designed experiments

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- Getting students to do your work for you

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I'll show student feedback I've received and discuss pros and cons of projects.

Sample digital project description

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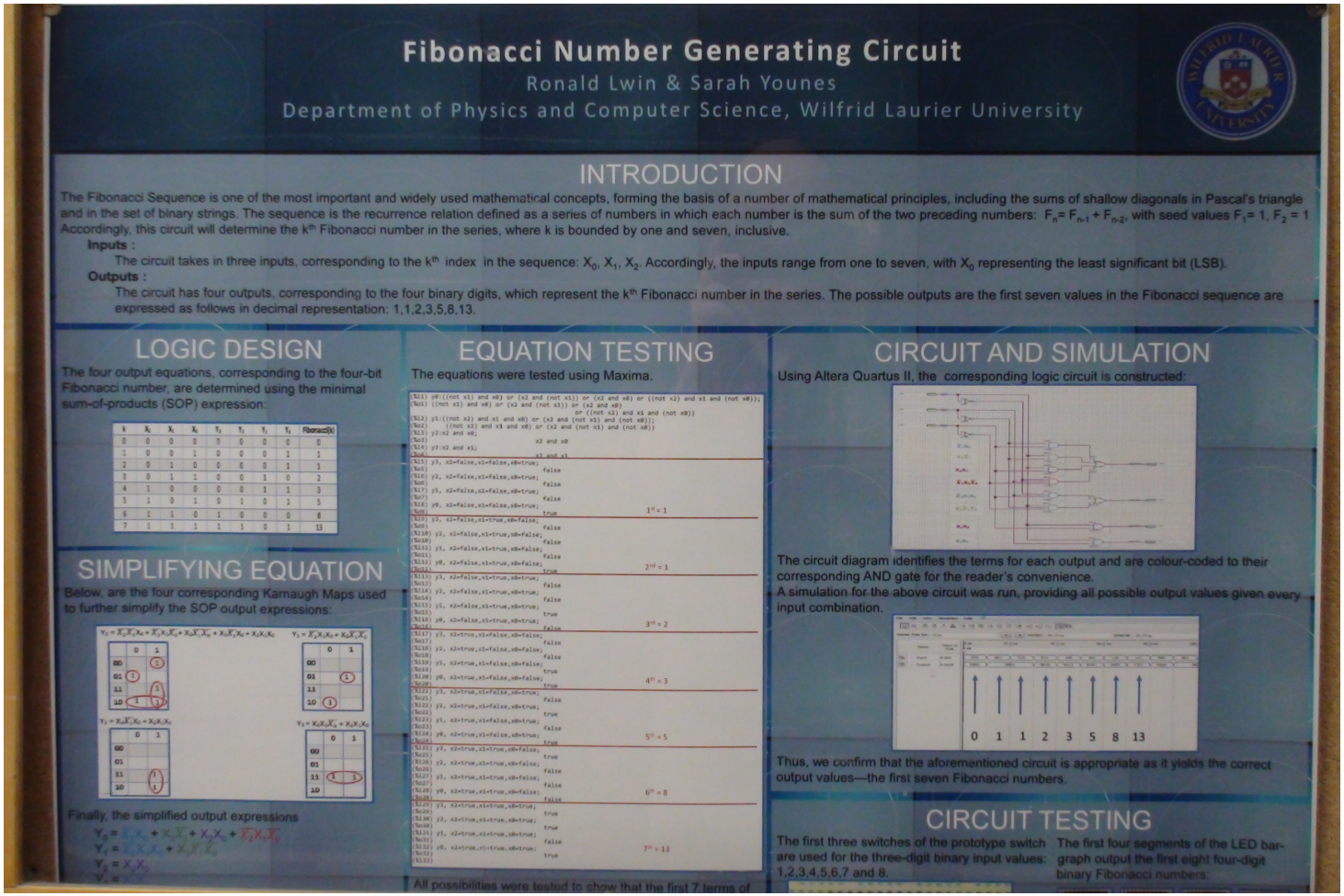
Sample digital project description

Number of prime ministers from each province

4 inputs, to give binary representation of province or territory

?? outputs, indicating how many prime ministers were born in that province or territory

Students must design, simulate, build, test, and present a circuit to do this. Course assignments may cover some of these topics, but not on a *single* example.



Fibonacci Number Generating Circuit

Ronald Lwin & Sarah Younes
Department of Physics and Computer Science, Wilfrid Laurier University

INTRODUCTION

The Fibonacci Sequence is one of the most important and widely used mathematical concepts, forming the basis of a number of mathematical principles, including the sums of shallow diagonals in Pascal's triangle and in the set of binary strings. The sequence is the recurrence relation defined as a series of numbers in which each number is the sum of the two preceding numbers: $F_n = F_{n-1} + F_{n-2}$, with seed values $F_1 = 1$, $F_2 = 1$ Accordingly, this circuit will determine the k^{th} Fibonacci number in the series, where k is bounded by one and seven, inclusive.

Inputs :

The circuit takes in three inputs, corresponding to the k^{th} index in the sequence: X_0, X_1, X_2. Accordingly, the inputs range from one to seven, with X_0 representing the least significant bit (LSB).

Outputs :

The circuit has four outputs, corresponding to the four binary digits, which represent the k^{th} Fibonacci number in the series. The possible outputs are the first seven values in the Fibonacci sequence are expressed as follows in decimal representation: 1,1,2,3,5,8,13.

LOGIC DESIGN

The four output equations, corresponding to the four-bit Fibonacci number, are determined using the minimal sum-of-products (SOP) expression:

k	X_2	X_1	X_0	Y_3	Y_2	Y_1	Y_0	Fibonacci(k)
0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	1
2	0	1	0	0	0	0	1	1
3	0	1	1	0	0	1	0	2
4	1	0	0	0	0	1	1	3
5	1	0	1	0	1	0	1	5
6	1	1	0	1	0	0	0	8
7	1	1	1	1	1	0	1	13

SIMPLIFYING EQUATION

Below, are the four corresponding Karnaugh Maps used to further simplify the SOP output expressions:

Finally, the simplified output expressions

$Y_0 = \overline{X_2}X_0 + X_2\overline{X_0} + X_2X_0 + \overline{X_2}\,\overline{X_0}$

$Y_1 = \overline{X_2}X_1X_0 + X_2\overline{X_1}X_0 + X_2X_1\overline{X_0} + \overline{X_2}\,\overline{X_1}X_0$

$Y_2 = X_2\overline{X_1}\,\overline{X_0} + X_2X_1X_0$

$Y_3 = X_2X_1\overline{X_0} + X_2X_1X_0$

EQUATION TESTING

The equations were tested using Maxima.

```
(%i1) y0:((not x1) and x0) or (x2 and (not x1)) or (x2 and x0) or ((not x2) and x1 and (not x0));
(%o1) ((not x1) and x0) or (x2 and (not x1)) or (x2 and x0)
                                             or ((not x2) and x1 and (not x0))
(%i2) y1:((not x2) and x1 and x0) or (x2 and (not x1) and (not x0));
(%o2)    ((not x2) and x1 and x0) or (x2 and (not x1) and (not x0))
(%i3) y2:x2 and x0;
(%o3)                          x2 and x0
(%i4) y3:x2 and x1;
(%o4)                          x2 and x1
(%i5) y3, x2=false,x1=false,x0=true;
(%o5)                            false
(%i6) y2, x2=false,x1=false,x0=true;
(%o6)                            false
(%i7) y1, x2=false,x1=false,x0=true;
(%o7)                            false
(%i8) y0, x2=false,x1=false,x0=true;
(%o8)                             true                    1st = 1
(%i9) y3, x2=false,x1=true,x0=false;
(%o9)                            false
(%i10) y2, x2=false,x1=true,x0=false;
(%o10)                           false
(%i11) y1, x2=false,x1=true,x0=false;
(%o11)                           false
(%i12) y0, x2=false,x1=true,x0=false;
(%o12)                            true                   2nd = 1
(%i13) y3, x2=false,x1=true,x0=true;
(%o13)                           false
(%i14) y2, x2=false,x1=true,x0=true;
(%o14)                           false
(%i15) y1, x2=false,x1=true,x0=true;
(%o15)                            true
(%i16) y0, x2=false,x1=true,x0=true;
(%o16)                           false                   3rd = 2
(%i17) y3, x2=true,x1=false,x0=false;
(%o17)                           false
(%i18) y2, x2=true,x1=false,x0=false;
(%o18)                           false
(%i19) y1, x2=true,x1=false,x0=false;
(%o19)                            true
(%i20) y0, x2=true,x1=false,x0=false;
(%o20)                            true                   4th = 3
(%i21) y3, x2=true,x1=false,x0=true;
(%o21)                           false
(%i22) y2, x2=true,x1=false,x0=true;
(%o22)                            true
(%i23) y1, x2=true,x1=false,x0=true;
(%o23)                           false
(%i24) y0, x2=true,x1=false,x0=true;
(%o24)                            true                   5th = 5
(%i25) y3, x2=true,x1=true,x0=false;
(%o25)                            true
(%i26) y2, x2=true,x1=true,x0=false;
(%o26)                           false
(%i27) y1, x2=true,x1=true,x0=false;
(%o27)                           false
(%i28) y0, x2=true,x1=true,x0=false;
(%o28)                           false                   6th = 8
(%i29) y3, x2=true,x1=true,x0=true;
(%o29)                            true
(%i30) y2, x2=true,x1=true,x0=true;
(%o30)                            true
(%i31) y1, x2=true,x1=true,x0=true;
(%o31)                           false
(%i32) y0, x2=true,x1=true,x0=true;
(%o32)                            true                   7th = 13
(%i33)
```

All possibilities were tested to show that the first 7 terms of

CIRCUIT AND SIMULATION

Using Altera Quartus II, the corresponding logic circuit is constructed:

The circuit diagram identifies the terms for each output and are colour-coded to their corresponding AND gate for the reader's convenience.
A simulation for the above circuit was run, providing all possible output values given every input combination.

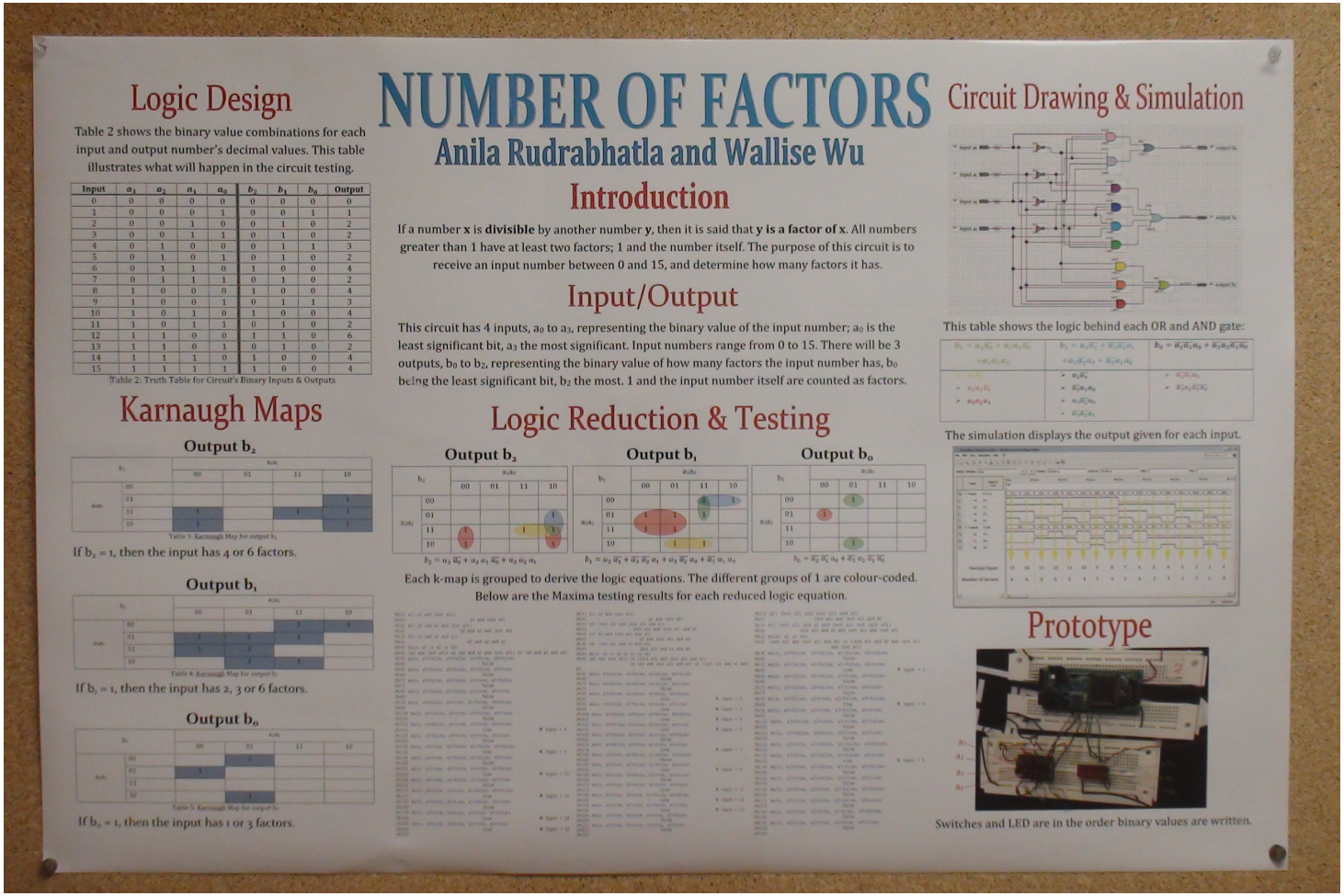
Thus, we confirm that the aforementioned circuit is appropriate as it yields the correct output values—the first seven Fibonacci numbers.

CIRCUIT TESTING

The first three switches of the prototype switch are used for the three-digit binary input values: 1,2,3,4,5,6,7 and 8.

The first four segments of the LED bar-graph output the first eight four-digit binary Fibonacci numbers:

Digital project; sample poster



NUMBER OF FACTORS

Anila Rudrabhatla and Wallise Wu

Introduction

If a number **x** is **divisible** by another number **y**, then it is said that **y is a factor of x**. All numbers greater than 1 have at least two factors; 1 and the number itself. The purpose of this circuit is to receive an input number between 0 and 15, and determine how many factors it has.

Input/Output

This circuit has 4 inputs, a_0 to a_3, representing the binary value of the input number; a_0 is the least significant bit, a_3 the most significant. Input numbers range from 0 to 15. There will be 3 outputs, b_0 to b_2, representing the binary value of how many factors the input number has, b_0 being the least significant bit, b_2 the most. 1 and the input number itself are counted as factors.

Logic Design

Table 2 shows the binary value combinations for each input and output number's decimal values. This table illustrates what will happen in the circuit testing.

Input	a_3	a_2	a_1	a_0	b_2	b_1	b_0	Output
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1	1
2	0	0	1	0	0	1	0	2
3	0	0	1	1	0	1	0	2
4	0	1	0	0	0	1	1	3
5	0	1	0	1	0	1	0	2
6	0	1	1	0	1	0	0	4
7	0	1	1	1	0	1	0	2
8	1	0	0	0	1	0	0	4
9	1	0	0	1	0	1	1	3
10	1	0	1	0	1	0	0	4
11	1	0	1	1	0	1	0	2
12	1	1	0	0	1	1	0	6
13	1	1	0	1	0	1	0	2
14	1	1	1	0	1	0	0	4
15	1	1	1	1	1	0	0	4

Table 2: Truth Table for Circuit's Binary Inputs & Outputs

Karnaugh Maps

Output b_2

Table 3: Karnaugh Map for output b_2

If $b_2 = 1$, then the input has 4 or 6 factors.

Output b_1

Table 4: Karnaugh Map for output b_1

If $b_1 = 1$, then the input has 2, 3 or 6 factors.

Output b_0

Table 5: Karnaugh Map for output b_0

If $b_0 = 1$, then the input has 1 or 3 factors.

Logic Reduction & Testing

Output b_2 | **Output b_1** | **Output b_0**

$b_2 = a_3\overline{a_2} + a_2 a_1 \overline{a_0} + a_3 a_2 a_1$

$b_1 = a_2\overline{a_1} + \overline{a_3}\,\overline{a_2} a_1 + a_3\,\overline{a_2}\,a_0 + \overline{a_3} a_1 a_0$

$b_0 = \overline{a_2}\,\overline{a_1}\,a_0 + \overline{a_3} a_2 \overline{a_1}\,\overline{a_0}$

Each k-map is grouped to derive the logic equations. The different groups of 1 are colour-coded. Below are the Maxima testing results for each reduced logic equation.

Circuit Drawing & Simulation

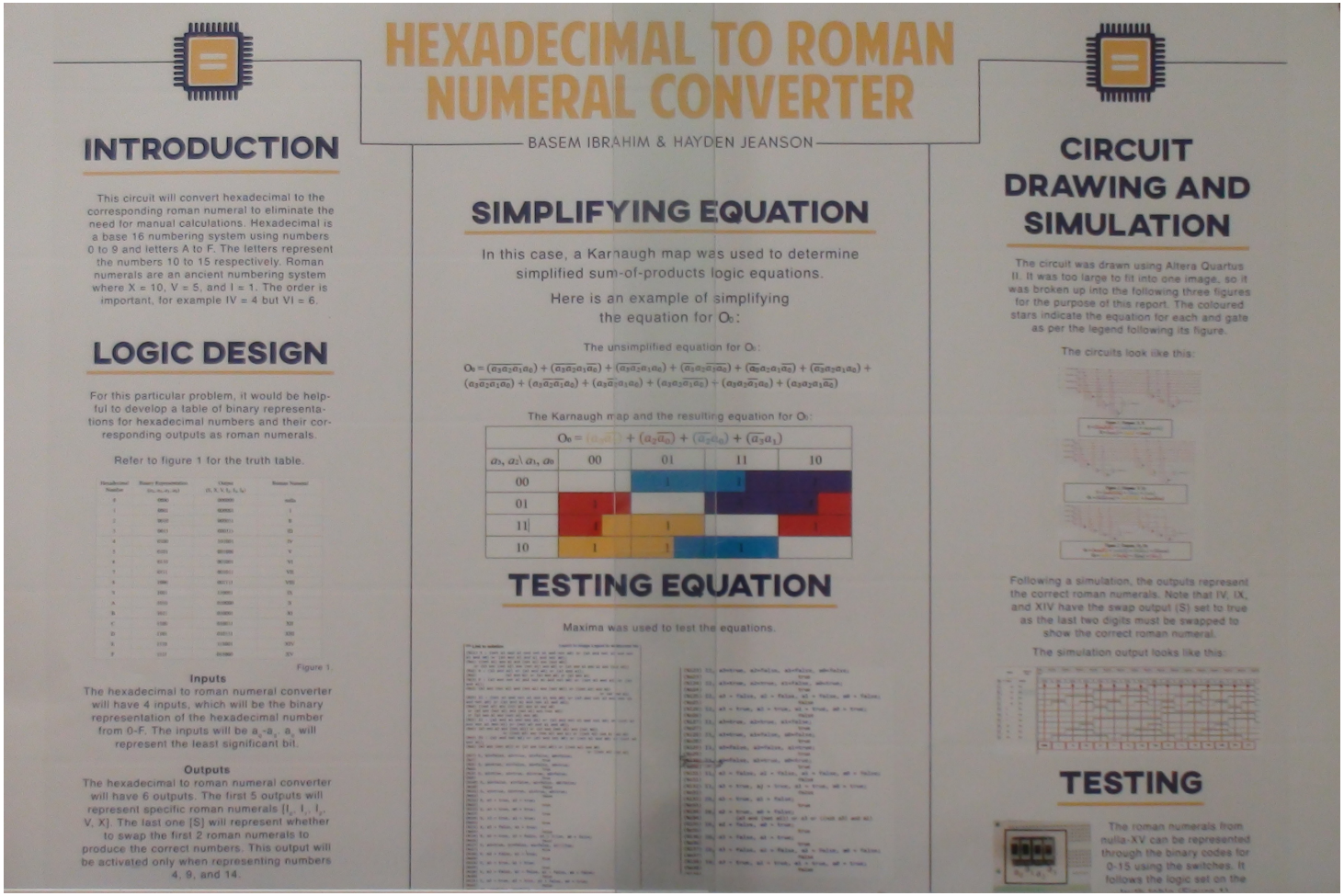
This table shows the logic behind each OR and AND gate:

The simulation displays the output given for each input.

Prototype

Switches and LED are in the order binary values are written.

Digital project; sample poster



HEXADECIMAL TO ROMAN NUMERAL CONVERTER

BASEM IBRAHIM & HAYDEN JEANSON

INTRODUCTION

This circuit will convert hexadecimal to the corresponding roman numeral to eliminate the need for manual calculations. Hexadecimal is a base 16 numbering system using numbers 0 to 9 and letters A to F. The letters represent the numbers 10 to 15 respectively. Roman numerals are an ancient numbering system where X = 10, V = 5, and I = 1. The order is important, for example IV = 4 but VI = 6.

LOGIC DESIGN

For this particular problem, it would be helpful to develop a table of binary representations for hexadecimal numbers and their corresponding outputs as roman numerals.

Refer to figure 1 for the truth table.

Figure 1.

Inputs

The hexadecimal to roman numeral converter will have 4 inputs, which will be the binary representation of the hexadecimal number from 0-F. The inputs will be a_3-a_0. a_0 will represent the least significant bit.

Outputs

The hexadecimal to roman numeral converter will have 6 outputs. The first 5 outputs will represent specific roman numerals [I_1, I_2, I_3, V, X]. The last one [S] will represent whether to swap the first 2 roman numerals to produce the correct numbers. This output will be activated only when representing numbers 4, 9, and 14.

SIMPLIFYING EQUATION

In this case, a Karnaugh map was used to determine simplified sum-of-products logic equations.

Here is an example of simplifying the equation for O_6:

The unsimplified equation for O_6:

$$O_6 = (\overline{a_3}a_2\overline{a_1}a_0) + (a_3\overline{a_2}a_1\overline{a_0}) + (\overline{a_3}a_2\overline{a_1}a_0) + (\overline{a_3}a_2a_1\overline{a_0}) + (a_3a_2\overline{a_1}\overline{a_0}) + (\overline{a_3}a_2a_1a_0) + (a_3\overline{a_2}\overline{a_1}a_0) + (a_3\overline{a_2}a_1a_0) + (a_3a_2\overline{a_1}a_0) + (a_3a_2a_1\overline{a_0})$$

The Karnaugh map and the resulting equation for O_6:

$O_6 = (a_3\overline{a_2}) + (a_2\overline{a_0}) + (\overline{a_2}a_0) + (\overline{a_3}a_1)$

$a_3, a_2 \backslash a_1, a_0$	00	01	11	10
00		1	1	
01	1			1
11	1	1		1
10	1	1	1	

TESTING EQUATION

Maxima was used to test the equations.

CIRCUIT DRAWING AND SIMULATION

The circuit was drawn using Altera Quartus II. It was too large to fit into one image, so it was broken up into the following three figures for the purpose of this report. The coloured stars indicate the equation for each and gate as per the legend following its figure.

The circuits look like this:

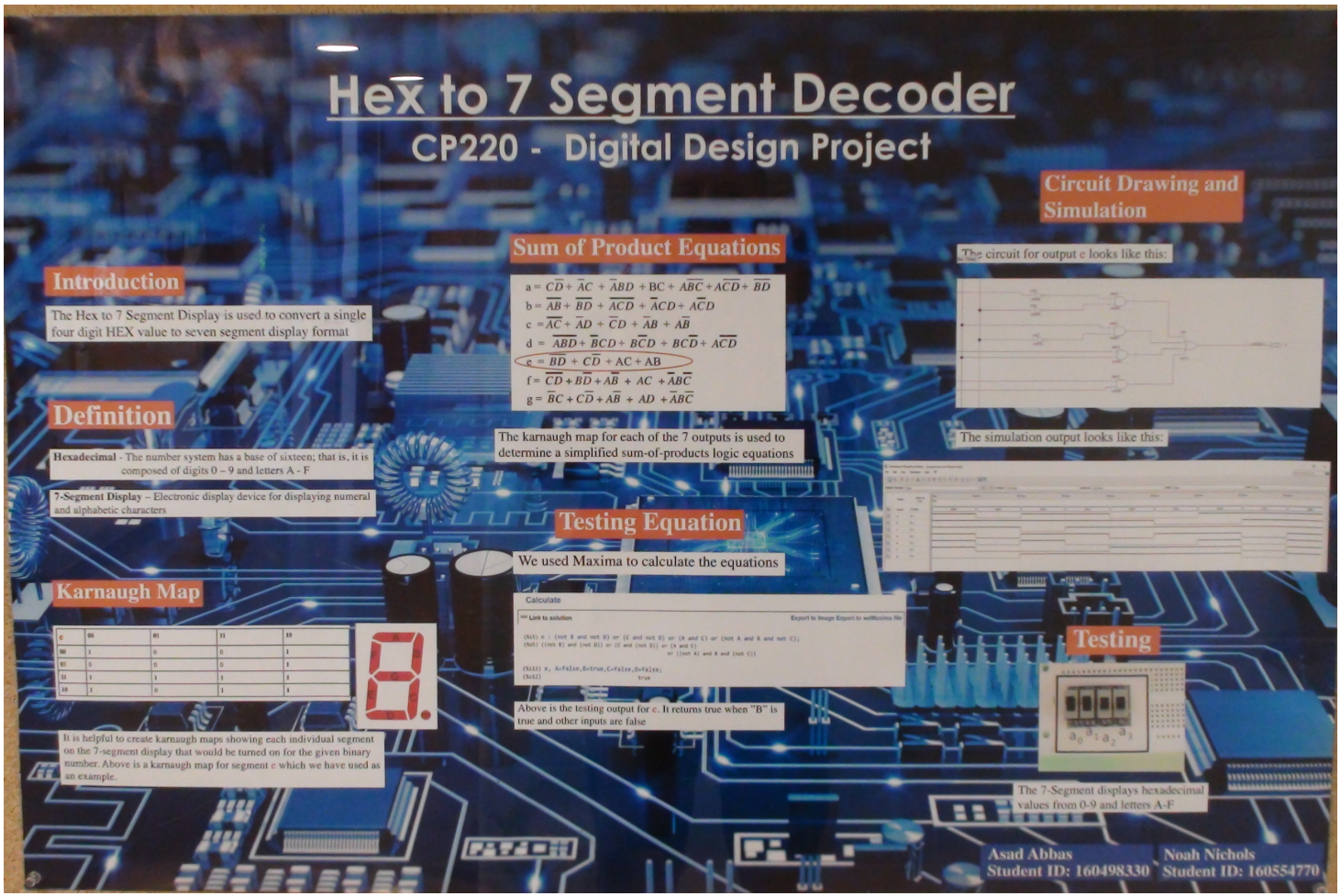
Following a simulation, the outputs represent the correct roman numerals. Note that IV, IX, and XIV have the swap output (S) set to true as the last two digits must be swapped to show the correct roman numeral.

The simulation output looks like this:

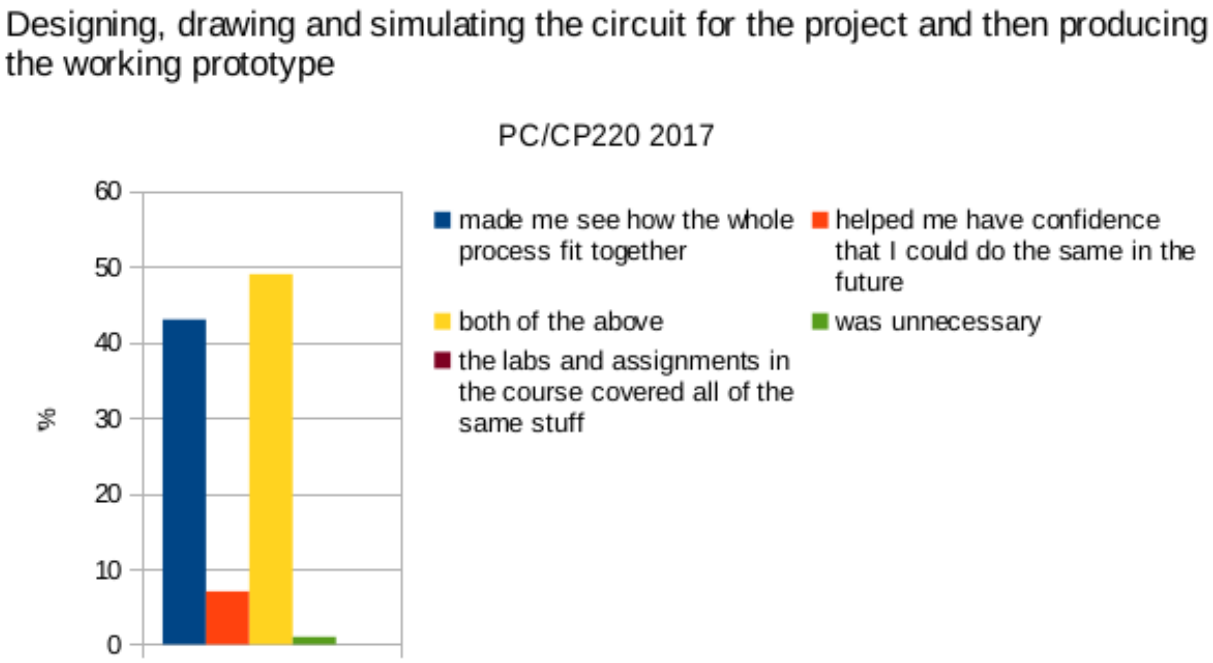
TESTING

The roman numerals from nulla-XV can be represented through the binary codes for 0-15 using the switches. It follows the logic set on the

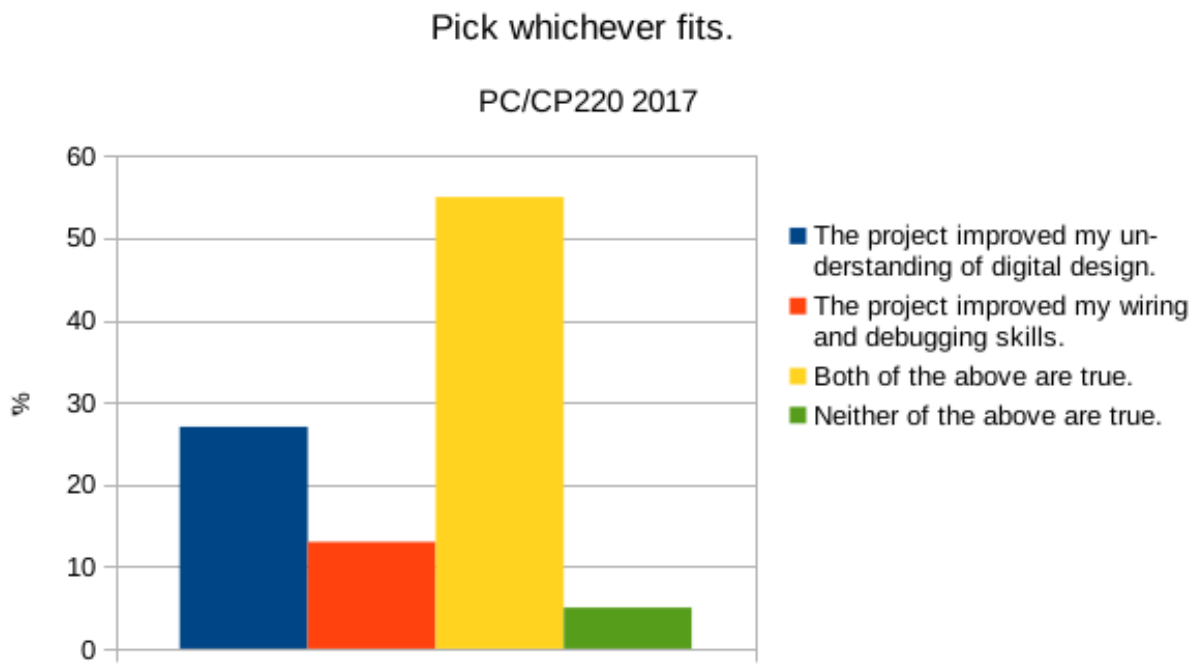
Digital project; sample poster



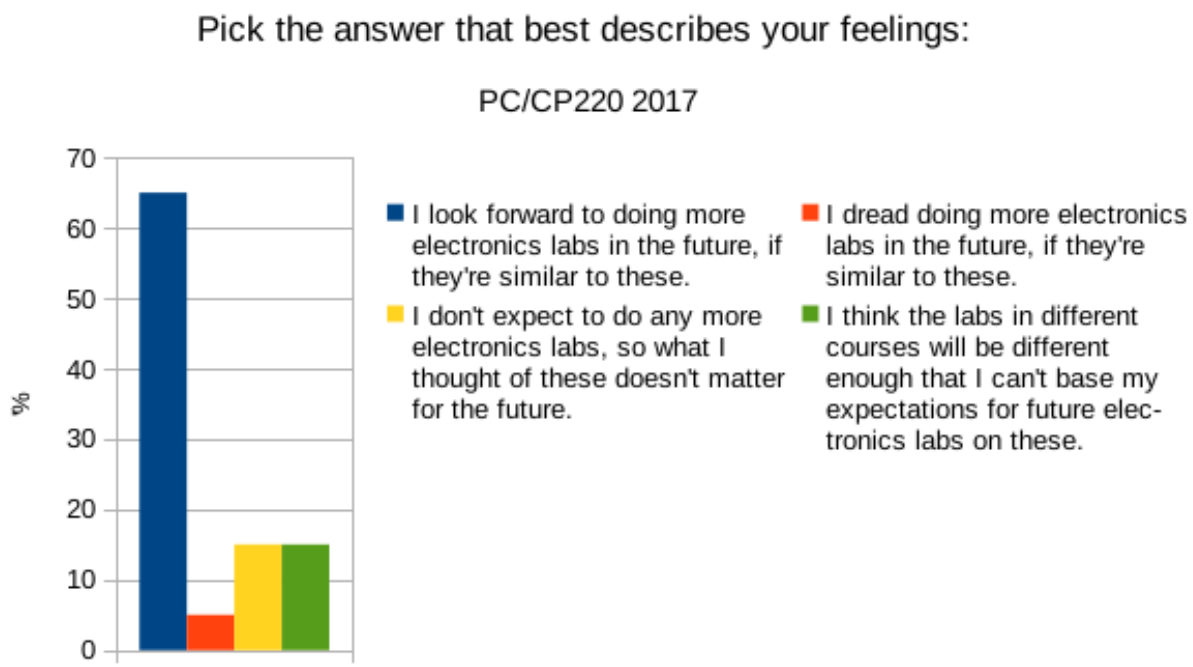
Digital project; sample poster



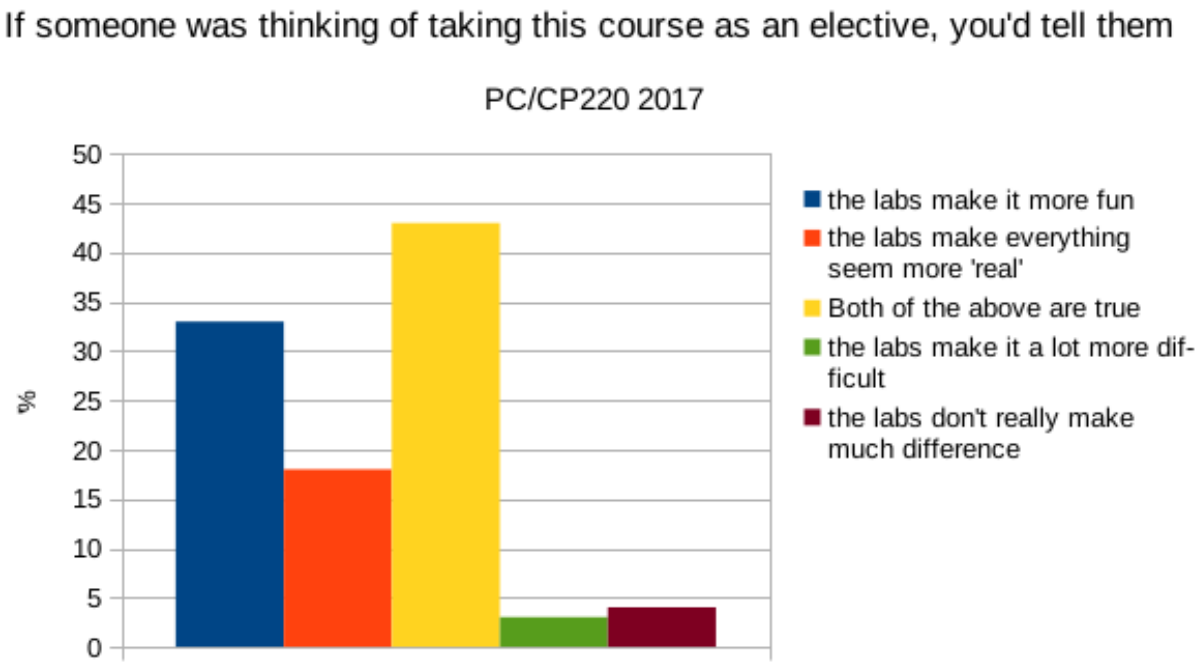
Digital project 2017; value of integration



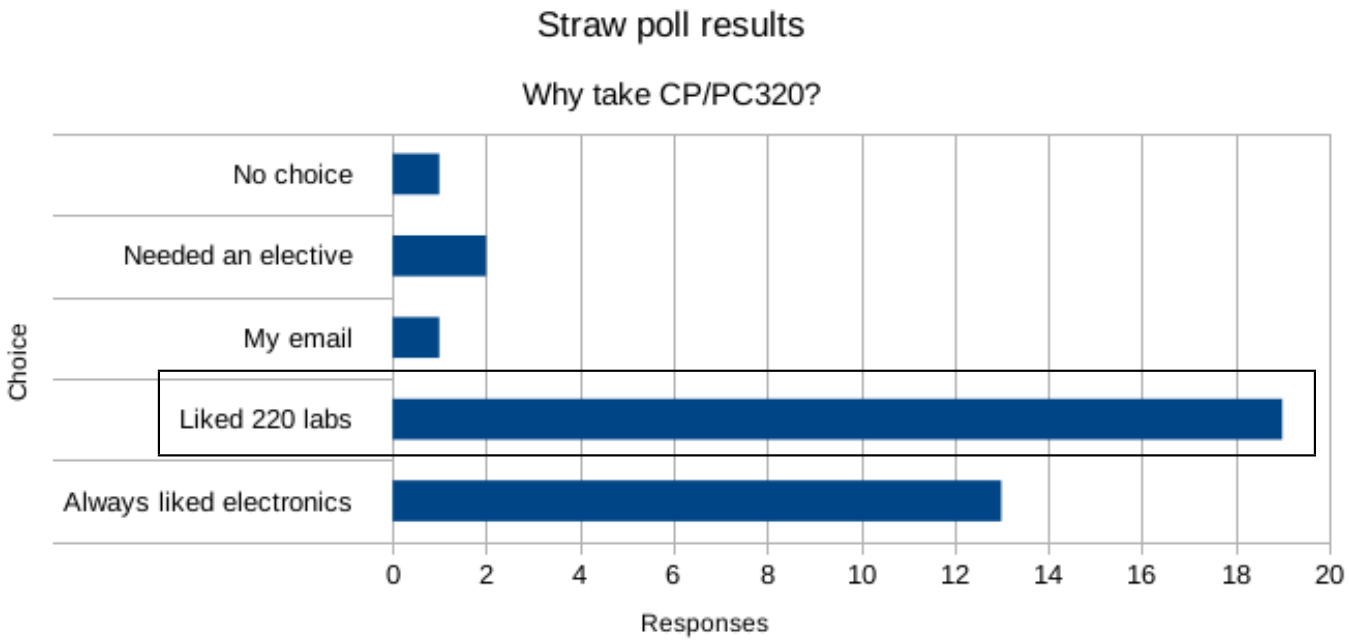
Digital project 2017; value of knowledge and skills



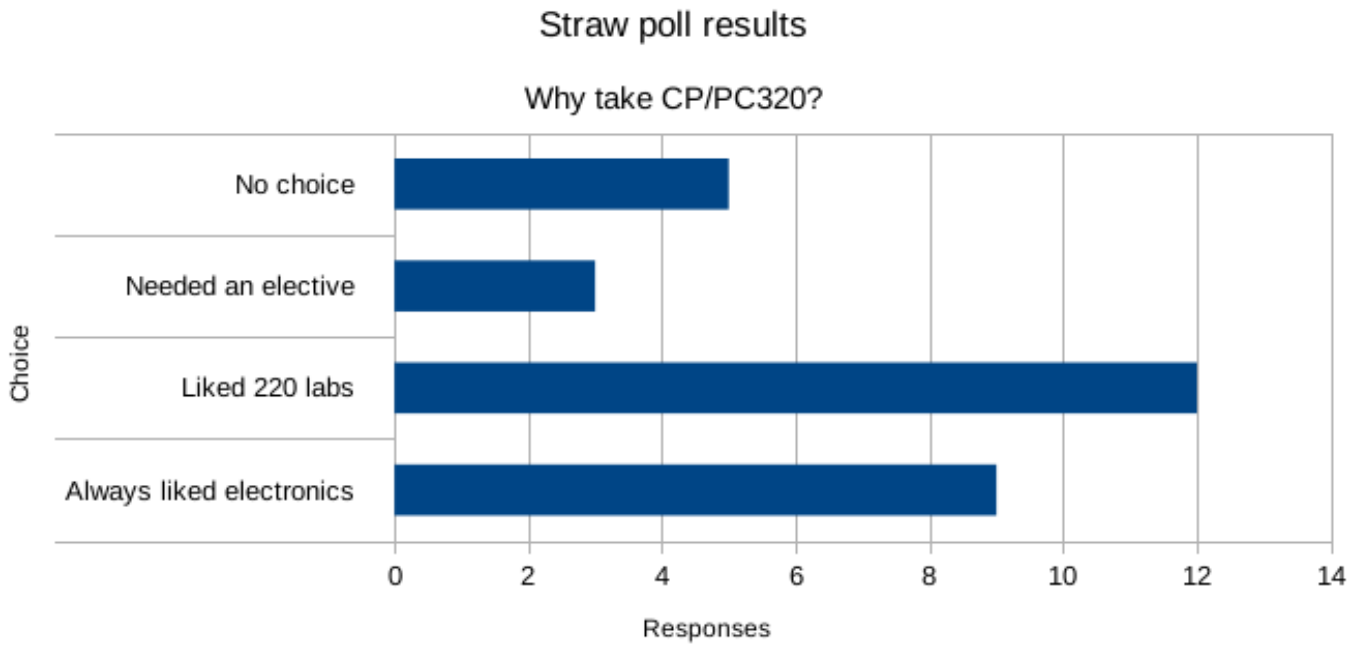
Digital project 2017; impression of labs



Digital project 2017; advice to others



Fall 2017; note the effectiveness of my personal invitation


Straw poll results
Why take CP/PC320?
No choice
Needed an elective
Liked 220 labs
Always liked electronics
Choice
0
2
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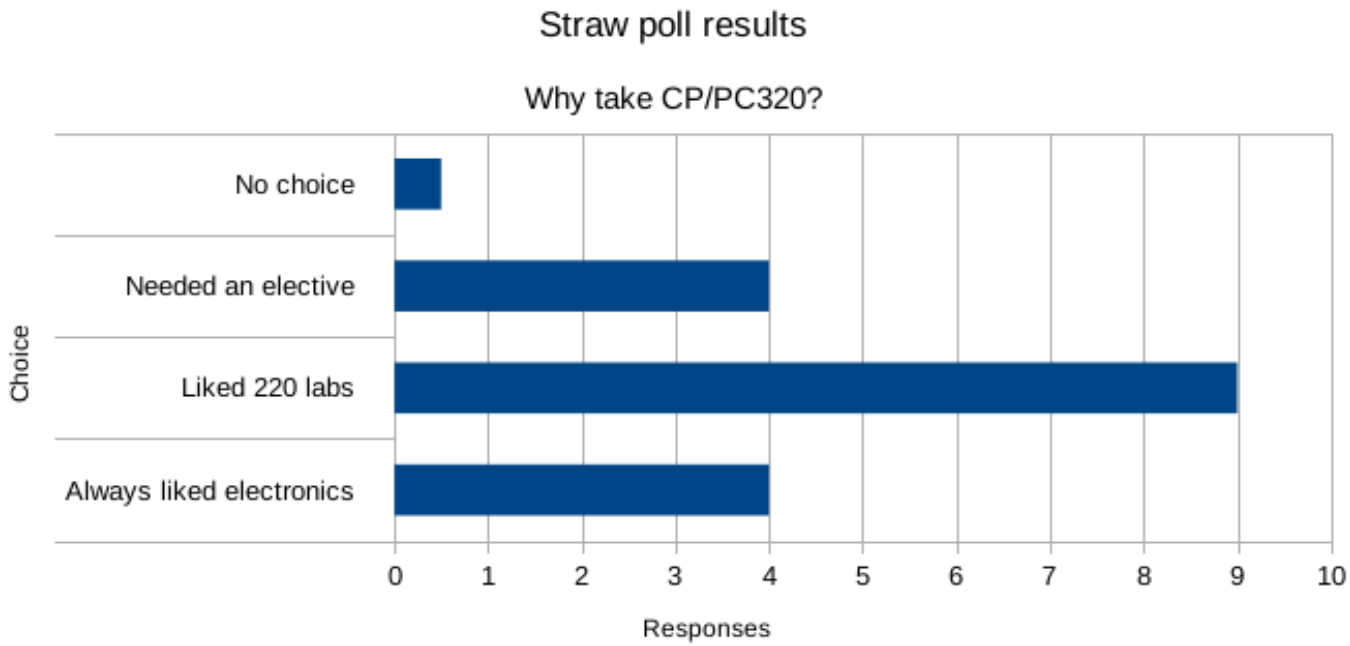
10
12
14
Responses

Fall 2018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Responses

Winter 2019

Student designed experiments

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Second week they find equipment, set it up, and determine how they will measure.

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Repeat for another phenomenon.

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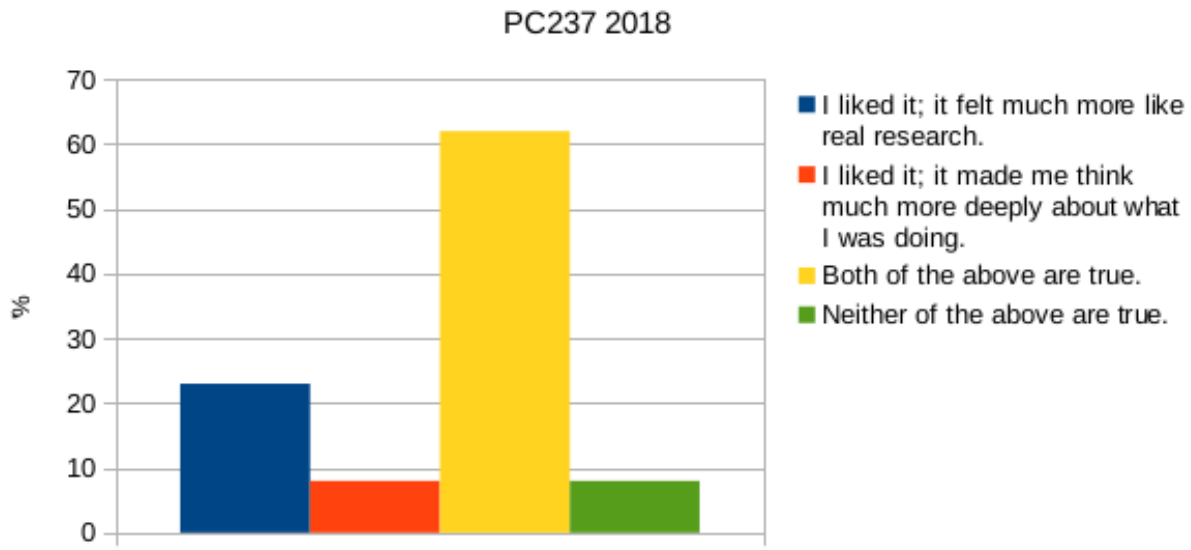
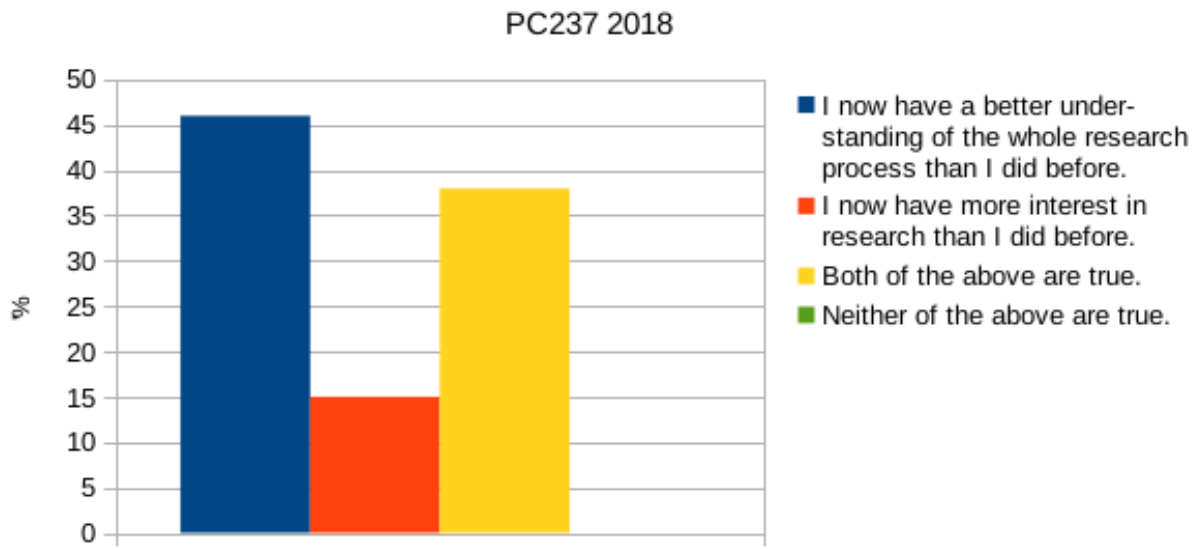
This last step is rare in labs.

What did you think about having to design experiments yourself rather than following given instructions?

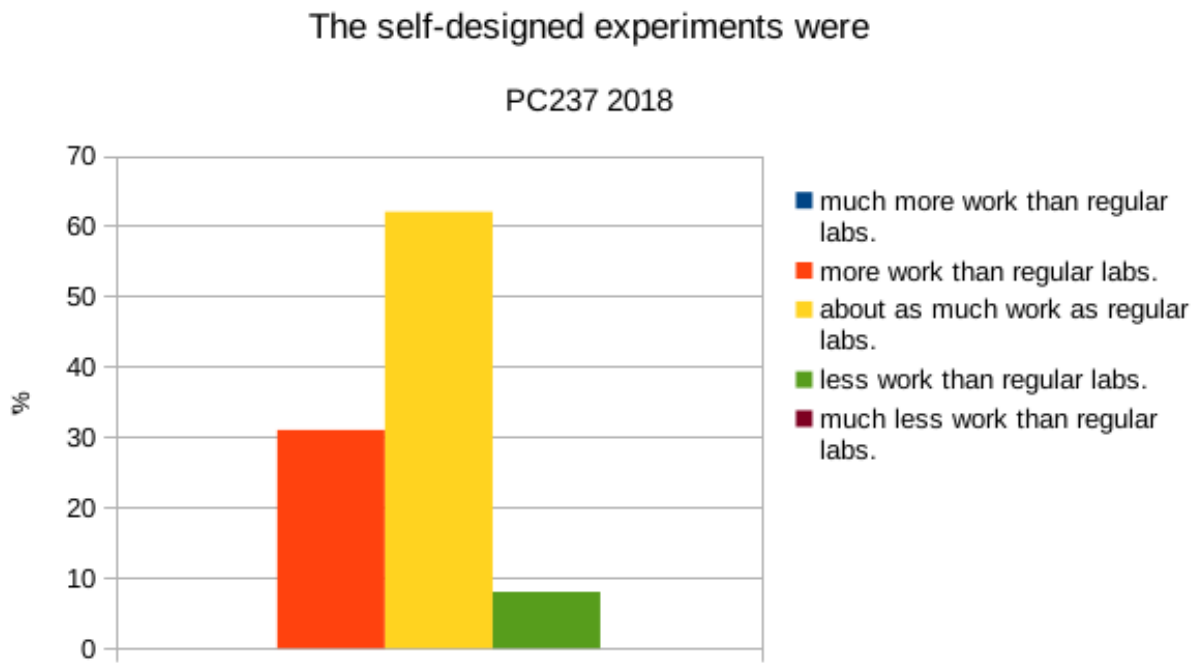


Self-designed experiments 2018

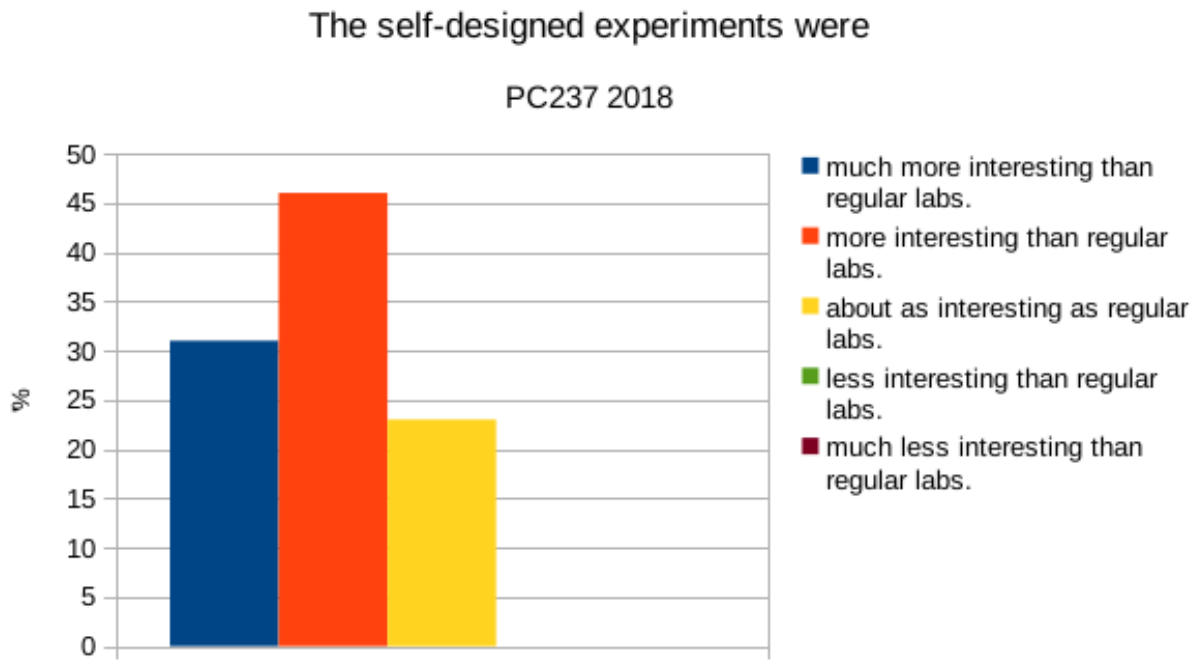
Pick whichever fits in describing your experience with the self-designed experiments.



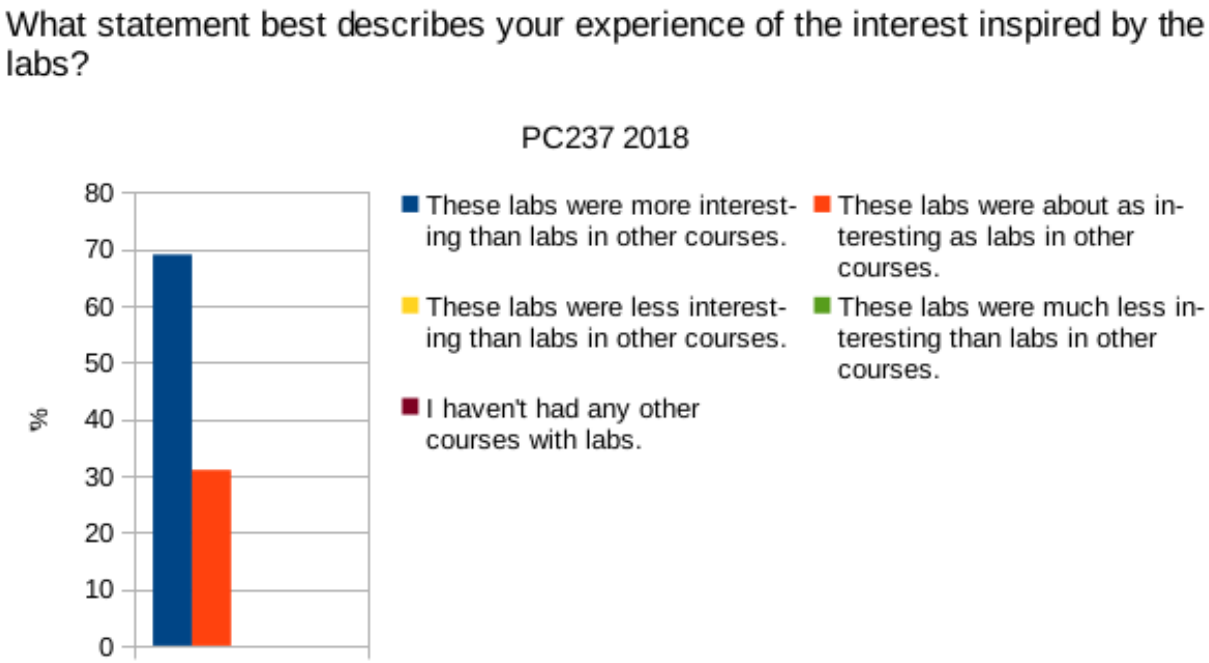
Self-designed experiments 2018



Self-designed experiments 2018



Self-designed experiments 2018



Self-designed experiments 2018

Getting students to do your work for you

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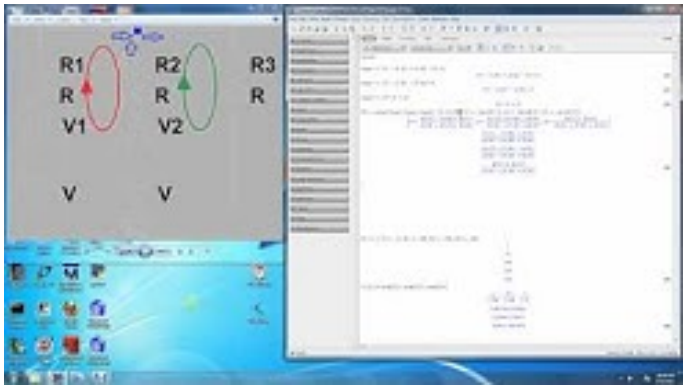
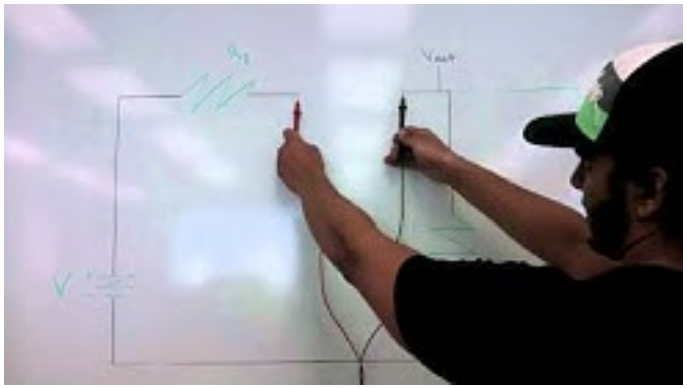
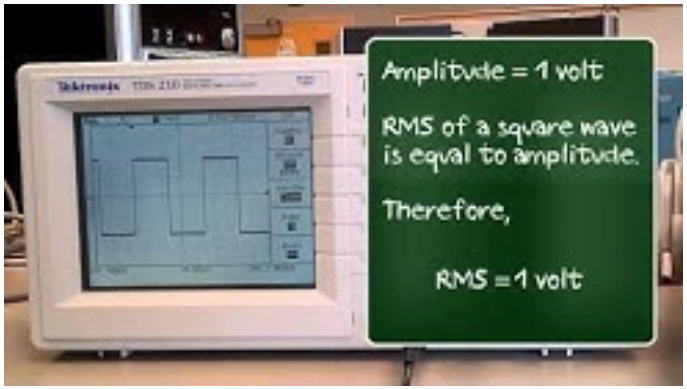
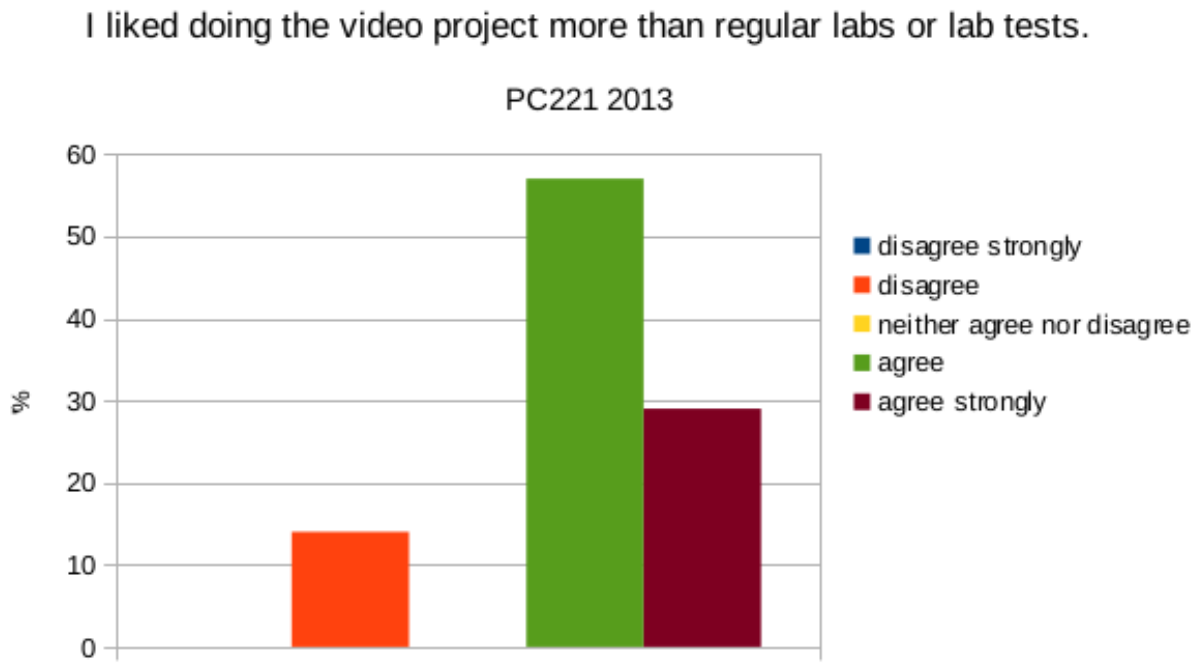
This is a great chance for peer feedback.



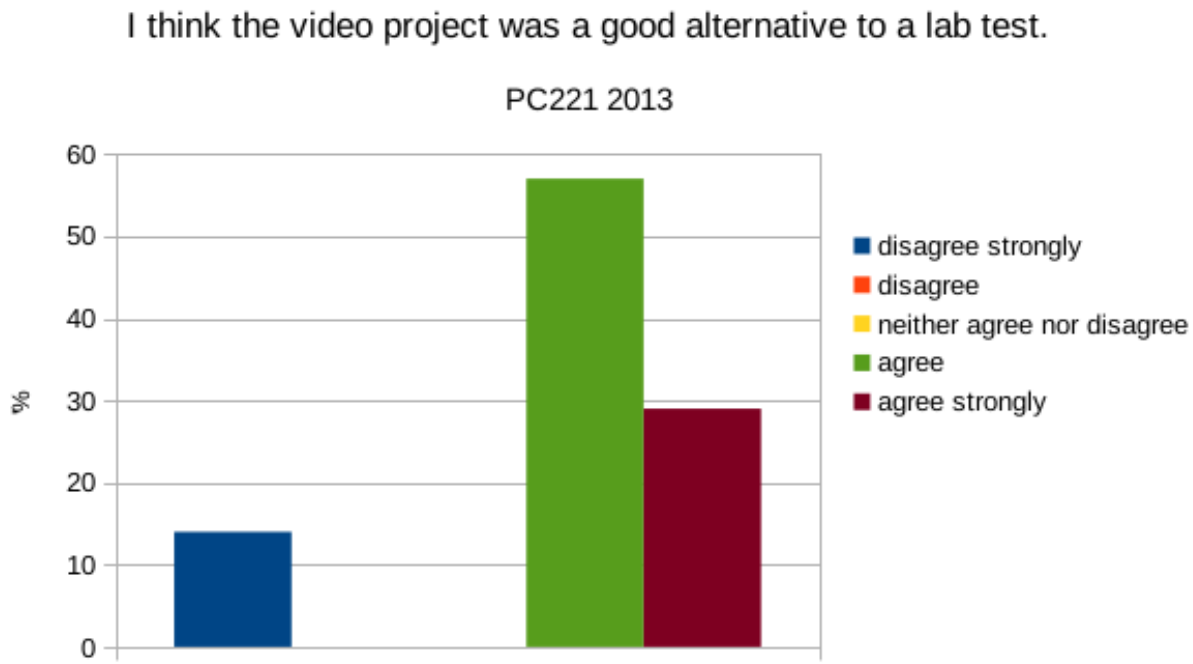




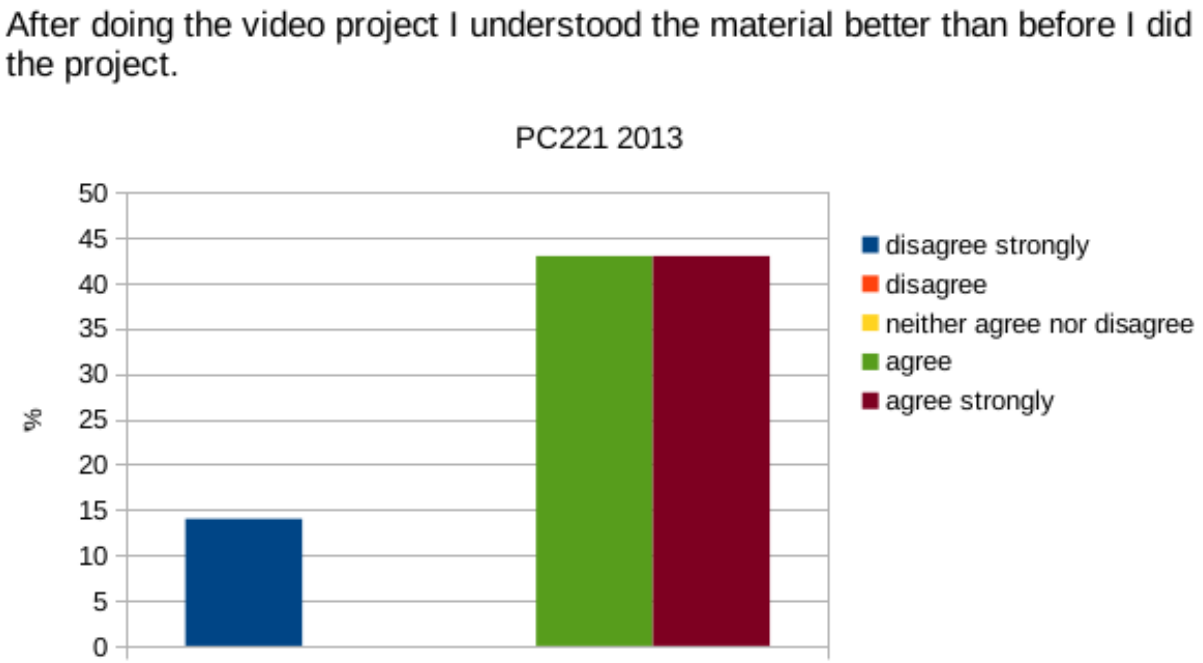
Video project; sample thumbnails



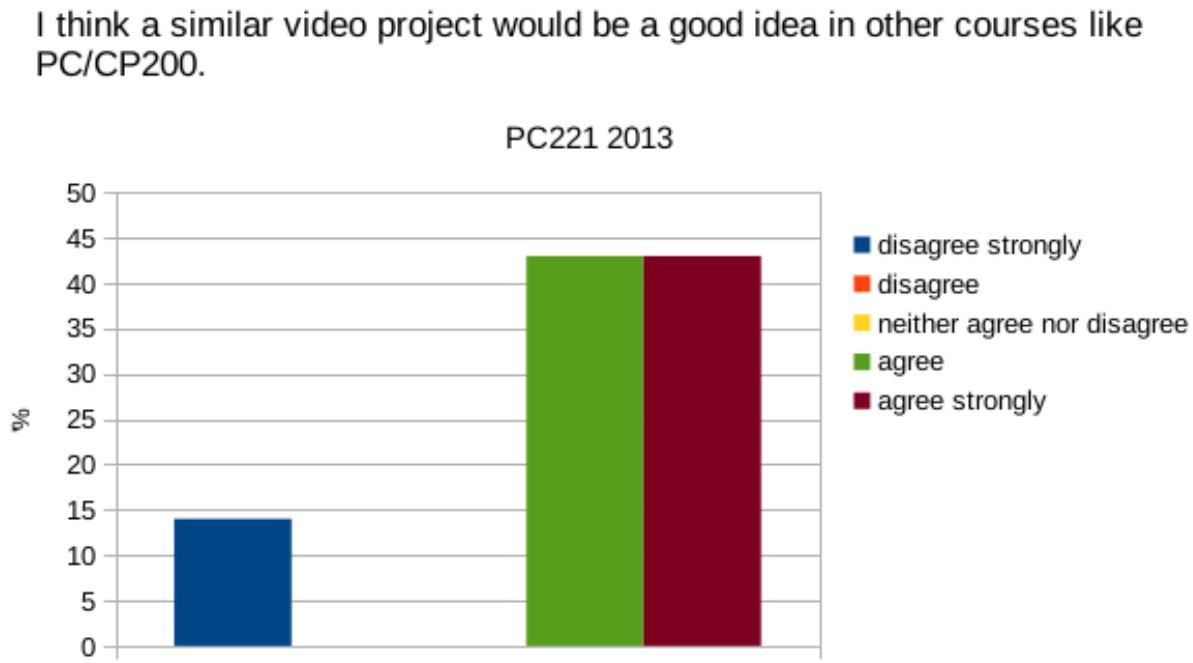
Video project 2013



Video project 2013



Video project 2013



Video project 2013

Video	Views
Choosing resistor values for LEDs	83,408 10.7%
Determining Capacitor Polarity	89,574 11.5%
Adding a model in LTspice	58,119 7.5%
DC sweeps in LTspice	28,358 3.6%
Using the Stimulus Feature in MPLABX	16,410 2.1%
How to produce pdf with LaTeX	73,841 9.5%
Quartus II CPLD Programming	19,668 2.5%
Quartus II Preparing to Simulate using ModelSim - After ...	12,916 1.7%
Resistance, Capacitance, and Inductance Measurement...	15,790 2.0%
AC analysis in LTspice	16,365 2.1%
Uncertainty Calculations - Division	15,881 2.0%
DC and AC measurements with an oscilloscope	15,395 2.0%
Transient analysis in LTspice	19,674 2.5%
Exporting LTspice Data	12,996 1.7%
Operating point analysis in LTspice - Part I	17,520 2.3%
Quartus II Introduction - Drawing and Compiling Circuits	8,507 1.1%
XY graph with X error bars and Y error bars in LibreOffice (...	16,133 2.1%
Uncertainty Calculations - Multiplication	9,790 1.3%
DC and AC measurements with an oscilloscope (prelimin...	18,066 2.3%
DC and AC voltage measurements with a digital multimet...	14,052 1.8%

YouTube views; over 250000 views (as of March 2019)

Peer marking to highlight expectations

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It can be done during a project for feedback or at the end.

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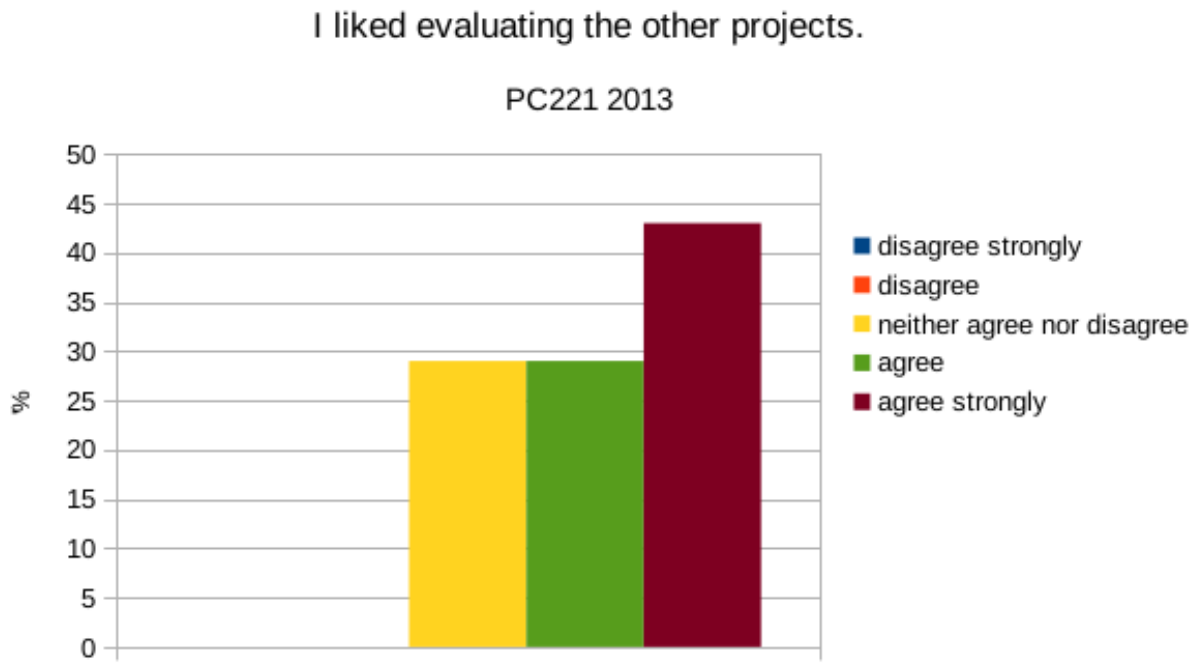
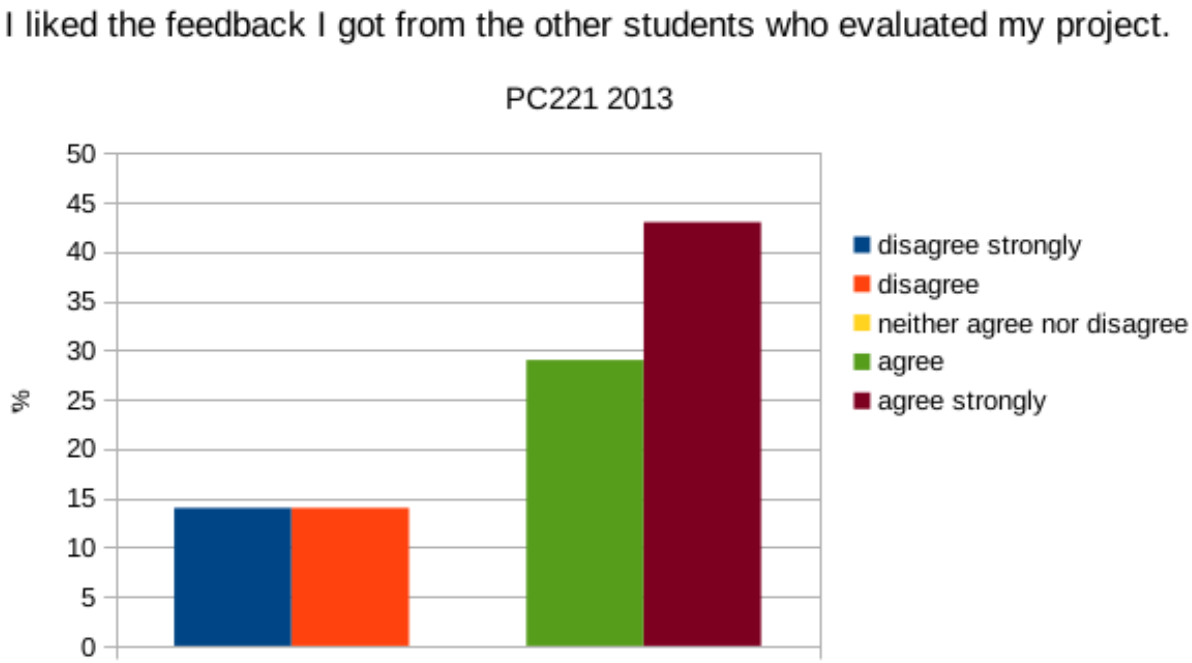
All projects are different, so seeing others' work doesn't directly allow copying.



Video project 2013



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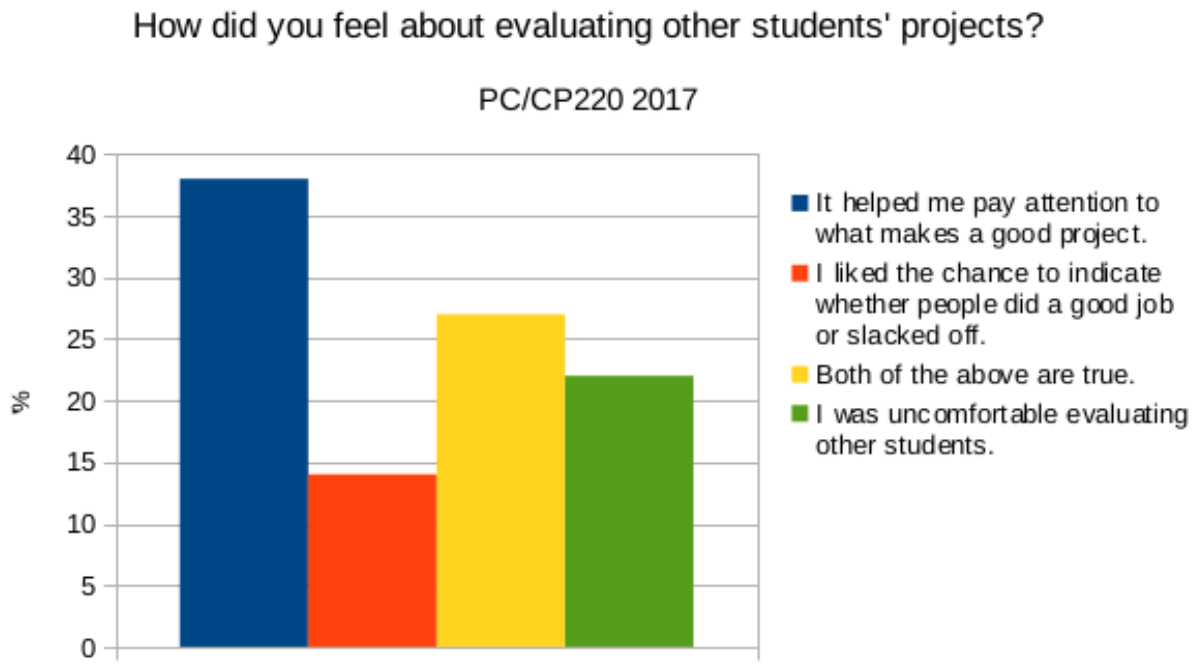
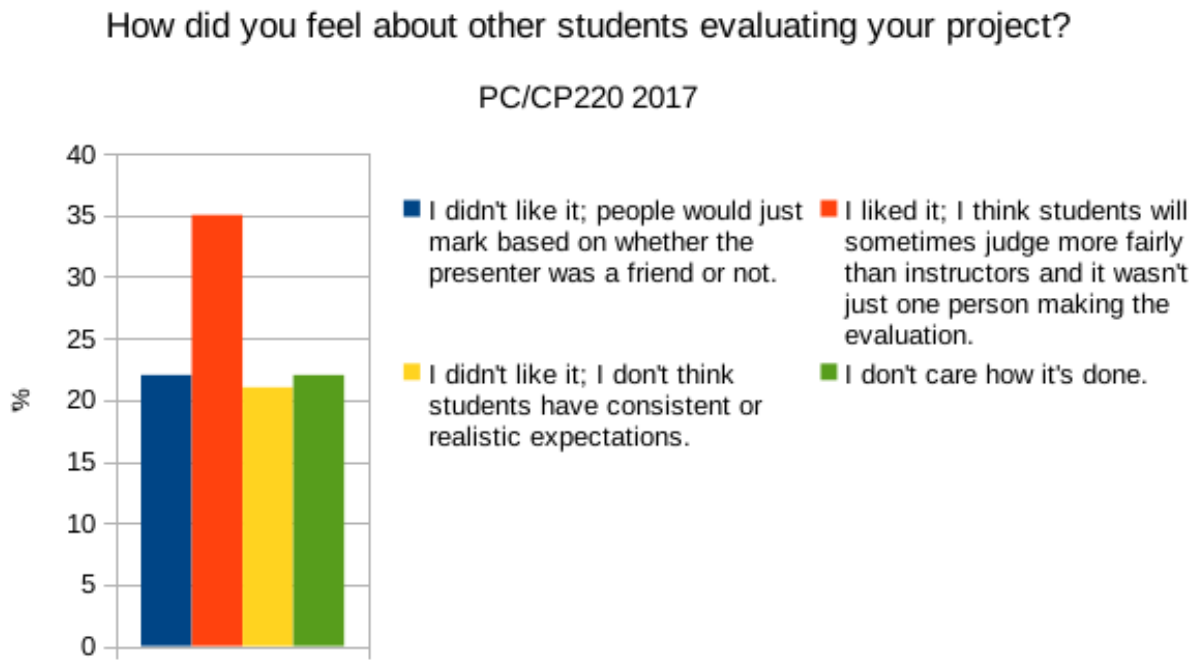


Digital project 2017; marking others



Digital project 2017; being marked by others

Pros and cons of projects

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This precludes labs on the most advanced material.

They cover less material, but in greater depth.

Pros and cons of projects (continued)

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Project constraints limit scope.

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The strongest students could handle "wide open" projects.

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The weakest students couldn't handle "wide open" projects.

Pros and cons of projects (continued)

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Getting the constraints right takes iteration.

Final thoughts

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Projects that are engaging are better than projects that are "well-intentioned".

General project principles

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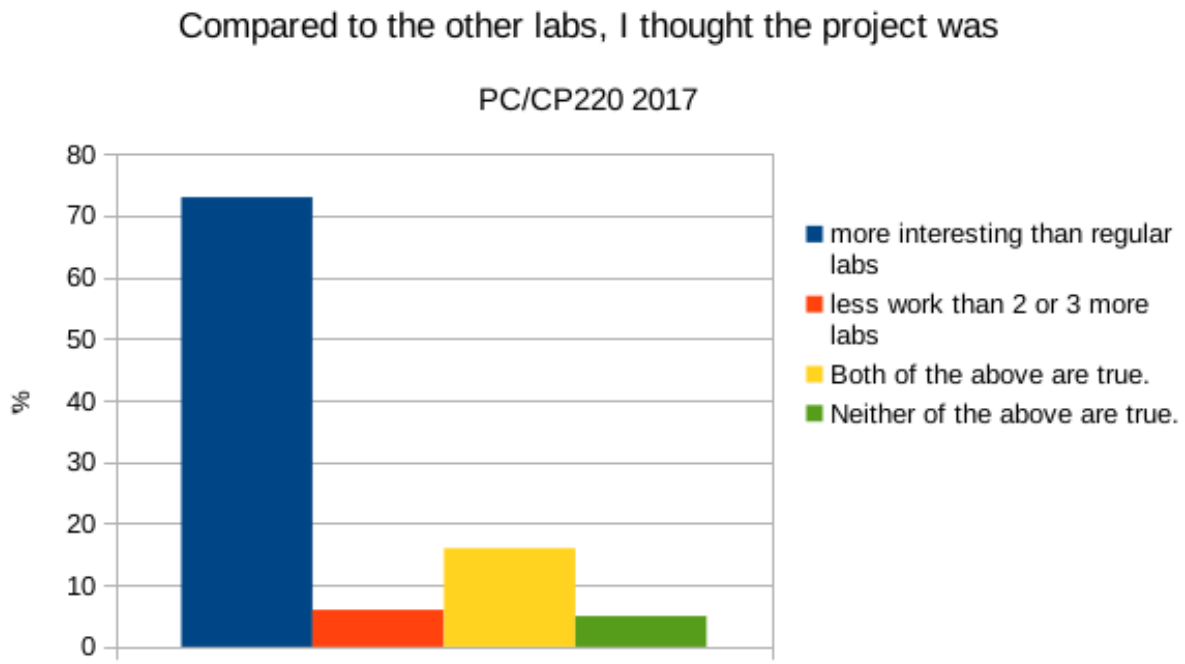
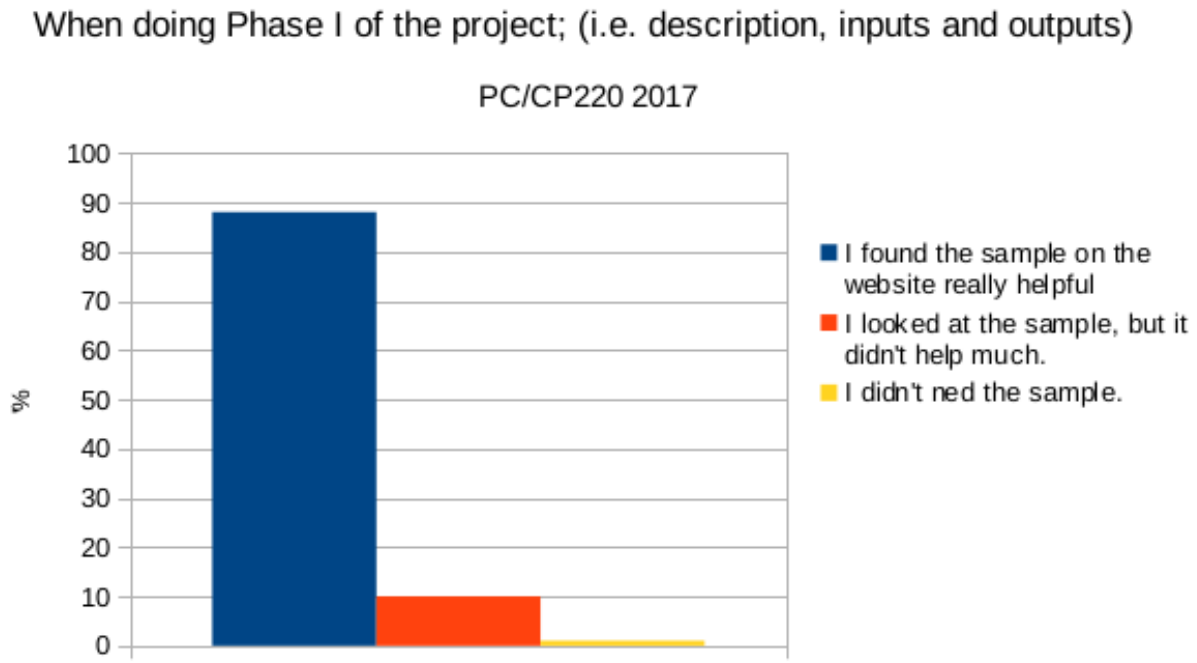
Phase III is due in week 10. Work starts in lab during week 9.

Phase IV takes last 3 weeks of lab time.

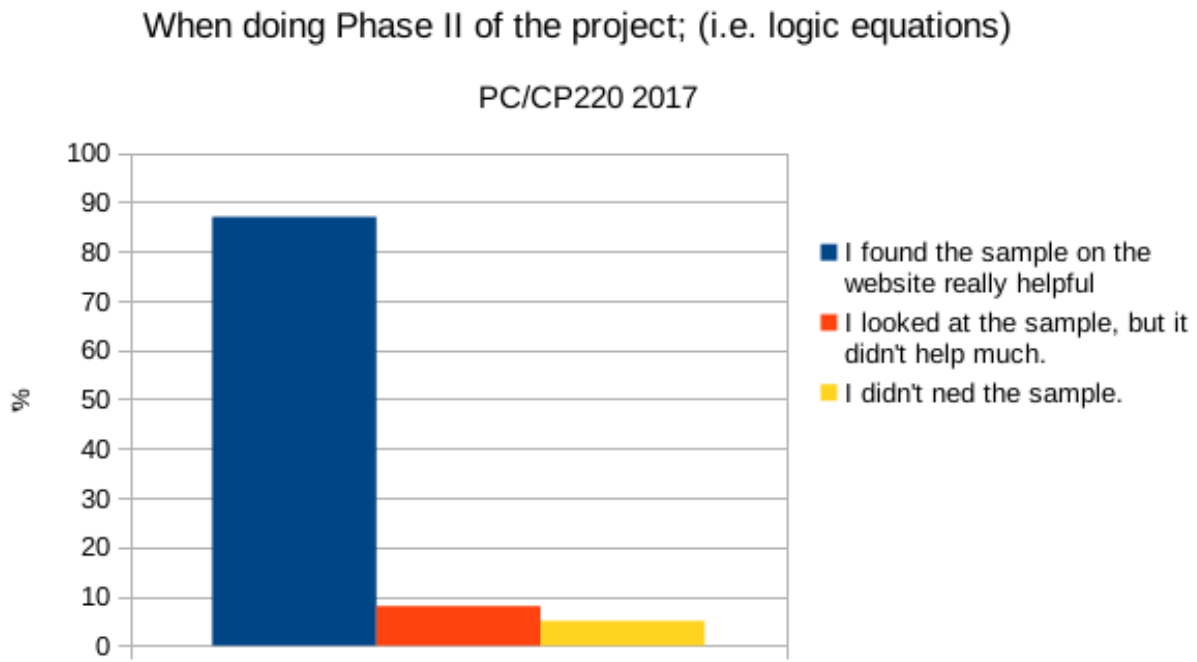
Final presentation is during the last lab period.



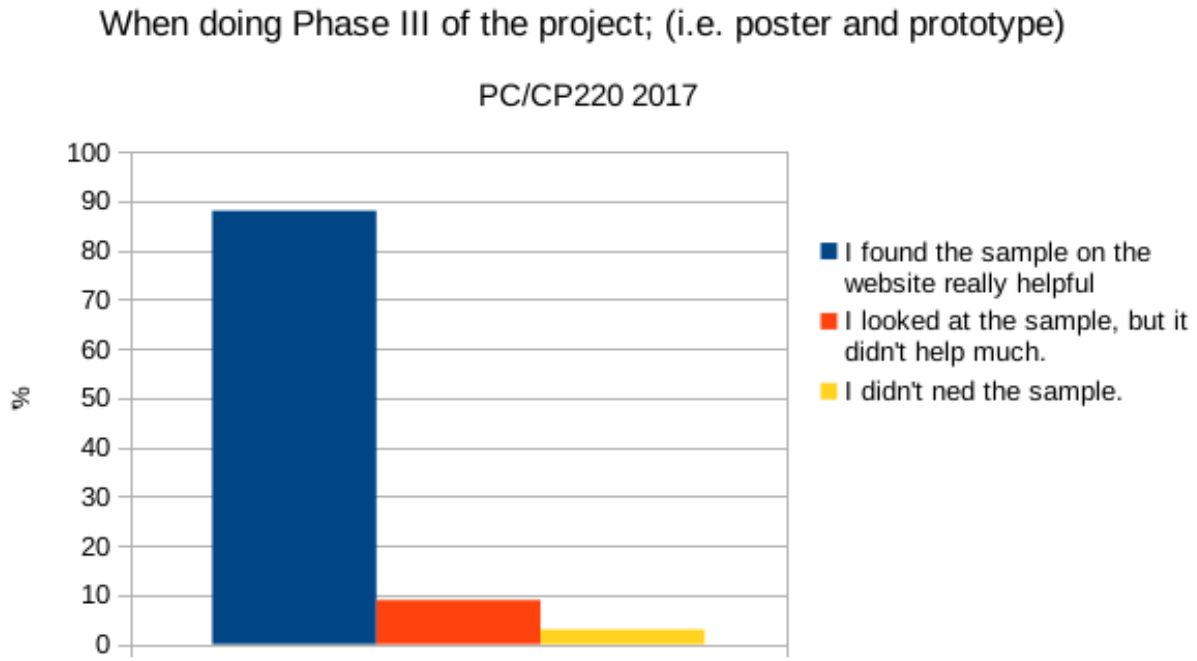
Digital project 2017; work versus interest



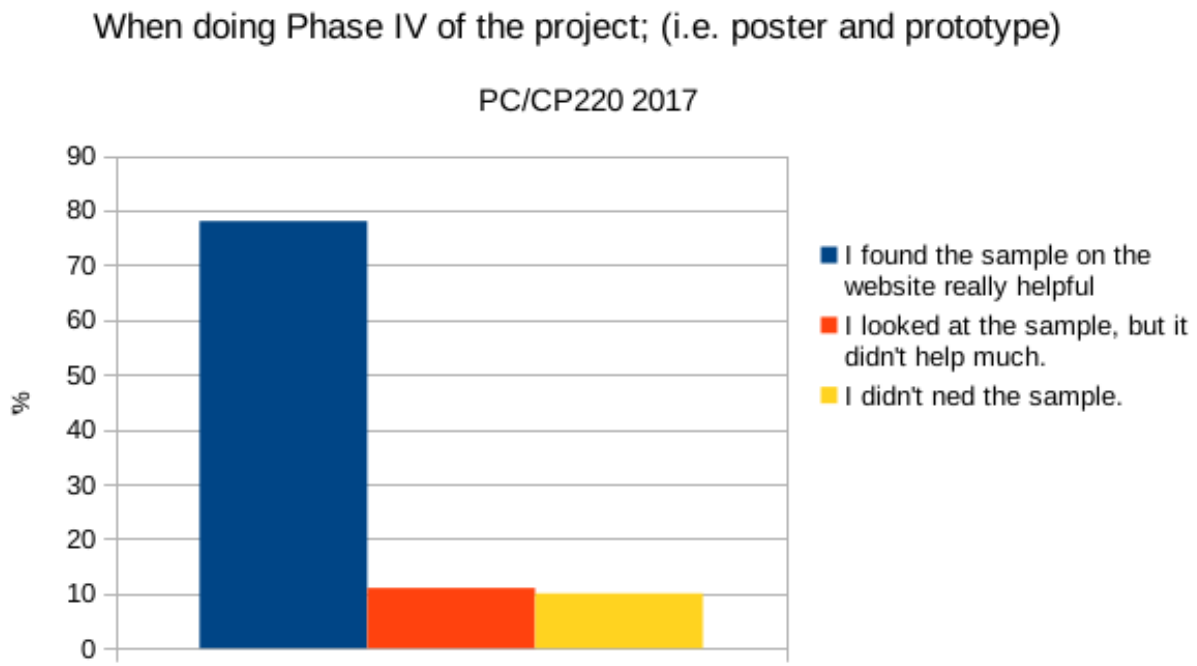
Digital project 2017; value of Phase I example



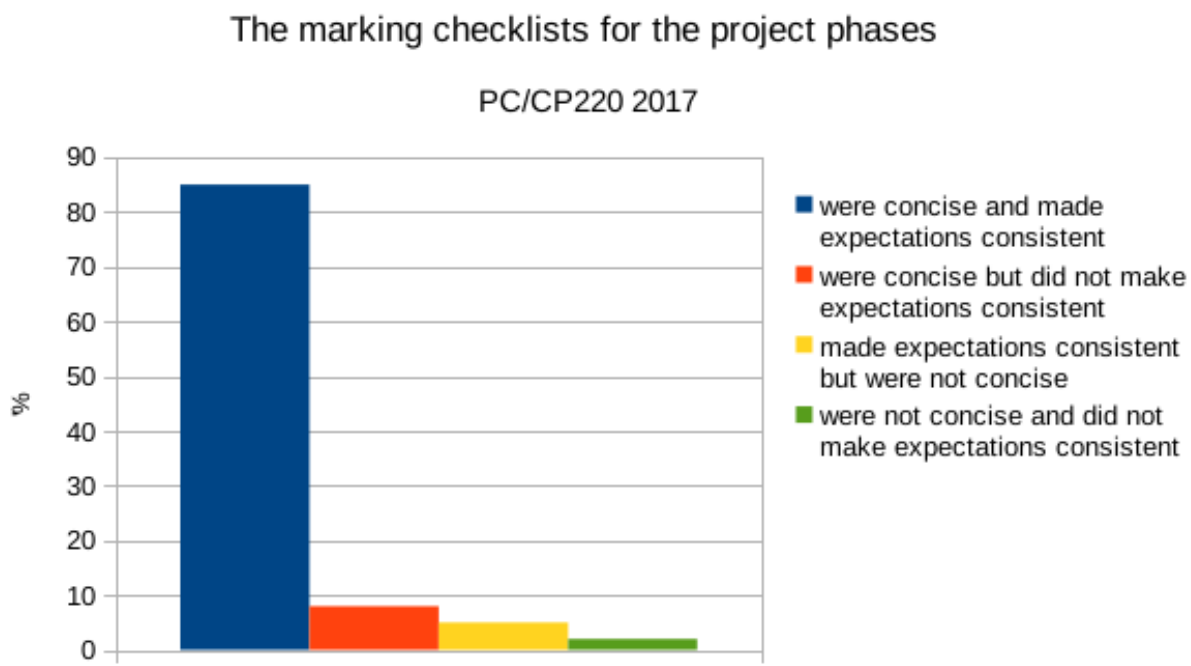
Digital project 2017; value of Phase II example



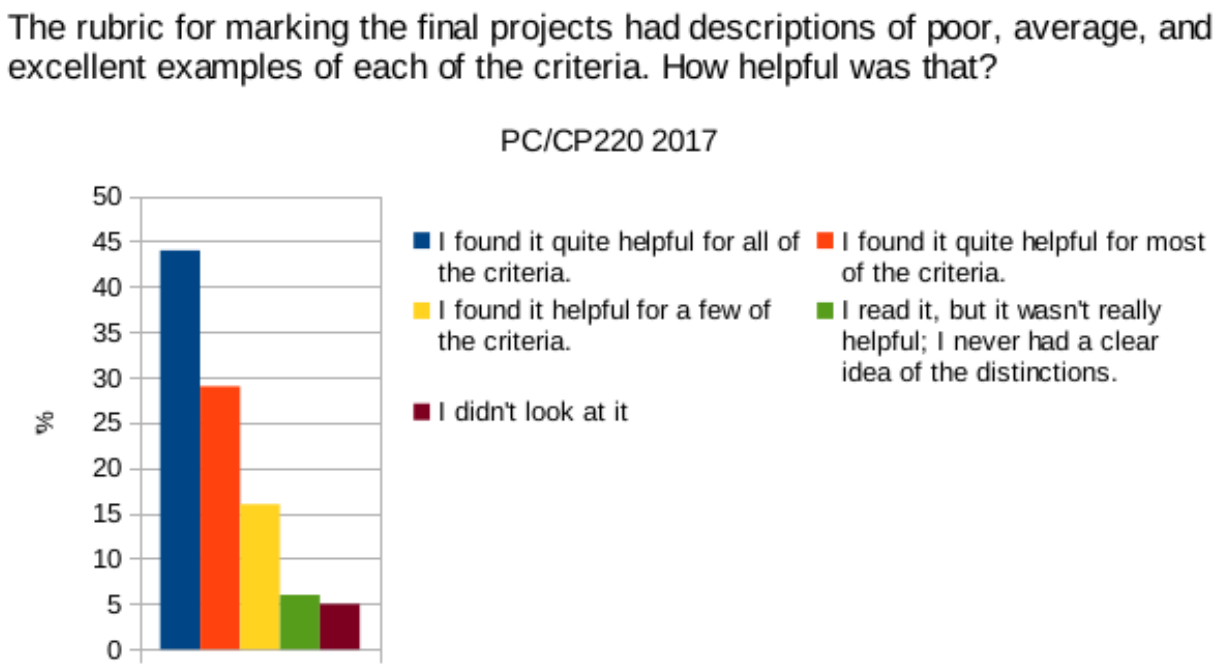
Digital project 2017; value of Phase III example



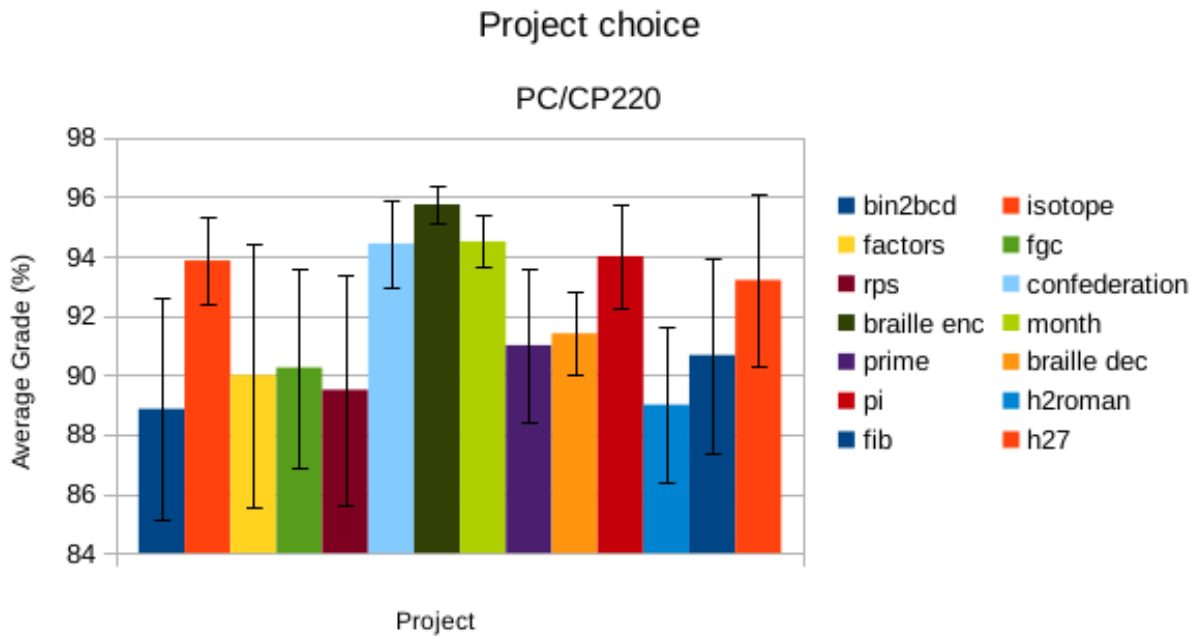
Digital project 2017; value of Phase IV example



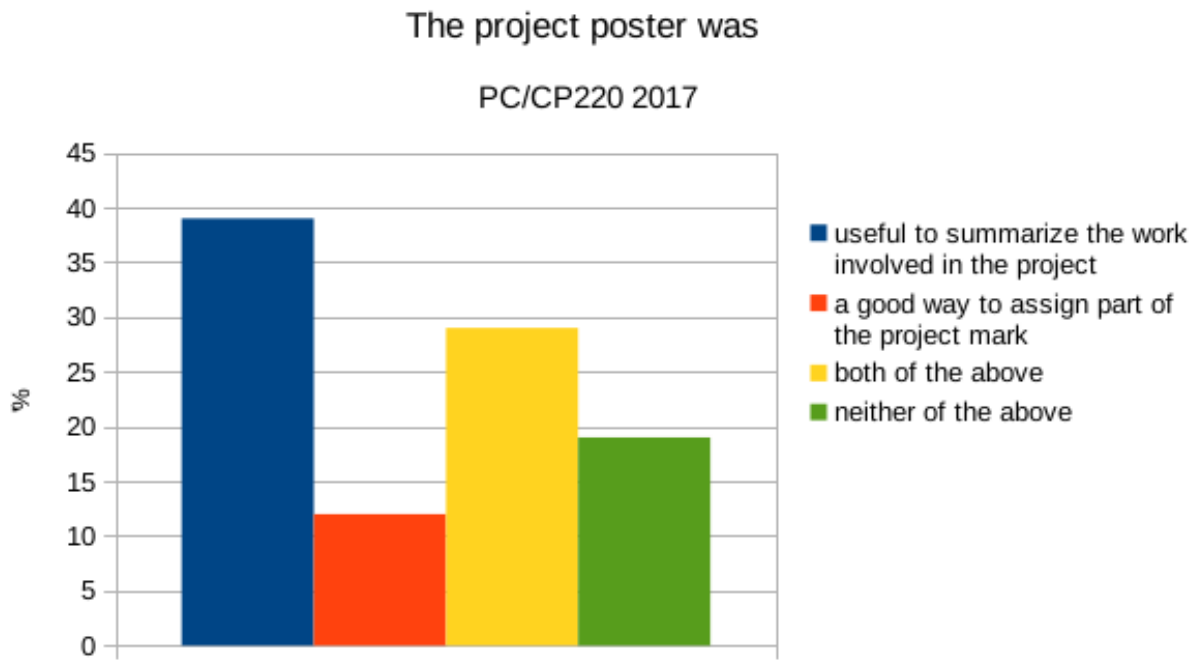
Digital project 2017; value of checklists



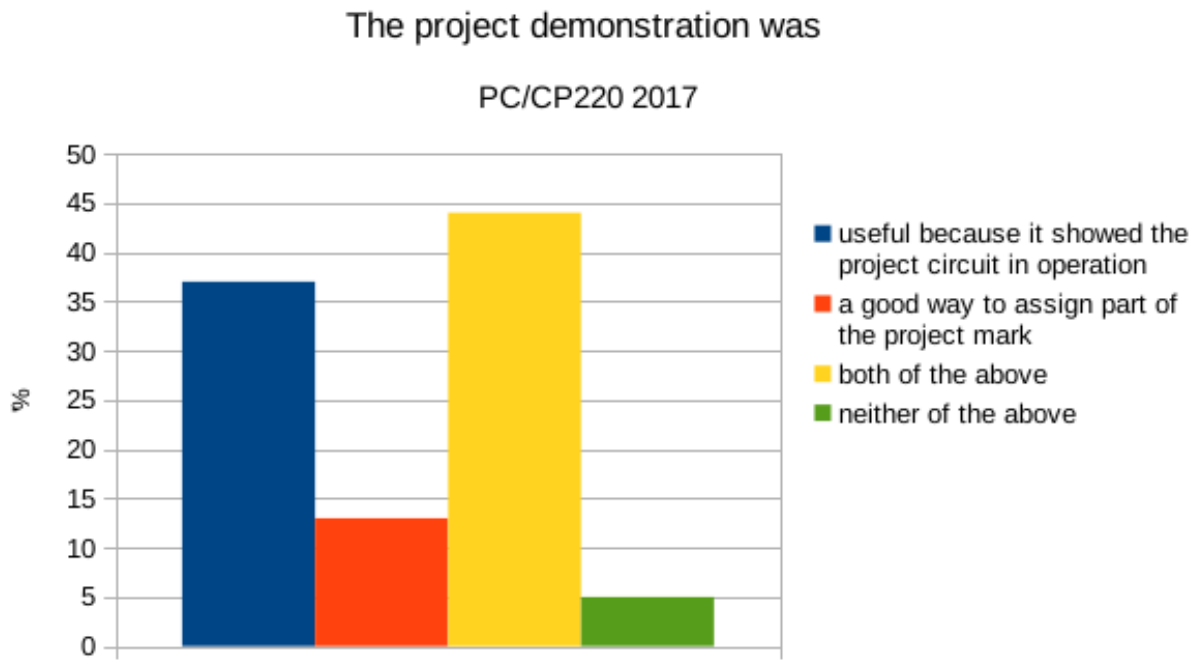
Digital project 2017; value of rubric



Digital project 2017; grade effect of project choice



Digital project 2017; value of poster



Digital project 2017; value of prototype demonstration

Digital project peer marking

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Students give a grade from 1(poor) to 5 (excellent) on 10 criteria.

Digital project peer marking

Students give a grade from 1(poor) to 5 (excellent) on 10 criteria.

They also evaluate their partner's contribution.

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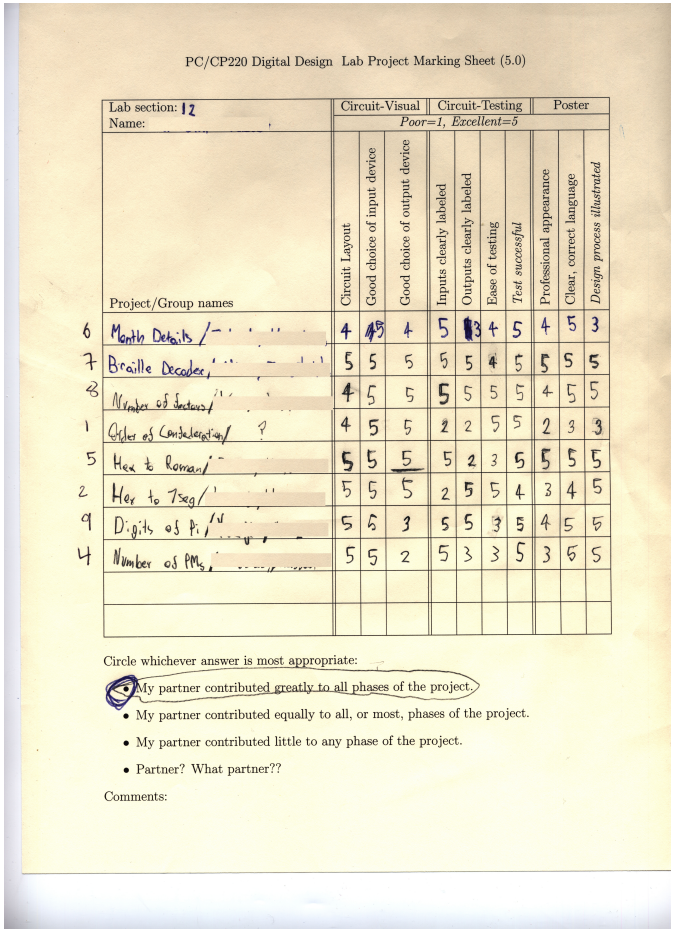
About 90% of partners are happy with each other.



PC/CP220 Digital Design Lab Project Marking Sheet (5.0)

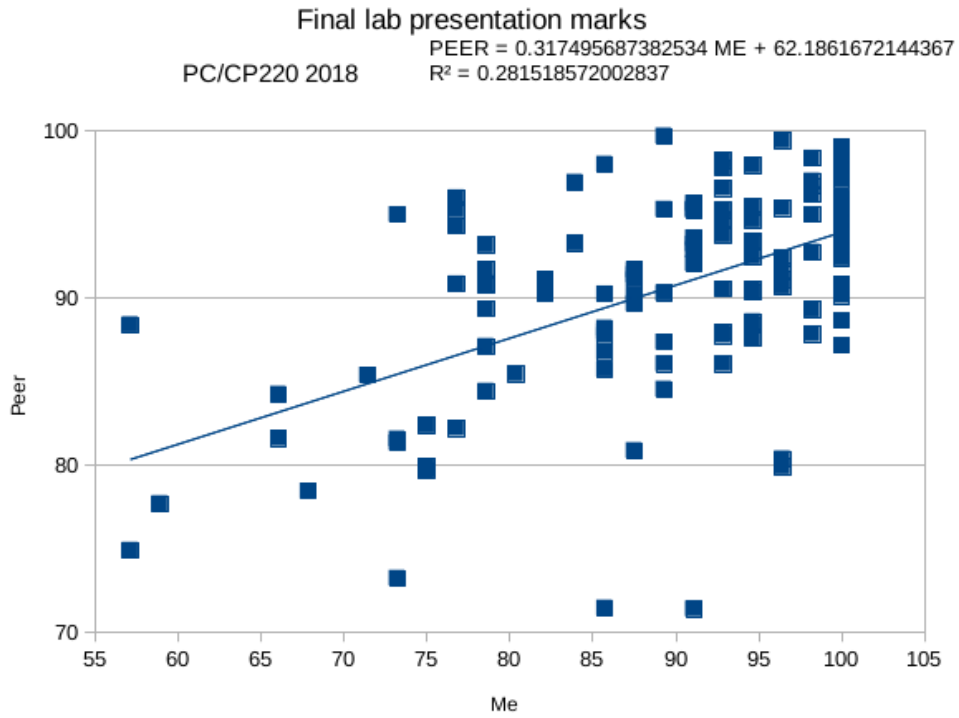
	Lab section: 12 Name:	Circuit-Visual			Circuit-Testing				Poster		
		Poor=1, Excellent=5									
	Project/Group names	Circuit Layout	Good choice of input device	Good choice of output device	Inputs clearly labeled	Outputs clearly labeled	Ease of testing	*Test successful*	Professional appearance	Clear, correct language	*Design process illustrated*
6	Month Details	4	4/5	4	5	3	4	5	4	5	3
7	Braille Decoder	5	5	5	5	5	4	5	5	5	5
8	Number of factors	4	5	5	5	5	5	5	4	5	5
1	Order of Complexity	4	5	5	2	2	5	5	2	3	3
5	Hex to Roman	5	5	5	5	2	3	5	5	5	5
2	Hex to 7seg	5	5	5	2	5	5	4	3	4	5
9	Digits of Pi	5	5	3	5	5	3	5	4	5	5
4	Number of PMs	5	5	2	5	3	3	5	3	5	5

Circle whichever answer is most appropriate:

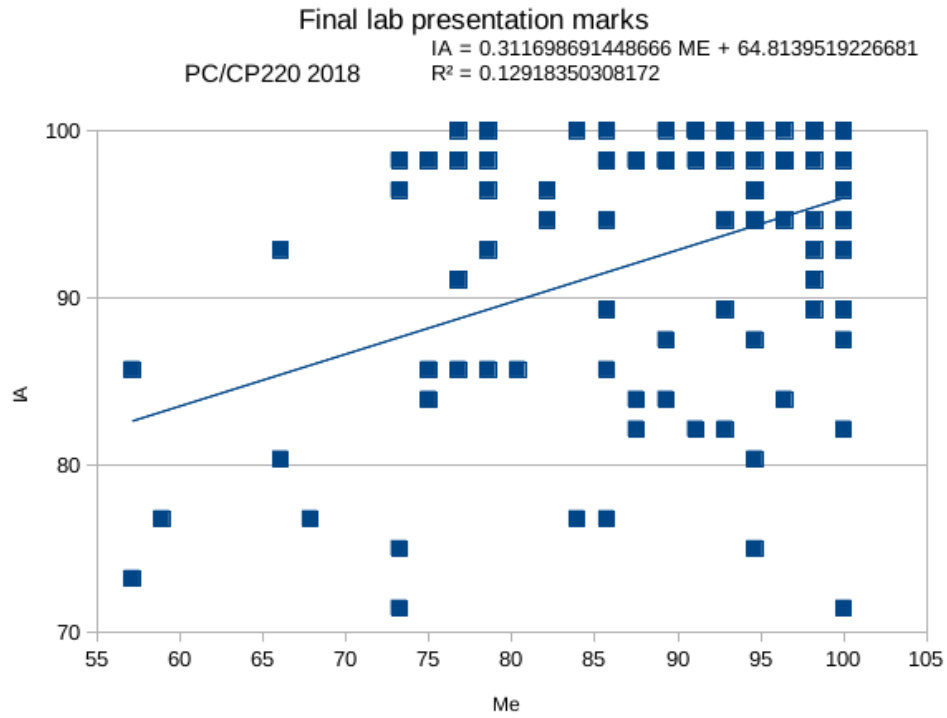
- My partner contributed greatly to all phases of the project.
- My partner contributed equally to all, or most, phases of the project.
- My partner contributed little to any phase of the project.
- Partner? What partner??

Comments:

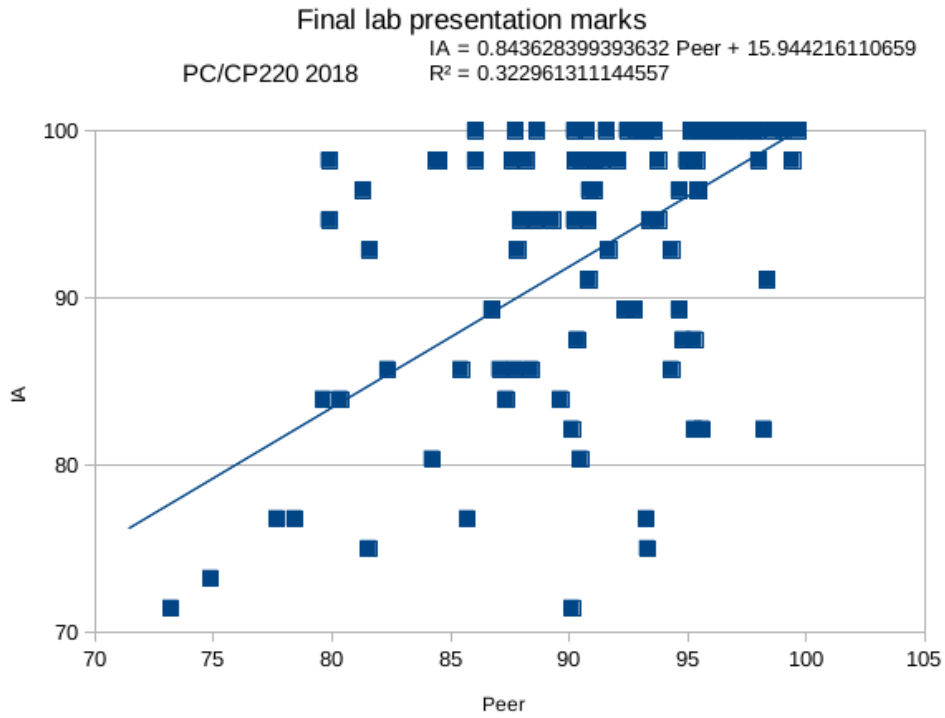
Digital project peer marking



Digital project correlation Peer vs. Me (peer marking)



Digital project correlation IA vs. Me (peer marking)



Digital project correlation IA vs. Peer (peer marking)

Video project

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Students fill out *short* form for *all* of the projects.

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Students fill out *short* form for *all* of the projects.

Students fill out *long* form for *two* of the projects.

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I compile results and return to students.

Video project

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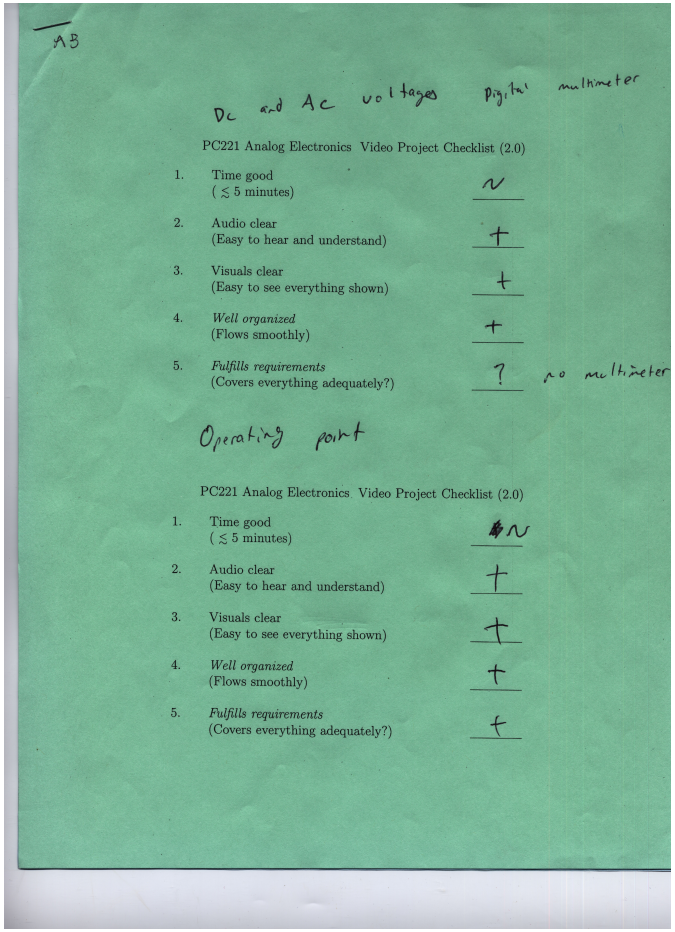
I compile results and return to students.

The long form is just the short form with room for comments.



AB

Dc and Ac voltages Digital multimeter

PC221 Analog Electronics Video Project Checklist (2.0)

1. Time good (≲ 5 minutes) ~
2. Audio clear (Easy to hear and understand) +
3. Visuals clear (Easy to see everything shown) +
4. *Well organized* (Flows smoothly) +
5. *Fulfills requirements* (Covers everything adequately?) ? no multimeter

Operating point

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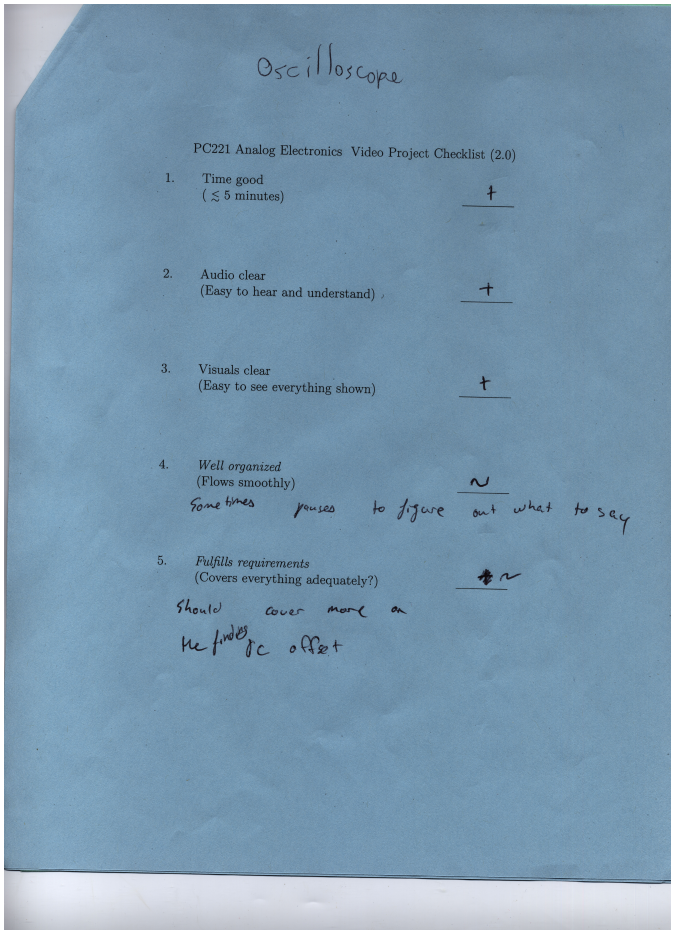
Video short feedback form 2013



Oscilloscope

PC221 Analog Electronics Video Project Checklist (2.0)

1. Time good
   ($\lesssim$ 5 minutes) +

2. Audio clear
   (Easy to hear and understand) +

3. Visuals clear
   (Easy to see everything shown) +

4. *Well organized*
   (Flows smoothly) ~
   Sometimes pauses to figure out what to say

5. *Fulfills requirements*
   (Covers everything adequately?) + ~
   Should cover more on
   the finder pc offset

Video long feedback form 2013

Student designed experiments

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This was in an optics course.

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It works well because experiments are quite independent.

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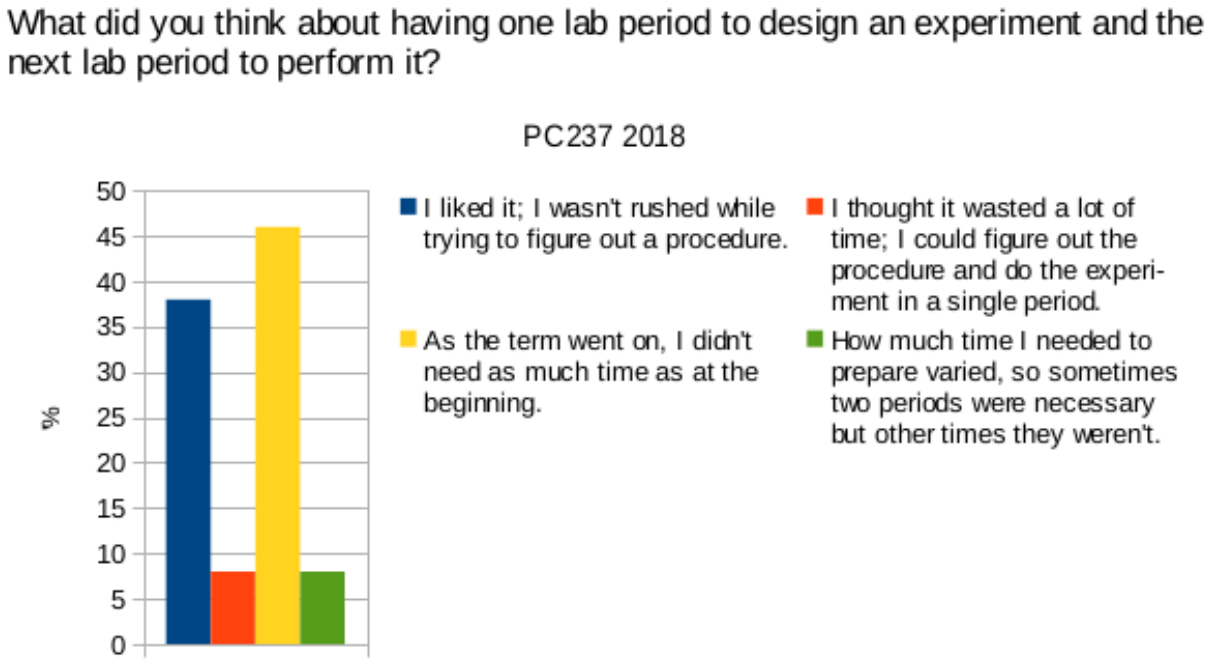
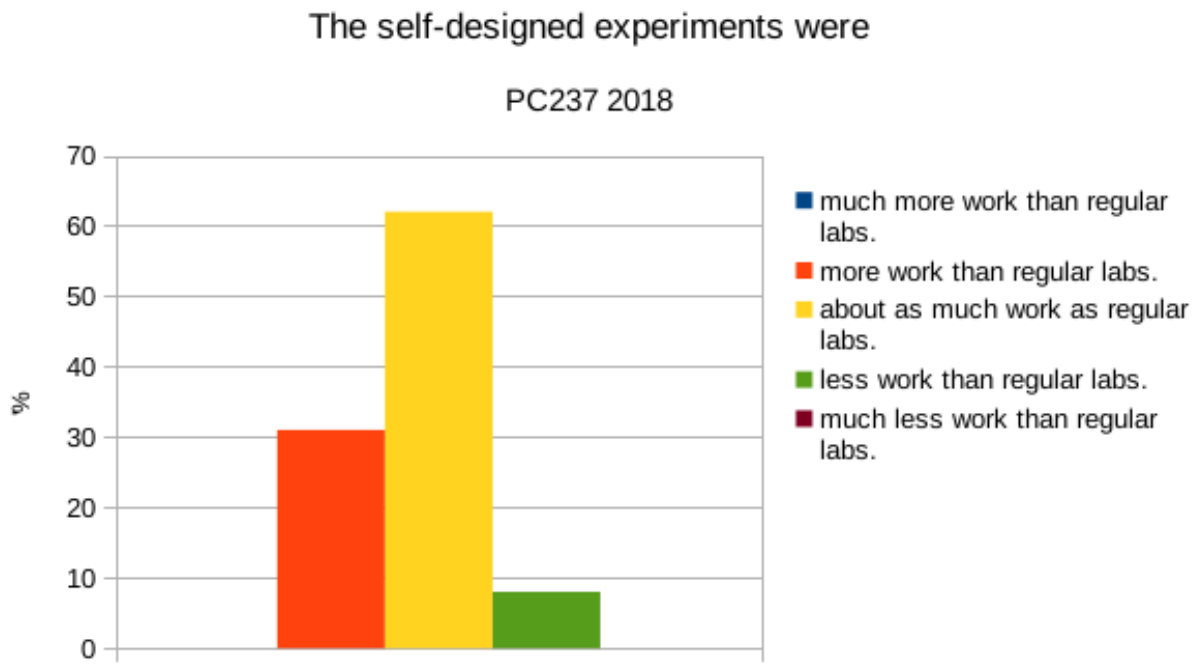
It works well because experiments are quite independent.

The same equipment can be used to examine various phenomena.



Self-designed experiments 2018



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